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Analytical method to determine optimal out-of-band gain in multi-bit delta-sigma modulator

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Abstract: A simple, systematic and deterministic MATLAB simulation which employs Risbo method and analytical simulation is proposed to determine the optimal out-of-band gain to achieve a maximal SNR and the maximum stable amplitude in a multi-bit delta-sigma modulator. Using the proposed method, a 128 MS/s, 2 MHz signal bandwidth 4^{th} order 2-bit continuous-time delta-sigma modulator is designed and implemented in 0.18 μm CMOS technology to verify the concept. As a result, the modulator achieves a peak SNDR of 79.3 dB and a dynamic range of 83 dB for a 2 MHz signal bandwidth (OSR = 32) while consuming only 7.8 mW from 1.8 V supply.

Keywords: analog-to-digital conversion, continuous-time delta-sigma modulator, feedforward, excess loop delay

Classification: Integrated circuits

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1 Introduction

In recent times, continuous-time delta-sigma modulators have gained tremendous attention because of their exceptional features such as inherent anti-aliasing filter (AAF), relaxed gain-bandwidth requirement on active elements resulting in a low power consumption compared to their counterpart discrete-time delta-sigma modulator [1].

The method to determine the out-of-band gain in [2] is neither deterministic nor systematic. Here, we propose a simple, systematic and deterministic approach to determine the out-of-band gain (OBG) for optimized noise transfer function (NTF) synthesis which maximizes the SNR and the maximum stable amplitude (MSA) simultaneously. For illustration, we present the design of a 4^{th} order 2-bit continuous-time delta-sigma modulator operating at 128 MS/s with a signal bandwidth of 2 MHz. The design is simulated in 0.18 μm CMOS technology with supply voltage of 1.8 V which achieves a peak SNDR of 79.3 dB and a dynamic range of 83 dB that are well suited for UMTS application. To relax the requirement on operational amplifier and to save power, one clock excess loop delay (ELD) compensation is employed. Moreover, a capacitive summation technique using the opamp of the last integrator is realized to save power.

2 System level designs

System level design is done using MATLAB. To reduce the circuit complexity, a single loop topology is chosen. A 4^{th} order NTF with oversampling ratio (OSR) of 32 is sufficient to result in a SNDR of 80 dB for a signal bandwidth of 2 MHz. A multi-bit quantizer is preferred to a single bit because of its several advantages over a single bit quantizer [3].

In a delta-sigma modulator, to ensure the maximum SNR and stability, out-of-band gain (OBG) is critical. For a delta-sigma modulators with single-bit quantizer, a heuristic result called Lee's criterion states that modulator is likely to be stable if the out-of-band gain (OBG) is less than 1.5. For a multi-bit quantizer, the criterion [3] to ensure stability is given by Eq. (1).

$$MSA \leq M + 2 - \|h\|_1 \tag{1}$$

$$\|h\|_1 = \sum_{n=0}^{\infty} |h(n)| \tag{2}$$

In Eq. (1) and Eq. (2) M is the number of steps, $\|h\|_1$ is the out-of-band gain (OBG) and $\|h\|_n$ is the inverse z-transform of the NTF H (z). However, Eq. (1) is sufficient but not the necessary criterion when poles and zeros of NTF are optimized [3]. Even with an aggressive NTF, MSA can further be increased and therefore stability must be determined through extensive simulation. A higher OBG limits the maximum stable amplitude and thereby reduces the dynamic range. Hence, OBG optimization is desirable to meet both SNR and dynamic range requirement. We employ a simple and systematic approach to optimize SNR and MSA through MATLAB simulation, and determine the best suitable OBG as follows. First, NTF is synthesized

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for a range of OBG and the MSA is determined using Risbo method. Then the DSM is simulated for the determined MSA which provides the maximum stable SNR. The plots of maximum SNR and MSA against OBG provide the optimum OBG where increase in SNR significantly reduces the MSA. This approach results in a multi-bit modulator with an aggressive NTF which is stable with optimal SNR and MSA. As per simulation result shown in Fig. 1, the MSA is 2.7 (for LSB size 2 and full scale 4). According to Eq. (1), the OBG should be less than 3.29. However, as per simulation for such high OBG, the MSA drops drastically beyond −10 dBFS which highly limits the dynamic range. Therefore, considering the trade-off between the SNR and the MSA, the optimal OBG is chosen to be 2. Finally, the NTF is determined using the *synthesizeNTF* function available in [4].

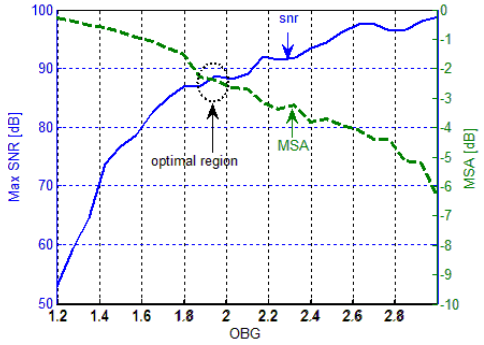

Fig. 1. SNR and MSA versus the out-of-band gain (OBG) of the NTF for 4^{th} order 2-bit DSM.

The finite regenerative time of flash converter and digital logic delay time in the feedback introduce extra delay, excess loop delay (ELD), in the loop and thus increase the order of the modulator. One of the efficient methods to compensate ELD is coefficient tuning by adding a direct path between the DAC output and the flash input [1]. From the circuit design and operation point of view, it is easier to compensate for half a clock or integral multiple of half a clock. Here, we compensate for one clock delay to relax the requirement on analog building blocks. The discrete-time (DT) coefficients of a modulator must be translated into continuous-time (CT) coefficients in accordance with the DAC pulse shape. NRZ DAC pulse is preferred to other DAC pulse shapes because of its higher immunity to clock-jitter. For NRZ DAC and one clock ELD compensation, the discrete-time coefficients are converted into the continuous-time using the function *realizeNTF_ct* in [4] and scaled.

The block diagram of the loop filter is shown in Fig. 2 [5]. The fourth integrator is used to integrate with R_4C_4 and opamp and the same opamp is used to sum feedforward voltages with a_0C_4, a_1C_4, a_2C_4 and, a_3C_4 along with C_4. The coefficients a_0, a_1, a_2 and a_3 are realized with the capacitive sum while the coefficient a_4 is embedded in the integration with R_4C_4. This completely eliminates the summation opamp and thereby saves a significant amount of power. The determined CT coefficients are translated into "R"

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and "C" values with the thermal noise constraint as per Eq. (3) [1].

$$R_1 = \frac{v_{in}^2/2}{32kTf_B * 3 * 2^{2B-1}} \tag{3}$$

In Eq. (3), R_1 is the resistance at the input of the first integrator, v_{in} is the input signal voltage, k is Boltzmann constant, T is the temperature, f_B is the frequency bandwidth and B is the effective number of bit. A 16384 point Hann window PSD predicts a peak SNDR of 84.2 dB for a single tone at 203.125 KHz.

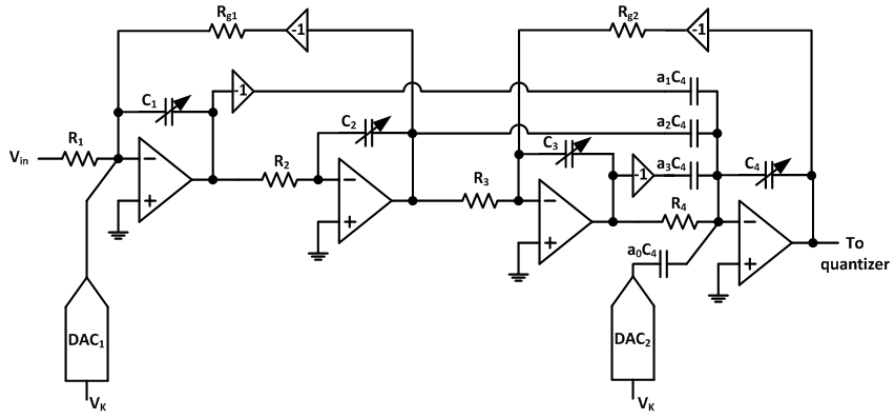

Fig. 2. Loop filter using the capacitive feedforward and last integrator as summation amplifier.

3 Circuit design

In this section, we describe the circuit implementation of the building blocks used in the modulator.

3.1 Opamp

A generic two stage miller compensated opamp is used for a high speed and a wide output swing. Long length input transistors are used to mitigate the input referred flicker noise. To reduce the power consumption and make the stability simple, the opamp is optimized with only one common mode feedback (CMFB) loop to hold the common mode output voltage at V_{cm}. The opamp draws a total current of 0.94 mA, including the CMFB and biasing, from a supply of 1.8 V.

3.2 Comparator

A fully differential comparator from [1] with SR-latch is used in the flash converter.

3.3 Feedback DAC

For excess loop compensation by one clock, the output of the flash converter must be retimed. A retiming d-flip-flop (DFF) is designed to perform this

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task. A current steering DAC is chosen to ensure high speed operation. The cascade current source in the DAC cell is used to achieve a high output resistance of 70 KΩ.

4 Results and discussions

From the system design as explained in section 2, a 4^{th} order 2-bit continuous-time delta-sigma modulator is designed in 0.18 μm CMOS technology. Fig. 3 shows the modulator output spectrum for a single tone at 203.125 KHz. A 16384 point Hann window PSD is produced to ensure the sufficient accuracy. The determined peak SNDR is 79.3 dB (a 5 dB lower SNDR than the predicted one due to circuit non-idealities). Table I summarize the overall performance of the modulator and compare it with the state of the art design. From Table I, it is evident that, the proposed design has a better SNDR dB, a higher dynamic range by 4 dB at the cost of a lower power resulting in a FoM of 0.26 pJ/conv.

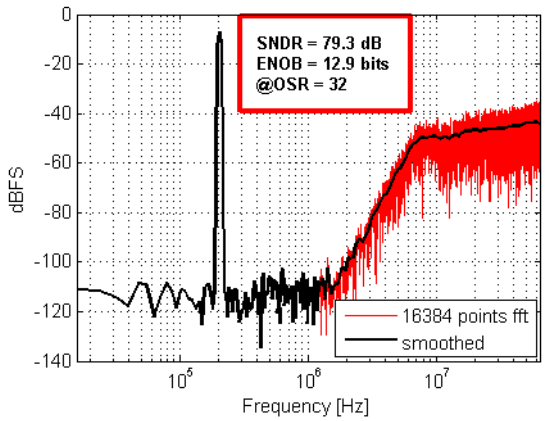

Fig. 3. Output power spectrum of the modulator for a single tone input at 203.125 KHz.

Table I. Performance Summary.

Parameter	Ref [6]		this work
Signal Bandwidth	1.92 MHz		2 MHz
Sampling Frequency	46.08 MHz	61.44 MHz	128 MHz
DR	70 dB	79 dB	83 dB
Peak SNDR	65 dB	77 dB	79.3 dB
Input Range (diff)	0.7 V_{pp}	1.4 V_{pp}	1.8 V_{pp}
FoM*	0.6 pJ/conv	0.3 pJ/conv	0.26pJ/conv
Power Consumption	3.5 mW	7.4 mW	7.8 mW
Power Supply	1.2 V		1.8 V
Process	0.13 μm		0.18 μm
* (FoM = Power/(2.BW.2^{ENOB}))			

5 Conclusion

A simple and systematic MATLAB simulation is proposed to determine the optimal out-of-band gain (OBG) in a multi-bit delta-sigma modulator. To

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verify the proposed methodology, the determined OBG is used to implement a 128 MS/s, 2 MHz signal bandwidth 4^{th} order 2-bit continuous-time delta-sigma modulator in 0.18 μm CMOS technology. As a result, the modulator achieves a peak SNDR of 79.3 dB and a dynamic range of 83 dB for a 2 MHz signal bandwidth (OSR = 32) which is well suited for UMTS applications. The modulator consumes 7.8 mW power from a 1.8 V supply to achieve FoM of 0.26 pJ/level.

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