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A dual-mode single-inductor dual-output dc-dc converter with fast transient response

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Abstract: A novel integrated single-inductor dual-output (SIDO) buck converter with peak current common-mode and the two output voltage ripples comparison differential-mode control method in continuous conduction mode is presented. The system can use only one inductor to provide two independent output voltages, 1.2 V and 1.8 V, with a maximum total output current 460 mA. The proposed converter has been fabricated in a 0.18 μm 1P6M CMOS process. Experimental results show the load transient response time is only 8 μs and the cross-regulation is about 0.05 mV/mA when the load current suddenly changes 200 mA. The maximum power conversion efficiency 93.5% is achieved at total output power 240 mW.

Keywords: single-inductor dual-output, transient response, common-mode, differential-mode

Classification: Integrated circuits

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1 Introduction

To achieve high speed and low power consumption, portable applications need different supply voltages for different modules. In previous years, using two or multiple single-inductor dual-output (SISO) DC-DC converters to build a power supply system is a kind of solutions [1]. Now a more interesting and efficient solution is adopted to use just one single inductor to obtain two or multiple outputs, which benefits with significant overall cost saving, small size and light weight of device [2].

Some kinds of SIDO switching converters have been reported in recent years. The converter in Ref. [3] works in discontinuous conduction mode (DCM) which makes use of the time-multiplexing control. This control method makes the two channels independent of each other which can reduce the cross-regulation but suffers from larger output voltage ripples, lower conversion efficiency and lower output current. The converter in Ref. [4], working in pseudo continuous conduction mode (PCCM), can increase the output current and decrease the output voltage ripples. However, it needs to add a power transistor to generate a constant current for putting the inductor current on a stable value. Therefore, the continuous conduction mode (CCM) has become a hot spot due to its small ripples, high conversion efficiency and large output current. The power-distributive control is adopted to sustain large load current and high conversion efficiency, but serious cross-regulation and slow transient response still exist due to the interleaving energy-conservation mode by the voltage mode control with large capacitor compensation [5]. The SIDO converter in Ref. [6] also uses the control method with large capacitors compensation to control the main loop and the secondary loop respectively. Fortunately, it solves the voltage spike problem by using a flying capacitor. However, the bulk capacitor increases the cost in a real system application and the transient response is limited by the complicated loop design.

In this paper, a novel control with peak current common-mode and the output voltage ripples comparison differential-mode is proposed to increase the transient response. The peak current mode control is used to regulate the total energy from the input supply to the output load in the main loop. The peak current loop without large capacitor compensation is adopted to improve transient response speed of the main loop. The two output voltage ripples comparison control is adopted to increase the transient response

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speed of the secondary loop, which distributes the energy to the two outputs. Besides, the peak conversion efficiency is improved by the simple structure implementation.

2 Proposed SIDO DC-DC converter structure

Fig. 1 (a) illustrates the proposed SIDO buck converter, which uses peak current common-mode to control its main loop and the two output voltage ripples comparison differential-mode to control its secondary loop. Based on the classical buck converter topology, the power stage of the SIDO converter is obtained by adding another two switches at the output node of the inductor. S_1 and S_2 in the main loop are used to regulate the total input energy. S_3 and S_4 in the secondary loop are used to distribute the energy to the two outputs.

The main loop is made up of error amplifier (EA), PWM comparator, flip-flop, ramp compensation and current sensing circuit. The two output voltages V_1 and V_2 are set constantly to be 1.8 V and 1.2 V respectively. To make sure that the output voltage ripples are equal in value, the common-mode voltage should be set as $K(V_1 + V_2)$. In this design, K is a constant sampling value which chooses 2/5.

The EA amplifies the difference between $2(V_1+V_2)/5$ and V_{ref} (1.2 V). Its output is compared with the sampled inductor current and then generates the main loop duty cycle D_1. The secondary loop is made up of the comparator, slope compensation and flip flop. The first sampling output voltage K_1V_1

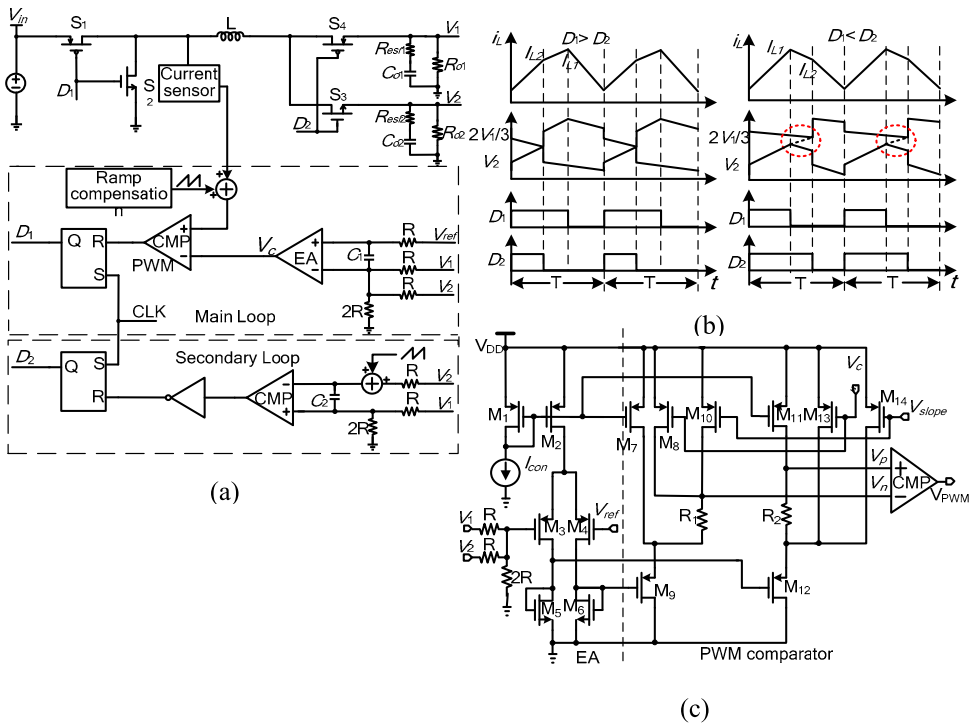

Fig. 1. The system block of the SIDO converter: (a) the proposed system schematic; (b) the control waves of the two output voltages and inductor current; (c) the circuits of the EA and PWM comparator

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compares with the second sampling output voltage K_2V_2 to generate the secondary loop duty cycle D_2. Here K_1 and K_2 are the constant sampling values. In the steady state, K_1V_1 must be equal to K_2V_2. In this design, K_1 chooses 2/3 and K_2 chooses 1.

The method of the two output voltage ripples comparison is used in the secondary loop to increase the transient response which is similar to the ripple control method in the SISO converter. So when the load current changes suddenly, the secondary duty cycle D_2 can change quickly. However, the two output voltages cannot keep stable under all conditions if this method is used directly. In the steady state, $D_1 = \dfrac{D_2V_1 + (1-D_2)V_2}{V_{in}}$ and $D_2 = \dfrac{I_{o1}}{I_{o1}+I_{o2}}$, it is uncertain which value is bigger. The crossing point of the two output voltages can be got easily when $D_1 > D_2$ as shown in Fig. 1 (b). However, when $D_1 < D_2$, the ripple voltages of the two outputs all decrease during the time D_1T to D_2T in one period as the dotted line circle shown in Fig. 1 (b), the two output voltages cannot be intersected. So the two output voltages would not be stable under this condition. Therefore, the slope compensation in the secondary loop is presented to suppress this problem. When $D_1 < D_2$, the two output voltage ripples are defined as

$$V_{1\_Ripple} \approx I_{L2}R_{esr1}. \tag{1}$$

$$V_{2\_Ripple} \approx I_{L2}R_{esr2} + \frac{I_L(1-D_1)T}{C_{o2}}. \tag{2}$$

where R_{esr1} and R_{esr2} are the equivalent series resistances of the output capacitor C_{o1}, C_{o2} respectively. I_{L2} is the inductor current at $t = D_2T$ in one period. I_L is the average inductor current. In the steady state:

$$\frac{2}{3}\left(V_1 - \frac{V_{1\_Ripple}}{2}\right) = V_2 + \frac{V_{2\_Ripple}}{2} + M_aD_2T. \tag{3}$$

where M_a is the slope of the compensation ramp signal in secondary loop. If M_a is too small, Eq. (3) will be inconsistent and the two output voltages will not keep stable. So the value of the secondary loop compensation M_a must be set right and then the two output voltages can keep stable. Therefore, the two output voltage ripples comparison differential-mode with the slope compensation method in the proposed SIDO converter can not only keep the two output voltages stable but also increase the transient response under all conditions.

The main loop control schematic implementation including the differential-in differential-out (DIDO) EA and PWM are shown in Fig. 1 (c). The main loop slope compensation is added with the current sensing signal to eliminate the sub-harmonic problem. In order to increase the transient response, the DIDO error amplifier without large capacitor compensation is adopted in the proposed converter. In the conventional converter, the large capacitor in the output of the EA is used to keep the system loop stable, but it would decrease the slew rate of the EA. So the setting phase of output voltage transient response will become long [7]. Then the transient response time and overshoot voltage or undershoot voltage all become worse. Therefore in

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the proposed coverter, this large capacitor is deleted to improve the transient response and the lower DC gain of EA is adopte to keep the system stable. But the load regulation of the converter would be sacrificed in some extent. Therefore the constant voltage on the resistance R_2 as the simple compensation to improve load regulation is adopted in the proposed converter. The differential input signal of the PWM comparator is shown as follows:

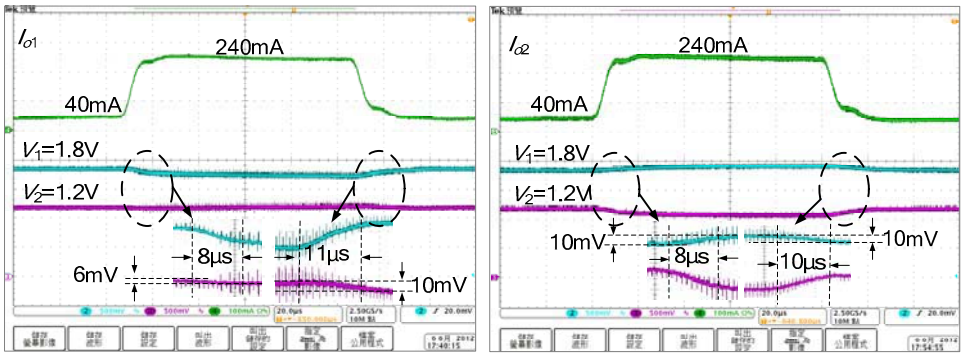
$$V_p - V_n = A(2(V_1 + V_2)/5 - V_{ref}) - (I_{cs} + I_{slope})R_1 + I_{con}R_2. \quad (4)$$

where A is the DC gain of the EA, I_{cs} is the sensing inductor current, I_{slope} is the slope compensation current and I_{con} is the constant compensation current. In the Eq. (4), the DC compensation term $I_{con}R_2$ is equal to increase the DC gain of the error amplifier. Therefore, the transient response is increased by proposed method and without the large loss of the load regulation.

In addition, the cross-regulation is an intrinsic problem of CCM control in the SIDO. If the common-mode and differential-mode control method is used in the converter, the two outputs will partly suppress the cross regulation [6]. Therefore, the proposed peak current common-mode and comparator differential-mode method will recede this problem.

3 Experimental results

The proposed buck SIDO converter has been fabricated in Chartered 0.18 μm 1P6M CMOS process. The chip area is 1.9 mm × 1.6 mm including all pads. The off-chip inductor is 4.7 μH and the filter capacitors both are 20 μF. Fig. 2 shows the measured transient response results of the test chip. The two output voltages can be set 1.2 V and 1.8 V, respectively. The transient response waves when I_{o1} changes between 40 mA and 240 mA with I_{o2} of 80 mA are shown in Fig. 2 (a). The transient response time is about 11 μs and the two output voltage variations are about 25 mV, 10 mV. The transient response waves when I_{o2} changes between 40 mA and 240 mA with I_{o1} of 80 mA are shown in Fig. 2 (b). The transient response time is about 10 μs and the two



(a) (b)

Fig. 2. Measured transient response results @: (a) I_{o2} = 80 mA, I_{o1} changing between 40 mA and 240 mA; (b) I_{o1} = 80 mA, I_{o2} changing between 40 mA and 240 mA

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Table I. Performance and comparison of SIDO converters

	Jing's [4]	Lee's [5]	Xu's [6]	This work
Process	0.35μm CMOS	65nm CMOS	0.25μm CMOS	0.18μm CMOS
Power Supply	1.8-2.4 V	2.7-3.6V	2.7-5 V	2.7-3.6 V
Switch Frequency	1.25MHz	1MHz	1.3MHz	1.27MHz
Output Voltage	3.0V/3.6V	1.2V/1.8V	1.2V/1.8 V	1.2V/1.8 V
Inductor/Capacitor	1μH/4.7μF	4.7μH/4.7μF	4.7μH/47μF	4.7μH/20μF
Load Current	0.4A/0.6A	0.3A/0.3A	0.4A/0.2A	0.24A/0.24A
Transient Response	120μs ($\triangle I_{load}$=0.3A)	25μs ($\triangle I_{load}$=0.17A)	12μs ($\triangle I_{load}$=0.27A)	8μs ($\triangle I_{load}$=0.2A)
Cross-regulation	0.033mV/mA	0.075mV/mA	0.18mV/mA	0.05mV/mA
Load-regulation	<2%	<10%	<3%	<2%
Ripple	200mV	100mV	39mV	45mV
Peak Efficiency	91.6%	91%	87%	93.5%
Area(mm^2)	2.16	1.44	5.29	3.04

output voltage variations are about 10 mV, 25 mV. The results also show that the output voltages have no undershoot and overshoot voltage when the load changes suddenly. The load regulation is about 1.7%.

The performances of the proposed SIDO converter compared with the reported SIDO converters are summarized in Table I. The load transient response time of the proposed converter is the best, 8 μs, compared with the other designs. Moreover, the other performances have not been sacrificed such as the cross-regulation, the output voltage ripples and load-regulation. The maximum conversion efficiency is 93.5%, which is also better than the comparison designs.

4 Conclusions

This paper presents a novel control structure for SIDO buck converter, which use peak current common-mode to control its main loop and the output voltage ripples comparison differential-mode to control its secondary loop. The test chip has been fabricated in a standard 0.18 μm CMOS process. The response time is only 8 μs and the maximum conversion efficiency is 93.5%. Therefore the proposed SIDO converter is suitable for cost-effective power management of portable applications, especially on the occasion of the fast load change.

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