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A distributed ramp signal generator of column-parallel single-slope ADCs for CMOS image sensors

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Abstract: This paper proposes a distributed ramp signal generator of column-parallel single-slope ADCs for CMOS image sensors. This architecture does not require any power-hungry amplifiers of the conventional one but consists of miniaturized column-wise ramp signal generators connected together by metal wires, which achieves high linearity and high uniformity. Simulation results show less than 1LSB nonlinear error of the ramp signal at 12-bit ADC resolution is attained only by having the consumption current of 6.4 mA and the area of 2.4 mm^2 which are much smaller than the conventional one. It is also confirmed that 100 mΩ resistive connection attains less than 1LSB gain error mismatching, even though the mismatch of the column-wise ramp signal generators is as large as 20%.

Keywords: CMOS image sensors, ramp signal generator, column-parallel single-slope ADC, ultra-high-definition television, mismatch reduction

Classification: Integrated circuits

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1 Introduction

The next-generation vision systems require image sensors with aggressive performance. For instance, in ultra-high-definition television (UHDTV) broadcasting, a 33 Mpixel (8k4k) CMOS image sensor with 12-bit ADC resolution at 120 fps has been developed. A column-parallel ADCs is the key element for the CMOS image sensor to realize the high pixel rate [1, 2, 3]. However the power consumption, which determines dark current noise, is still greater than 2W and the pixel pitch of 2.8 μm is quite large compared with the state-of-the-art pixel size. In order to achieve high speed operation at very low power consumption and finer pitch column implementation, a single-slope ADC (SS-ADC) is an attractive architecture [3, 4]. However, if the horizontal number of pixels becomes as large as 8000, there is a difficulty to supply a ramp signal into all the columns uniformly, even though a power-hungry driver for the ramp signal generator (RSG) is used. In particular, a non-constant gate capacitance of the comparator in SS-ADCs seriously distorts the ramp signal where several thousands of comparators turn over simultaneously. Furthermore, a conventional RSG of the CMOS image sensor for UHDTV applications occupies large area of 5 mm^2 as reported approximately in [3].

This paper proposes a new architecture for ramp signal generation to reduce the power consumption and the waveform distortion of the ramp signal. In this architecture, small-size RSG units are distributed over all the columns and connected with neighboring units together by a same metal wire. The proposed RSG does not require the power-hungry driver amplifier which is essential in the conventional one but has high immunity of the waveform distortion and results in high linearity, just having the consumption current of 6.4 mA and the area of 2.4 mm^2. Moreover the resistive interconnection by the metal wire helps to reduce the influence of inherent mismatching between the columns due to the variation in transistor characteristics caused by semiconductor manufacturing process.

2 Circuit architectures

Fig. 1 describes the architectures of the conventional (Fig. 1 (a)) and proposed (Fig. 1 (b)) RSGs for CMOS image sensors which have 8000 column-parallel SS-ADCs consisting of a comparator and a counter. The time interval from the beginning of the ramp signal to the time when the ramp signal exceeds the pixel output is measured by the counter.

In the conventional architecture (Fig. 1 (a)), one input of the comparator is connected with a ramp signal line. This ramp signal is supplied by a common RSG outside the columns. In this architecture, a power-hungry driver amplifier is necessary to satisfy high linearity and high speed operation because a parasitic resistance r_p and a parasitic capacitance c_p of the ramp signal line distorts the linearity of the ramp signals, depending on bias current of the driver amplifier.

Moreover the ramp signal suffers from the voltage-dependent impedance

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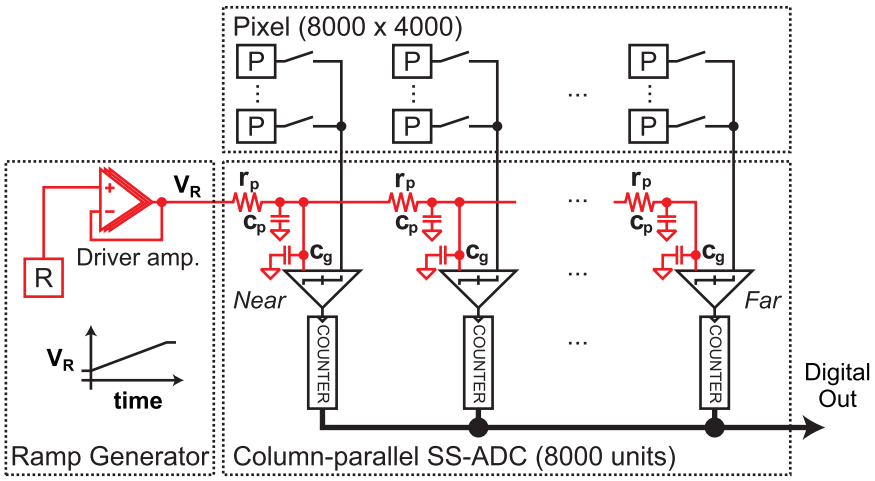
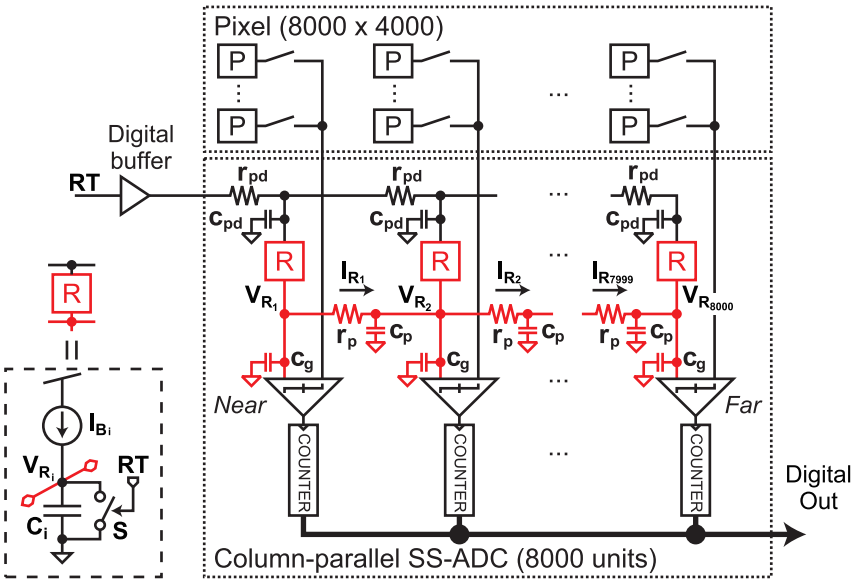


(a) The conventional ramp signal generator



(b) The proposed ramp signal generator

Fig. 1. The architectures for CMOS image sensors

loads because a gate capacitance c_g of the comparator in SS-ADCs has a large variation due to the input transistor's operating point and the ramp signal is distorted particularly when several thousands of comparators turn over simultaneously.

In the architecture of the proposed RSG used at the column as shown in Fig. 1 (b), each SS-ADC consists of an RSG, a comparator and a counter. The i-th ($i = 1, \ldots, 8000$) RSG unit consists of a capacitor C_i, a constant current source I_{B_i} and a switch S controlled by the common reset signal RT whose line has a parasitic resistance r_{pd} and a parasitic capacitance c_{dp}. When the switch is turned off, the ramp signal V_{R_i} is supplied to the comparator and the i-th column pixel output is compared with V_{R_i}. And V_{R_i} is connected with neighboring units ($V_{R_{i-1}}$, $V_{R_{i+1}}$) together by a same metal wire.

One of the features of the proposed RSG is that only digital signal RT is supplied from outside of columns. It is quite easier to maintain the uniformity of the signal by a digital buffer without consuming DC current and the wiring

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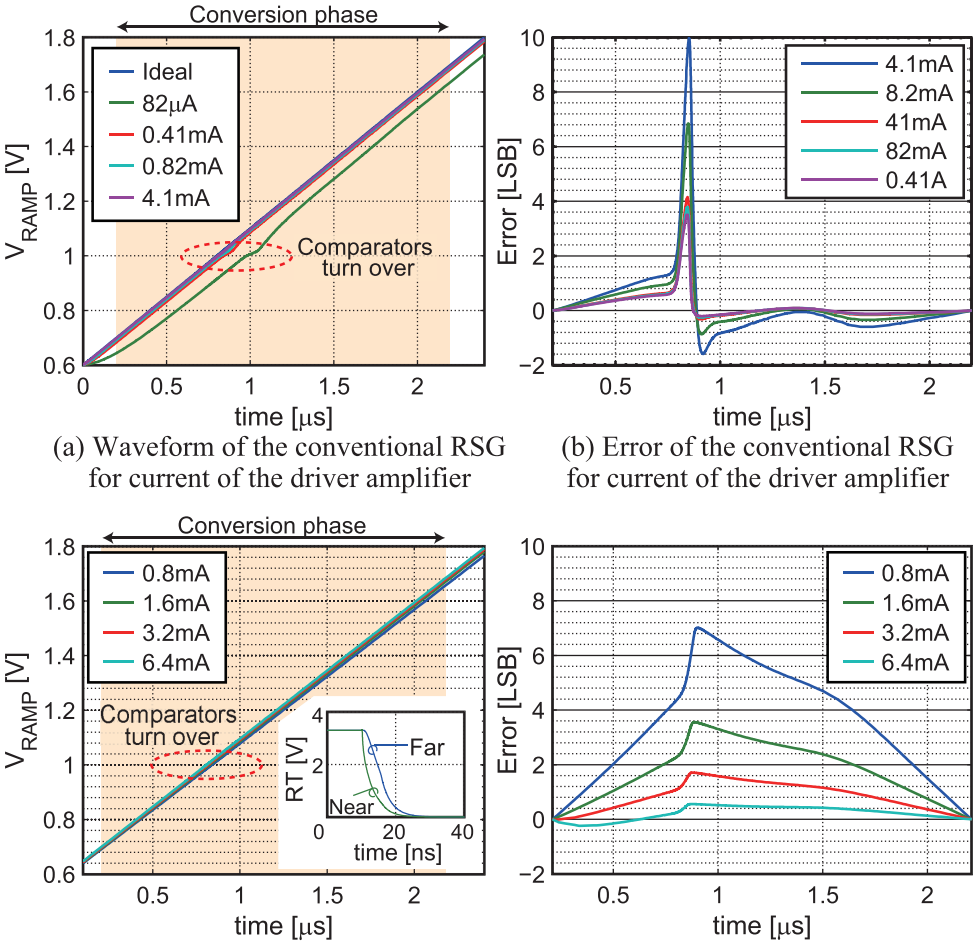
delay of RT is not so severe as the analog ramp signal itself. Moreover using much larger C_i than c_g can reduce nonlinearity due to the gate voltage dependence of c_g.

Another feature is the resistive interconnection of V_{R_i} by the metal wire. The deviation of the ramp signal gain between the columns due to the use of small-size components is reduced by the low-impedance interconnection of neighboring RSG outputs. Since adjacent two nodes are connected by the metal wire, a current I_{R_i} flows along with r_p, if V_{R_i} deviates from $V_{R_{i+1}}$. This current has an effect of averaging the voltage difference between the columns depending on r_p. As a result, the eventual ramp signal mismatch is drastically reduced.

3 Improvement of linearity

Fig. 2 shows characteristics of transient SPICE simulations at the farthest column (the left side) from signal sources (the right side). As the severest condition for the ramp signal, all the pixel outputs are fixed at 1 V, assuming that a row of the pixels is illuminated at the same level and the outputs of the comparators turn over simultaneously when the ramp signal level becomes



(a) Waveform of the conventional RSG for current of the driver amplifier

(b) Error of the conventional RSG for current of the driver amplifier

(c) Waveform of the proposed RSG for the total current of RSGs

(d) Error of the proposed RSG for the total current of RSGs

Fig. 2. Simulation results at the farthest column

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at 1 V. The conversion phase is from 0.2 μm to 2.2 μm, not including very nonlinear starting period. Here we estimates r_p of 10 mΩ, c_p of 2.3 fF, r_{pd} of 100 mΩ and c_{pd} of 0.23 fF, using 0.11 μm CMOS image sensor process.

Fig. 2 (a) shows the results for the conventional RSG. In the parametric simulation, the driver bias current is changed while maintaining the current density of transistors for the driver amplifier in which we employ a single-stage topology. This is a design example but we can immediately notice that the nonlinearity of the ramp signal is closely related to the bias current of the driver amplifier. From Fig. 2 (b), the case of 0.41 A is still larger than 3LSB of the error at 12-bit resolution, which is calculated by comparing the simulated values and the linearly-fitted values during the conversion phase.

Fig. 2 (c) shows the results for the proposed RSG. Here we change the total current of I_{B_i} as the parameter, while C_i is also changed to keep the ratio of I_{B_i}/C_i to 0.5 V/μs. In all the cases, the mean value and the transient peak value of the digital buffer current are 94 nA and 1.2 mA, respectively. Fig. 2 (d) shows that the total current of 6.4 mA, which corresponds to I_{B_i} of 800 nA and C_i of 1.6 pF, can achieve less than 1LSB error. Furthermore this can be implemented within the area of 2.4 mm^2, assuming the use of a MIM capacitor of 8 fF/μm^2. In addition, it should be noted that thermal (kT/C) noise of the RSG is only 51 μV$_{rms}$ and much smaller than 1LSB of 244 μV.

4 Mismatch analysis

For any distributed architectures, the influence of inherent mismatching between the columns due to the variation in transistor characteristics caused by semiconductor manufacturing process is very crucial. However, in the proposed RSG, the mismatch can be reduced by the resistive interconnection of the metal wire. In order to estimate the effect, numerical simulations are conducted by MATLAB. Here we choose C_i of 100 fF and I_{B_i} of 50 nA as very small-size components to investigate the condition that the circuit components greatly deviate from column to column.

Fig. 3 (a) shows relative errors of the ramp signals at the end of conversion, where the standard deviations, σ_C/C and σ_I/I_B are 5%, respectively. For the resistance of 100 MΩ which corresponds to supposing no wire resistive connection, the ramp signals greatly deviate from column to column because of the mismatch on both capacitors and constant current sources. Even 1 kΩ resistive connection well reduces the relative error to be less than $\pm$1%. Using 10 mΩ resistive wire connection, the error can be negligibly small (less than $\pm$0.001%).

Fig. 3 (b) shows how the parasitic resistance and circuit component mismatches are related to the ADC accuracy. The gain error (ΔG) of the ramp signals is expressed as a unit of LSB at 12-bit resolution by using

$$\Delta G = \frac{\Delta g \cdot T_c}{V_{FS}} \times 2^{12},$$

where Δg is the gain error as a unit of volt per second. Assuming that mismatches in the RSGs are normally distributed over the columns, the standard

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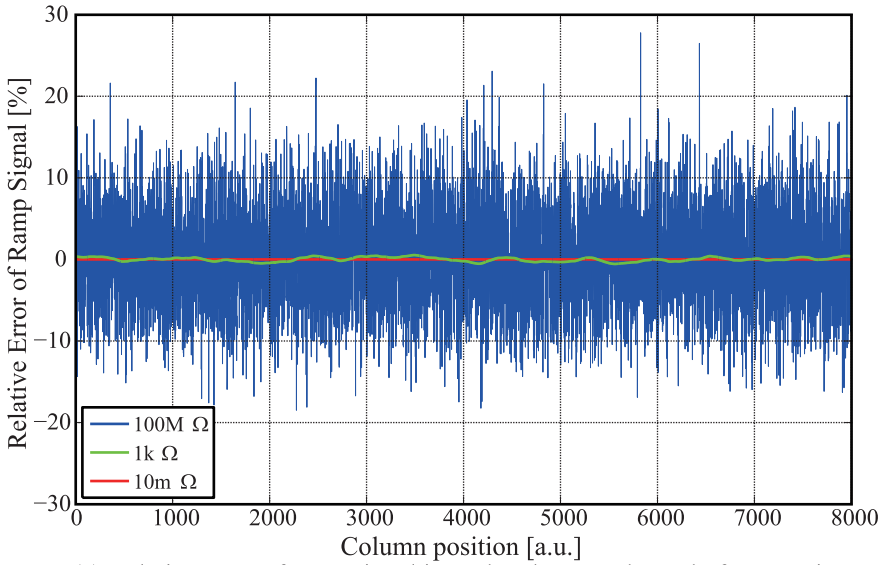
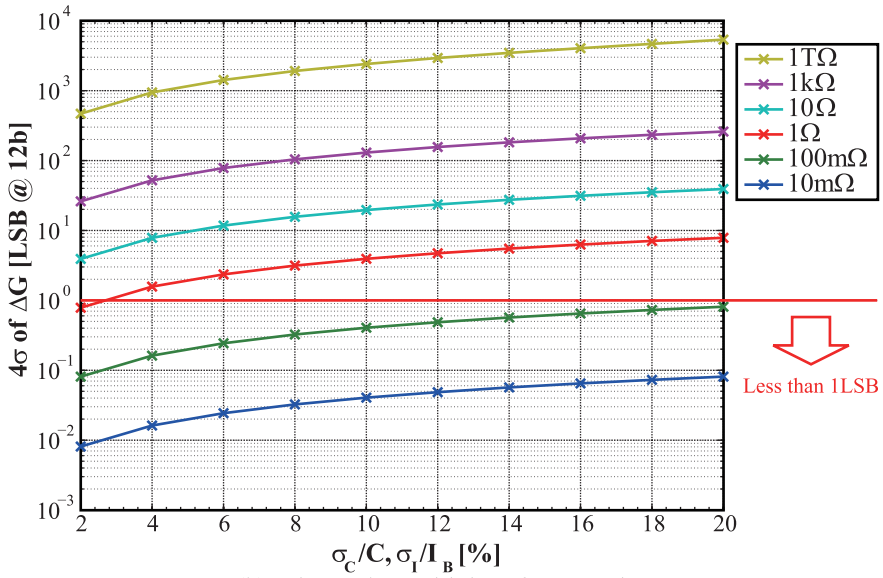


(a) Relative error of ramp signal in each column at the end of conversion (σ_C/C and σ_I/I_B are 5%)



(b) Mismatch sensitivity of ramp gain error

Fig. 3. Mismatch simulation results for 8000 columns

deviation of ΔG in each ADC is an index to evaluate the column-parallel ADC. Therefore 4σ of ΔG is calculated because the probability of taking outside of 4σ is 0.0063% which corresponds to less than 1 column out of 8000 columns ($8000 \times 0.0063\% = 0.51$).

As a result, even if 20% of the circuit component mismatches occurs, the available resistive connections of 100 mΩ and 10 mΩ well reduces the error to be less than 1LSB. This low sensitivity to circuit component mismatches allows us to use a small-size capacitance and current source.

5 Conclusion

A distributed ramp signal generator of column-parallel SS-ADCs for ultra-high-definition television CMOS image sensors has been described. This can solve the problem on how to supply the analog ramp signal evenly over all

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the columns by the column implementation of unit ramp signal generators and those interconnections by a same metal wire.

In the proposed architecture, only the digital signal is supplied from the outside of columns instead of the ramp signal itself. As a result, without the power-hungry driver amplifier in the conventional one, high linearity and high uniformity of the ramp signal are maintained, even though several thousands of comparators turn over simultaneously. From the simulation results, the nonlinear error is efficiently reduced to less than 1LSB at 12-bit resolution.

Although the column mismatch due to the variability on semiconductor manufacturing process may occur, the wire interconnection of ramp signal nodes between the columns provides high uniformity, reducing the eventual ramp signal mismatch. Numerical simulation results show that 100 mΩ resistive connection which is attained in 0.11 μm CMOS image sensor process reduces the number of column having more than 1LSB of the gain error to less than one column.

In conclusion, the proposed architecture achieves the consumption current of 6.4 mA and the area of 2.4 mm^2 for the conversion time of 2 μs and 8000 columns, while the conventional one has the consumption current of larger than 0.4 A and the area of 5 mm^2. Therefore in order to realize ultra-high-definition CMOS image sensors with very high pixel rate and lower power consumption, this distributed ramp signal generator for column-parallel single-slope ADCs becomes essential.

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