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# SCR-based ESD protection device with low trigger and high robustness for I/O clamp

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**Abstract:** This paper presents a novel silicon controlled rectifier (SCR)-based ESD protection device with a low trigger voltage and high robustness for I/O clamp. The low trigger voltage is achieved by injecting the trigger current into main SCR. We measured the I-V characteristics, leakage current analysis and ESD robustness characteristics. The proposed ESD protection circuit was validated using a transmission line pulse (TLP) system. From the experimental results, the proposed ESD protection device has a lower trigger voltage of 5.6 V. Also, the robustness has measured to human body model (HBM) 8 kV and machine model (MM) 600 V. The proposed ESD protection device is designed in 0.35 um Bipolar-CMOS-DMOS (BCD) technologies.

**Keywords:** ESD, silicon controlled rectifier (SCR)
**Classification:** Electron devices, circuits, and systems

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## 1 Introduction

Electrostatic Discharge (ESD) is one of the most important reliability issues in CMOS integrated circuit (IC) products [1]. As technology scales down, the ESD phenomenon has become a greater threat for deep-sub-micron ICs, due to their thinner gate oxide and shallow junction depths. The grounded-gate NMOS (GGNMOS) method is the most commonly used ESD protection structure because of its active discharge mechanism and compatibility to CMOS technologies. However, the GGNMOS needs a relatively large silicon area due to the low current passing capability. Therefore, significant parasitic effects are present, which makes GGNMOS devices the non-optimum solution for high-ESD robustness, high frequency, large pin count, and area-sensitive IC chips [2, 3].

Silicon controlled rectifiers (SCR) have been frequently used as on-chip ESD protection devices for superior ESD robustness and low on resistance. Also, the ESD performance of a SCR provides an area gain factor typically over a MOS-based protection structure. Certainly, the first breakdown voltage of an ESD protection structure for an I/O clamp should be less than the breakdown voltage of the gate oxide. However, a SCR has a relatively high triggering voltage (about 20 V) and its inherent positive feedback mechanism leads to strong snapback characteristics with a small holding voltage [4]. It is hard to effectively discharge an ESD current before malfunction of core circuit occurs and the destruction of gate oxide transpires. Some SCR-based devices (LVTSCR, GGSCR, etc) with low triggering voltages have been proposed. But, the trigger voltage of modified SCR is still high about 10 V.

In this paper, we propose an ESD protection device with trigger technique for SCR based on BCD process.

## 2 Proposed ESD protection device

Fig. 1 shows a cross-sectional view of the proposed ESD protection device. This device is made by adding the low voltage trigger SCR (LVTSCR) structure and p+ trigger node on the conventional SCR with a n+ bridge diffusion across the n/p-well junction. The LVTSCR is formed on the right-hand side of the device to reduce trigger voltage and to generate the trigger current. The p+ tab is formed at the center of the conventional SCR and connected to the cathode of LVTSCR. The p+ tab provides the p-well on the left-hand side of the device with the self-trigger current generated by LVTSCR. Also, the n+ tab on the left-hand side of the conventional SCR provides the trigger current to the right-hand side of p-well diffusion area.

Under normal operating conditions, the LVTSCR is in the off state and thus the main SCR is not operating as an ESD protection device. This is because the breakdown voltage of the main SCR is higher than the supply voltage. Therefore, the ESD protection device does not have an effect on the internal core circuit. When positive ESD surge is applied to the I/O pin, on the other hand, the LVTSCR of low trigger voltage compared to the main SCR, has an avalanche breakdown and the LVTSCR is turned on. And then,


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the generated current by avalanche breakdown is injected to the left-hand side of p-well on main SCR. As a result of this trigger current injection, the potential barrier is lower and thus the trigger voltage of main SCR decreases.

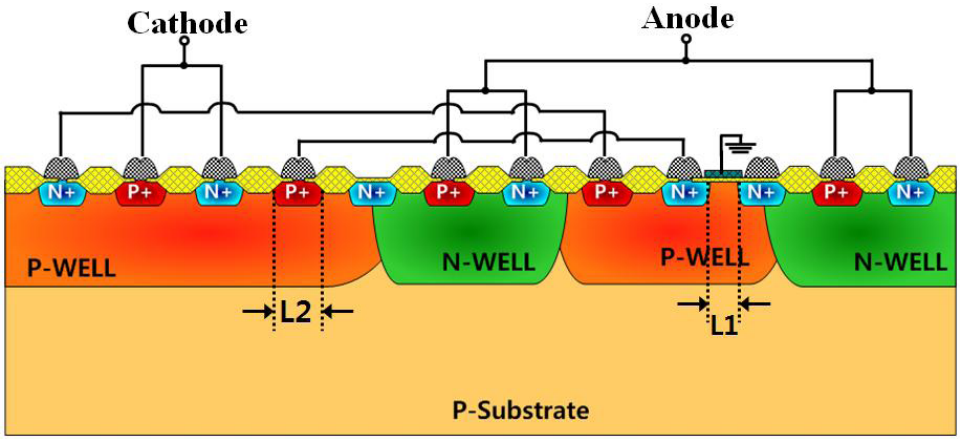


**Fig. 1.** The cross-sectional view of the proposed ESD protection device

## 3 Experimental results

### 3.1 TLP and leakage measurements

The proposed device was fabricated using the 0.35 um BCD process. It was verified using a transmission line pulse (TLP) system with a rise time of 10 ns and pulse width of 100 ns and Synopsys TCAD simulator. The LVTSCR were designed with the 0.8 um gate length and a width of 60 um width of proposed device.

The TLP is typically presented as a plot of the current versus the voltage showing a parameter, such as the turn-on point (Vt1, It1) of the snapback protection structure. Other parameters, such as the on-resistance, can also be easily found in the TLP I-V curve [5]. Fig. 2 (a) shows the DC-IV curves of the conventional GGNMOS and the proposed device are compared. From the simulation result, the trigger voltage of proposed device (4.6 V) was lower than conventional GGNMOS (7.8 V). Fig. 2 (b) shows a TLP I-V curve of the proposed ESD protection device. Due to the trigger current of LVTSCR, the trigger voltage of the main SCR in our proposed device has low trigger voltage of 5.6 V.

We have considered a channel length (L1) range of 0.8-1.4 um, and the TLP results of proposed devices are shown in Fig. 3 (a). This is due to the fact the channel length is the base thickness of the parasitic bipolar transistor in SCR, which controls the triggering of LVTSCR. Also, Fig. 3 (c) shows a TLP I-V curve of L2 length and the p+ active length (L2) is only related to the second triggering current. The second triggering current increases when L2 increases from 2.3 um to 6.7 um. This is because the p+ tab reduces the p-well resistance, then the trigger current needs more to turn parasitic npn bipolar in SCR.


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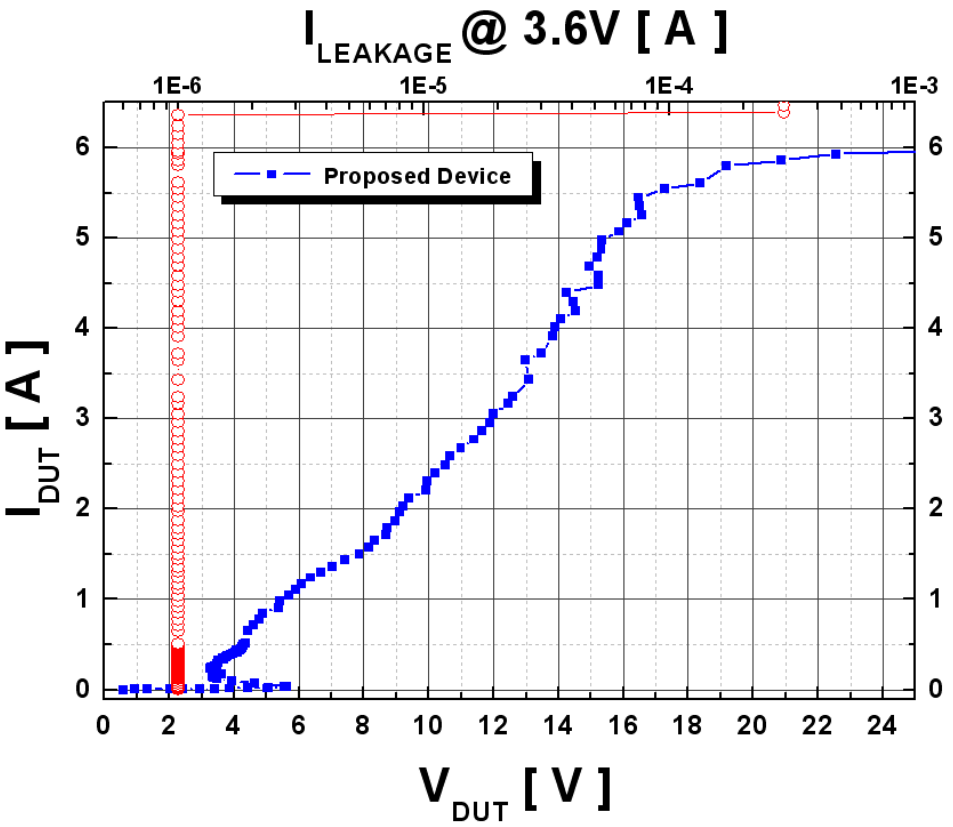
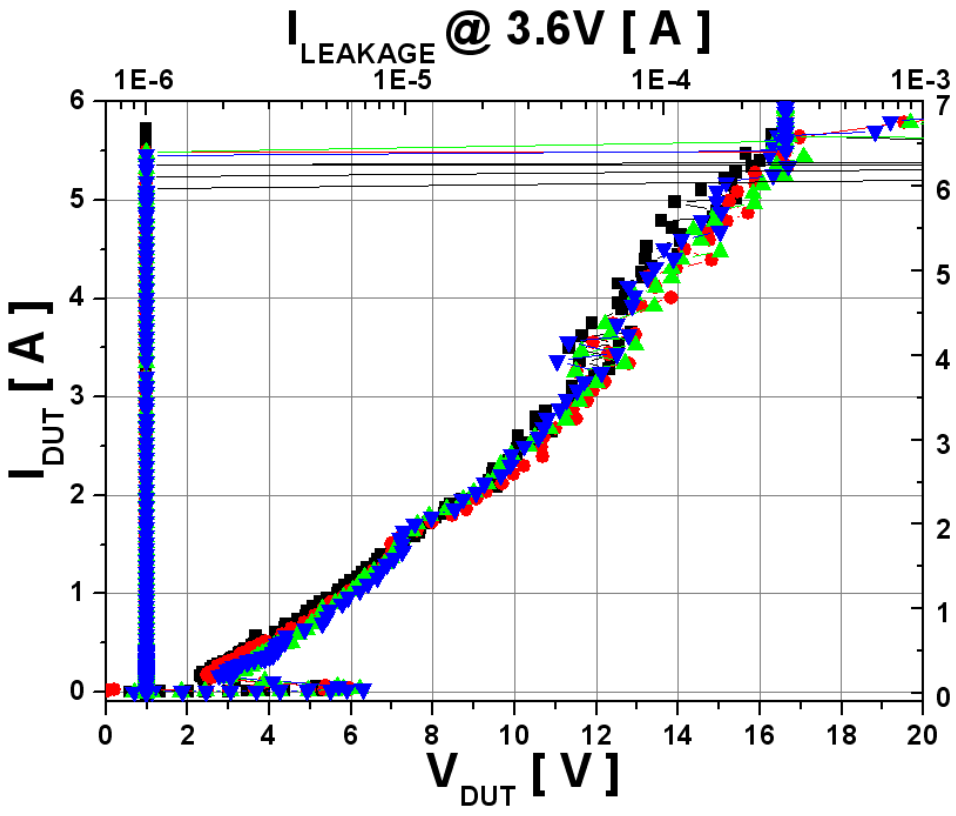



**Fig. 2.** TLP I-V curve of the proposed ESD protection device




(a)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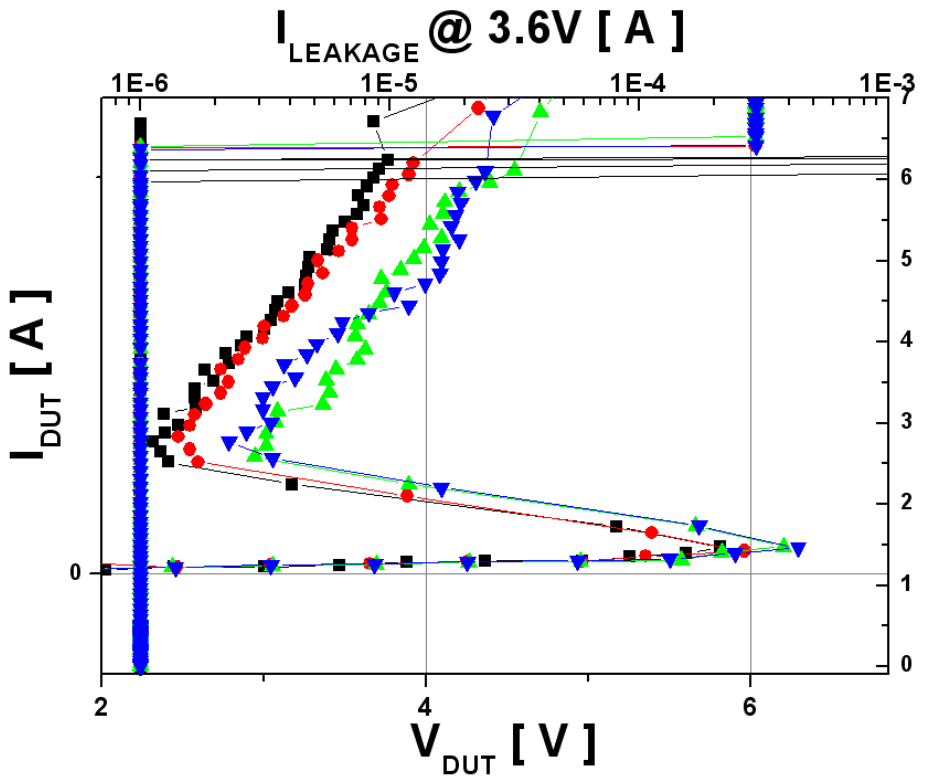
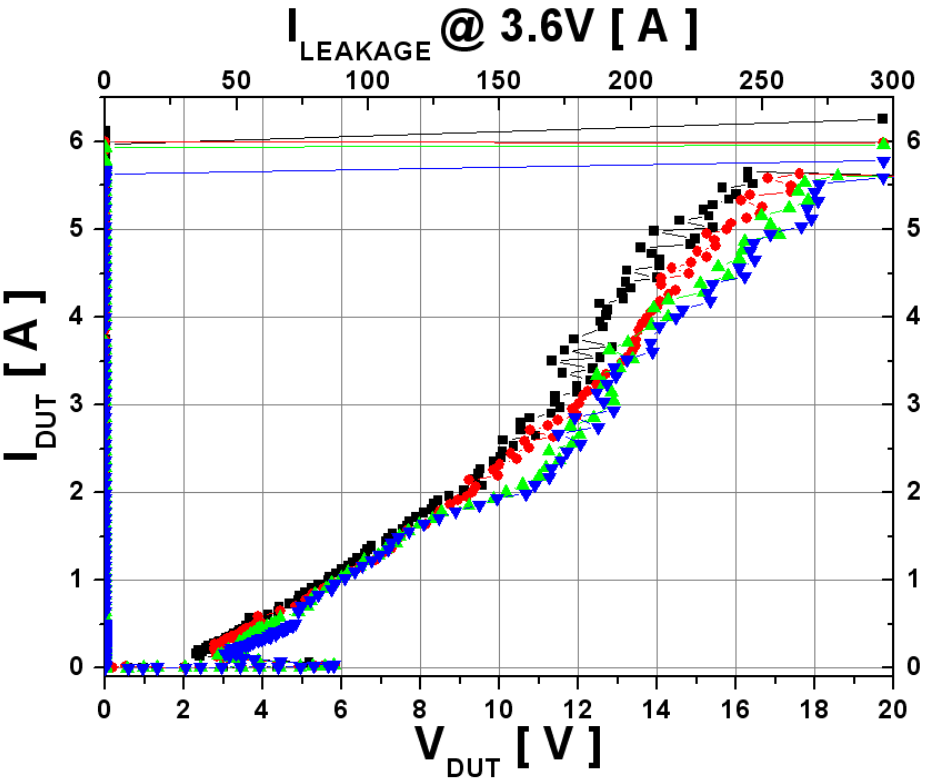



(b)




(c)

**Fig. 3.** TLP I-V characteristics of proposed device with different design parameters (a) L1 variation, (b) enlarge a trigger voltage of L1 variation, (c) L2 variation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### 3.2 ESD robustness (HBM test)

In order to evaluate the effectiveness of the protection in an integrated circuit, human body model (HBM) testing is performed. The HBM test is measured by the ESS-6008 ESD simulator. The proposed device is designed with a 60 um width. The target of the proposed device was an 8-kV HBM and MM 600 V of ESD robustness. Due to the operating 2-SCR, the proposed device has high robustness.

## 4 Conclusion

In this paper, the proposed ESD protection device using the 0.35 um BCD process has been investigated. The proposed device, with a trigger voltage of 5.6 V, is for 1.8 V and 3.3 V I/O applications. Compared to the conventional GGNMOS, the proposed ESD protection device has a lower trigger voltage. In addition, the robustness of the proposed ESD protection device exceeds 6-kV. From the experimental results, the trigger voltage of the proposed ESD protection device was reduced by about 30%, compared to the conventional GGNMOS, which enables an effectively discharge for low voltage domain I/O clamp.

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