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A new curvature-corrected CMOS bandgap voltage reference

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Abstract: The current paper presents an improved bandgap voltage reference (BGR) that utilizes curvature-corrected current generators which compensate for the voltage reference at lower and higher temperature range. The voltage reference is operated with a supply voltage of 2.5 V to achieve an output reference of 1.1835 V. The temperature coefficient achieved from the circuit is 1.342 ppm/°C, resulting from temperature changes between −50°C to 125°C, sixfold improvement from first-order BGR. The proposed circuit is simulated using Silterra 0.13 μm CMOS technology.

Keywords: CMOS bandgap reference, low variation
Classification: Integrated circuits

References

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1 Introduction

The performance of most circuit blocks is connected to that of the voltage references used to bias and power them. A first-order bandgap reference adds the forward-bias voltage across the p-n diode, and that voltage is weighted by adjusting the ratio of two resistors [1]. The voltage across the p-n diode is

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expressed as the sum of a constant term, a term proportional to temperature and a nonlinear term clearly explained in [2]. The variation of the nonlinear term with respect to temperature reported in [2] is 4.5 mV for the temperature between −50°C to 150°C. A few works reported on curvature-corrected BGR are presented in [3, 4]. Although these circuits have been proven to lower the voltage variation, the variation only ranges from 0°C to 125°C. In the current work, the variation of the nonlinear term is decreased through the inclusion of curvature-corrected current generators that compensate for the voltage reference at lower and higher temperature.

2 Proposed design

The operation of the proposed design is shown in Fig. 1. The first-order BGR produces an output given as

$$V_{REF} = K_1 V_T ln(n) + V_{EB}, \tag{1}$$

where K_1 is the temperature indepencent coefficient, V_T is the thermal voltage, and n is the emiter area ratio of BJT.

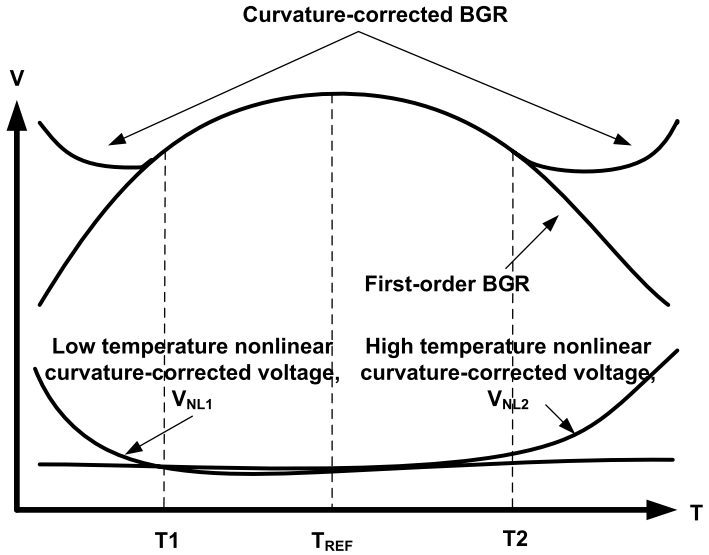

Fig. 1. Curvature-corrected BGR.

To compensate the nonlinearity of the first-order BGR, the nonlinear curvature-corrected voltages, V_{NL1} and V_{NL2}, are added. As a result, a curvature-corrected BGR is obtained, as graphically shown in Fig. 1. The proposed BGR consists of first-order BGR, current generators, G_A and G_B, and a startup circuit, as illustrated in Fig. 2 (a).

The output of the first-order BGR is expressed as follows:

$$V_{ref} = \frac{R_2 + R_3}{R_1} V_T ln(n) + V_{EB3}, \tag{2}$$

where n is the emitter area ratio of Q_2. The proposed current generator G_A is illustrated in Fig. 2 (b). The current I_{PTAT1} flowing through the resistor

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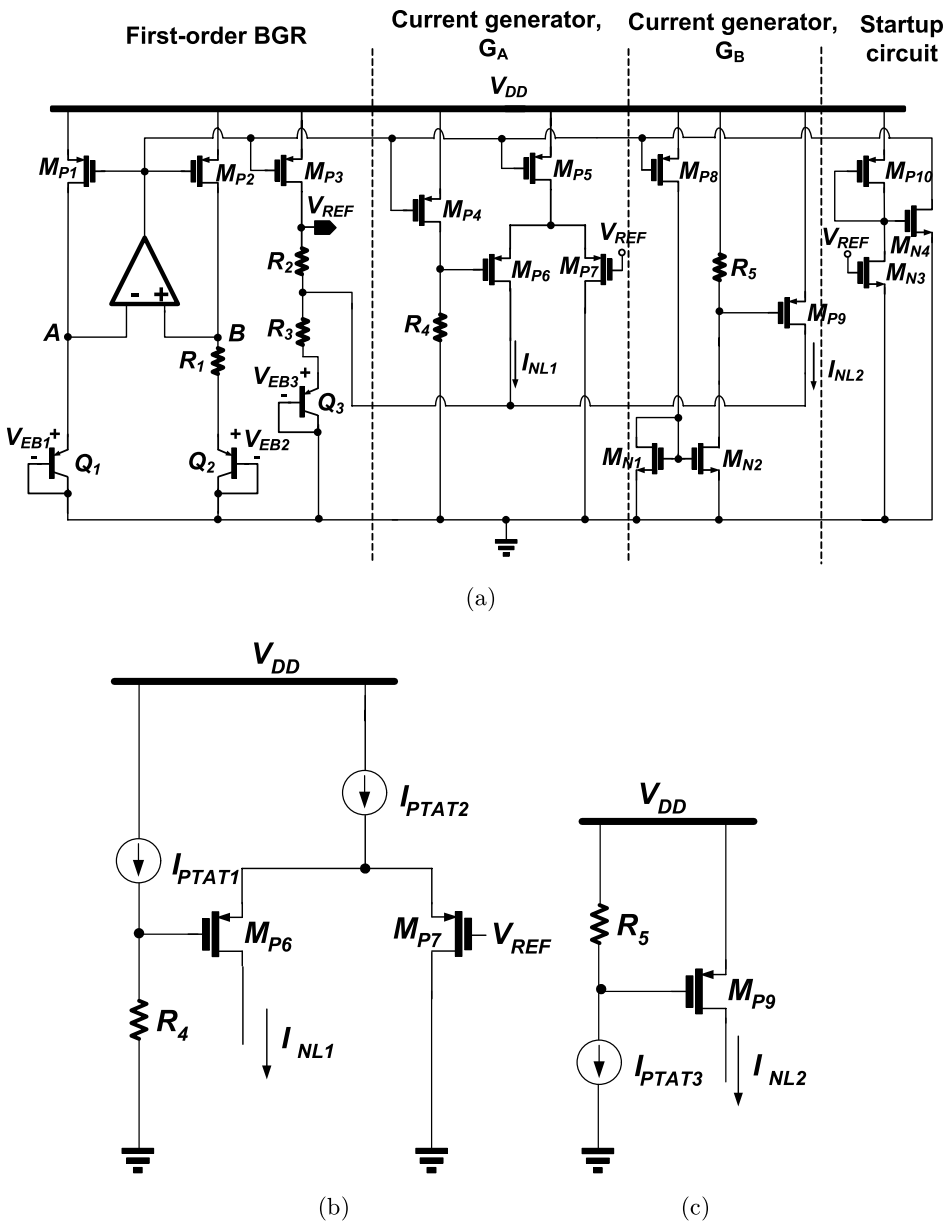

Fig. 2. (a) Proposed BGR, (b) Current generator, G_A, and (c) Current generator, G_B.

R_4 produces a PTAT voltage given as

$$V_{GMP6} = R_4 I_{PTAT1}, \tag{3}$$

where

$$I_{PTAT1} = \alpha \frac{V_T ln(n)}{R_1}. \tag{4}$$

Parameter α is the ratio of the size of M_{P4} to M_{P2}. The size of M_{P7} is larger than M_{P6} to reduce the variation of the source voltage M_{P6} and M_{P7}. At temperature below T_{REF}, when the voltage V_{SGMP6} is much larger than its threshold voltage, M_{P6} is operating in the saturation region. By further increasing the temperature, M_{P6} will no longer be in the saturation region; it starts operating in the weak inversion region.

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When V_{SGMP6} is much lower than its threshold voltage, the transistor M_{P6} will be completely cut off and there will be no current flowing through M_{P6}. The operation of the proposed circuit by [4] is illustrated in Fig. 2 (c). It works similar to the circuit of Fig. 2 (b), but it produces current I_{NL2} at high tempearature only. The voltage at gate terminal of M_{P9} is given by

$$V_{GMP9} = VDD - R_5 I_{PTAT3}, \tag{5}$$

where

$$I_{PTAT3} = \frac{\gamma V_T ln(n)}{R_1}. \tag{6}$$

Parameter γ is the ratio of the size of M_{P8} to M_{P2}. The gate-source voltage of transistor M_{P9} is insensitive to power supply variation expressed as follows

$$V_{SGMP9} = \frac{R_5 V_T ln(n)}{R_1}. \tag{7}$$

Currents I_{NL1} and I_{NL2} run through R_3. As a result, the corrected voltages V_{NL1} and V_{NL2} are generated. The addition of the corrected voltages with the output voltage produced by the first-order BGR expresses the following equation:

$$V_{REF} = \frac{R_2 + R_3}{R_1} V_T ln(n) + V_{EB3} + (I_{NL1} + I_{NL2}) R_3. \tag{8}$$

The corrected voltages are given by the third term of Eq. (8). It efficiently compensates the voltage variation, thereby keeping the output voltage of V_{REF} from changing with the change in temperature.

3 Simulation results

The proposed BGR shown in Fig. 2 (a) is carried out in a standard 0.13 μm CMOS process. Figure 3 shows the variation of voltage reference within the temperature range -50°C to 125°C. The voltage variation is only 0.278 mV for the proposed BGR, sixfold improvement from 1.714 mV for the first-order BGR. The curvature-corrected currents I_{NL1} and I_{NL2} are also shown in Fig. 3. When the temperature is less than 20°C, the nonlinear-corrected current I_{NL1} is increasing while I_{NL2} is completely cut off. By contrast, the current I_{NL2} starts increasing, whereas the current generator G_A is in off state when the temperature is greater than 20°C. The maximum currents of I_{NL1} and I_{NL2} are 450 and 250 nA, respectively.

4 Conclusion

A BGR with very low voltage variation has been presented. The proposed design produces an output voltage reference of 1.1835 V over a temperature range of -50°C to 125°C. The temperature coefficient achieved from the circuit is 1.342 ppm/°C, whereas the temperature coefficient of 8.276 ppm/°C is obtained for the first-order BGR.

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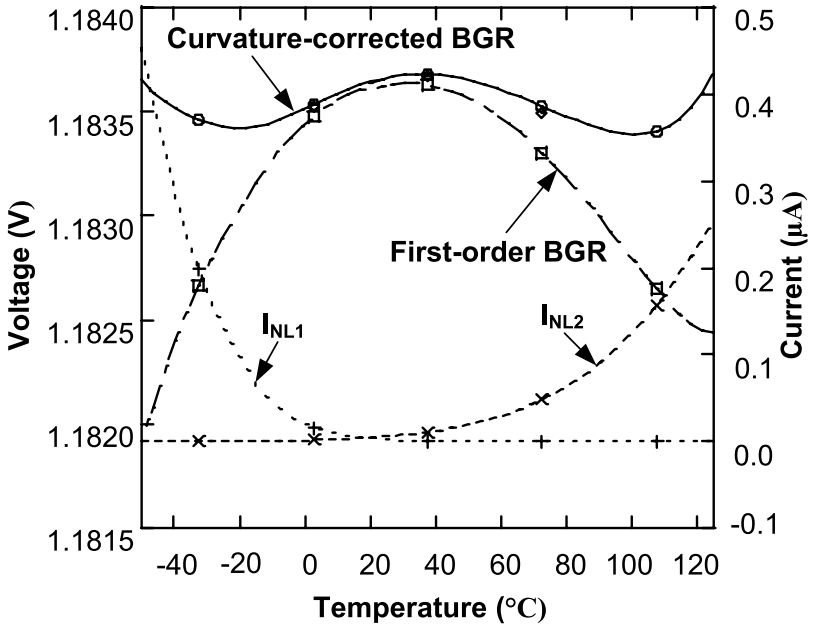

Fig. 3. Voltage reference and nonlinear current.

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