

# A 3.5 mW 5 $\mu$ sec settling time dual-band fractional-N PLL synthesizer

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**Abstract:** We explore a dual-band fractional-N PLL synthesizer with 3.5 mW, 5  $\mu$ sec settling time and 15  $\mu$ sec start-up time in 0.18  $\mu$ m CMOS technology. The power consumption is minimized through the design efforts in LC-VCO design to maximize the quality factor of an integrated inductor up to 6.1 at 866 MHz and minimize the VCO gain by a capacitor tuning technique with an on-chip nonvolatile memory and the proper choice of varactor. Measured results of a prototype fractional-N PLL satisfy the required settling and start-up times, and indicate that the phase noises at 10 kHz and 100 KHz offset are  $-108.7$  dBc/Hz and  $-98.3$  dBc/Hz, respectively, and the reference spurious level is  $-81.6$  dBc.

**Keywords:** phase locked loop, low power design, voltage controlled oscillator

**Classification:** Integrated circuits

## References

- [1] J.-G. Lee and S. Masui, "Loop design optimization of 4th-order fractional-N PLL frequency synthesizers," *Proc. IEEEJ Analog VLSI Workshop*, Bali, Indonesia, pp. 139–144, Nov. 2011.
- [2] Z. Xu, J.-G. Lee, and S. Masui, "Self-dithered digital delta-sigma modulators for fractional-N PLL," *IEICE Trans. Electron.*, vol. E94-C, no. 6, pp. 1065–1068, June 2011.
- [3] B. De Muer and M. Steyaert, *CMOS Fractional-N Synthesizers*, Kluwer Academic Publishers, Dordrecht, Netherlands, 2003.
- [4] C. P. Yue and S. Wang, "Physical modeling of spiral inductors on silicon," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 560–568, March 2000.
- [5] W.-Z. Chen and W.-H. Chen, "Symmetric 3D passive components for RF ICs application," *Proc. Radio Frequency Integrated Circuits Symposium*, Philadelphia, U.S.A., pp. 599–602, June 2003.
- [6] J.-G. Lee and S. Masui, "Design and optimization of program and restore operations in CMOS-compatible nonvolatile latch," *Extended Abstracts of International Conf. Solid State Devices and Materials*, Nagoya, Japan, pp. 156–157, Sept. 2011.
- [7] X. Kuang and N. Wu, "A fast-settling PLL frequency synthesizer with direct frequency presetting," *ISSCC Dig. Tech. Papers*, San Francisco, U.S.A., pp. 204–205, Feb. 2006.

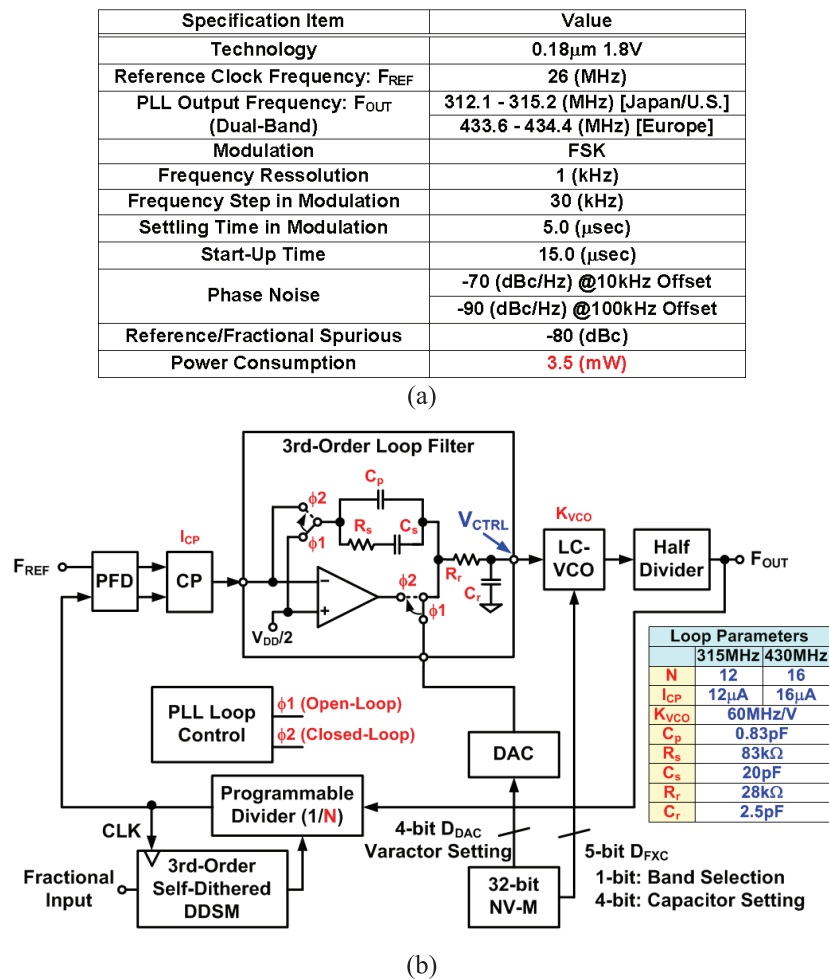
- [8] K. Woo, Y. Liu, E. Nam, and N. Wu, “Fast-lock hybrid PLL combining fractional-N and integer modes of differing bandwidth,” *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 379–389, Feb. 2008.

## 1 Introduction

We propose a dual-band fractional-N PLL (phase locked loop) synthesizer featuring 3.5 mW, 5  $\mu$ sec settling-time, and 15  $\mu$ sec start-up time in a 0.18  $\mu$ m CMOS for short-range communication transceivers applicable to smart-key systems. The specification and block diagram of the proposed 4th-order fractional-N PLL are shown in Fig. 1 (a), and Fig. 1 (b), respectively. The operation bands are 312.1–315.5 MHz (315 MHz band) used in Japan/U.S. and 433.6–434.4 MHz (433 MHz band) used in Europe. The power consumption of 3.5 mW is achieved by elaborations of VCO (voltage controlled oscillator) design as is described in the next section. In Fig. 1 (b), PFD, CP, DAC, DDSM, and NV-M represent phase frequency detector, charge pump, digital-to-analog converter, digital delta sigma modulator, and nonvolatile memory, respectively.

To maximize the data rate in FSK modulation, settling time of the proposed PLL is designed as 5  $\mu$ sec. The parameters that dominate the settling time are programmable divider ratio  $N$ , charge pump current  $I_{CP}$ , VCO gain  $K_{VCO}$ , and loop filter passive components,  $C_p$ ,  $R_s$ ,  $C_s$ ,  $R_r$ , and  $C_r$ . These parameter values are optimized from the constraints of settling time, phase noise and area by taking into account of process, voltage and temperature variations in the passive components, and obtained values are summarized in Fig. 1 (b) [1]. To accommodate to the dual-band operation and maintain the identical PLL crossover frequency for each operation band, only  $I_{CP}$  is scaled according to the change of  $N$ . Such design can remove influences by the change of passive components. The start-up time of 15  $\mu$ sec is achieved with an open-loop calibration method featuring VCO capacitor coarse setting, and  $V_{CTRL}$  setting with the NV-M in order to eliminate the frequency detection and VCO coarse tuning sequences used in conventional start-up acceleration techniques. In the VCO capacitor coarse setting, the predetermined setting code,  $D_{FXC}$ , is provided from the NV-M to the VCO capacitors, and in the subsequent  $V_{CTRL}$  setting, an optimized  $V_{CTRL}$  is supplied from the DAC and associated varactor setting code,  $D_{DAC}$ , stored in the NV-M. The PLL loop control circuit generates a non-overlapping clock  $\phi_1$ , representing open-loop status, to provide calibration codes to the capacitors and varactors in LC-VCO, and  $\phi_2$ , representing closed-loop status, to synthesize the PLL output. A 3rd-order self-dithered DDSM is employed to reduce the fractional spurious below  $-80$  dBc [2]. This DDSM demands 3rd-order loop filter, as shown in Fig. 1 (b), to filter out the shaped quantization noise.

In the following sections, the low-power design of the fractional-N PLL and its experimental results are presented.

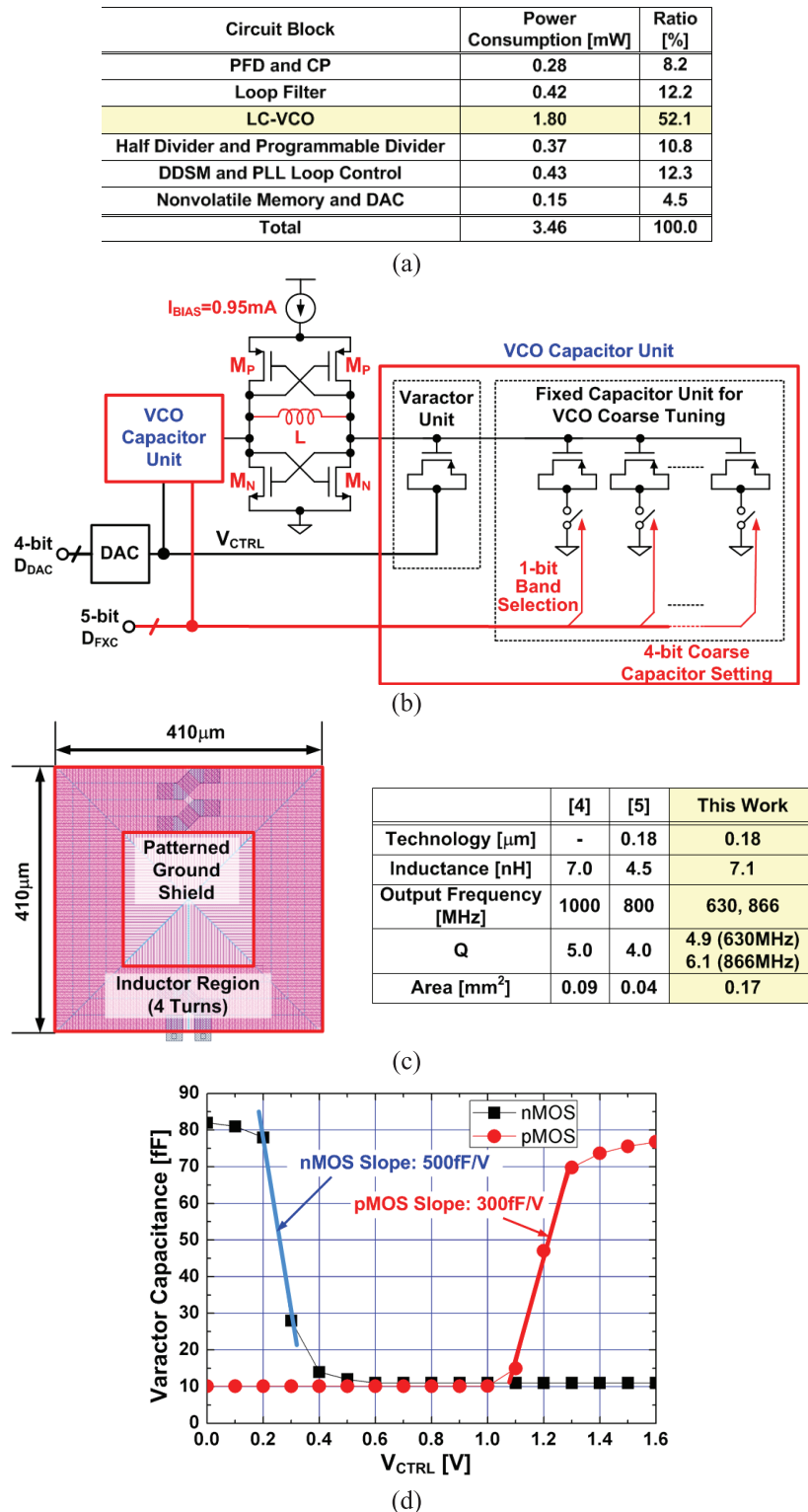


**Fig. 1.** Specification and architecture of the proposed fractional-N PLL synthesizer (a) Specification for short-range communication transceiver, (b) Architecture and circuit parameters of the proposed fractional-N PLL.

## 2 Low-power fractional-N PLL design

The power consumption in each block of the proposed fractional-N PLL designed in a 0.18  $\mu$ m CMOS is summarized in Fig. 2(a). Since over 52% of total power is consumed in the LC-VCO, the low-power VCO design by taking account of its phase noise becomes critical. The schematic diagram of the employed LC-VCO is shown in Fig. 2(b). To minimize the phase noise for a given bias current  $I_{BIAS}$  of 0.95 mA, quality factor  $Q$  of the inductor  $L$  should be maximized [3] and  $K_{VCO}$  should be minimized through the optimization of capacitors and varactors.

The layout of the employed inductor with a patterned ground shield as well as its characteristics compared with those of other inductors designed for the VCO output frequency around 1 GHz are shown in Fig. 2(c). It should be noted that the PLL output frequency is designed as a half of the VCO output frequency to reduce the phase noise.  $Q$  values of the designed inductor are higher than other results due to the increased size (410  $\mu$ m  $\times$  410  $\mu$ m)



**Fig. 2.** Low-power fractional-N PLL design (a) Power consumption in each block of the proposed PLL, (b) Schematic diagram of the proposed LC-VCO, (c) Layout of on-chip inductor and comparison of inductor characteristics, (d) C-V characteristics of nMOS and pMOS transistors for varactor application.

and line width ( $25\text{ }\mu\text{m}$ ) for a given 5th Al-metal layer. To minimize the VCO gain, the fixed-capacitor unit, whose value is controlled by  $D_{\text{FXC}}$  with 1-bit band selection code and 4-bit capacitor coarse setting code, is added to the varactors as shown in Fig. 2 (b). Furthermore, pMOS capacitors and varactors are employed in the LC-VCO. Fig. 2 (d) presents simulated C-V characteristics for nMOS and pMOS transistors available to varactors in a given technology. Since the slope of the C-V characteristic is smaller in pMOS, its relative change of VCO output frequency over  $V_{\text{CTRL}}$ , equivalent to  $K_{\text{VCO}}$ , becomes smaller than that of nMOS.

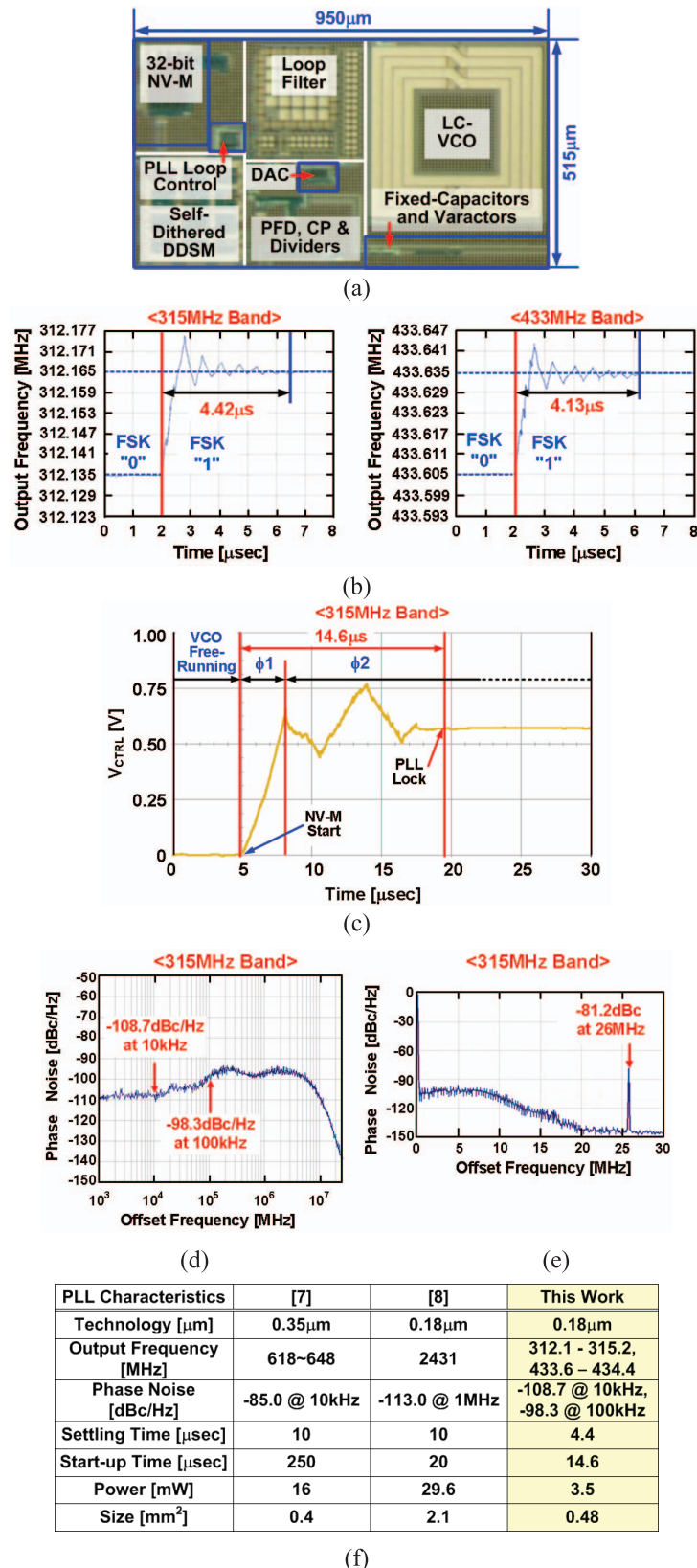
As shown in Fig. 2 (b), CMOS topology is used for the LC-VCO to increase the oscillation amplitude in the current-limited operation mode provided from  $I_{\text{BIAS}}$  of  $0.95\text{ mA}$  [3]. Total transconductance  $G_{\text{M}}$  necessary for the oscillation of  $630\text{ MHz}$  is calculated as  $21\text{ mS}$ , and 60% of  $G_{\text{M}}$  is supplied from nMOS transistors,  $M_{\text{N}}$ , and the rest of  $G_{\text{M}}$  is from pMOS transistors,  $M_{\text{P}}$ , to reduce the parasitic drain-to-bulk capacitance. Since the required  $G_{\text{M}}$  for  $866\text{ MHz}$  is  $17\text{ mS}$ , the identical LC-VCO structure can reduce the phase noise for  $433\text{ HHz}$  band. The simulated phase noises of the designed LC-VCO are  $-90.7\text{ dBc/Hz}$  at  $10\text{ kHz}$  offset, and  $-117.6\text{ dBc/Hz}$  at  $100\text{ kHz}$  offset for  $630\text{ MHz}$ , and  $-92.1\text{ dBc/Hz}$  at  $10\text{ kHz}$  offset, and  $-118.9\text{ dBc/Hz}$  at  $100\text{ kHz}$  offset for  $866\text{ MHz}$ . The phase noise of the PLL can be attenuated to the insignificant level by the loop filter [1]. The worst-case figures of merit of the designed LC-VCO have reasonable values of  $184.1$  and  $188.3$  for  $630\text{ MHz}$  and  $866\text{ MHz}$ , respectively [3].

As is described in this section, the low-power design of the proposed PLL is achieved by the elaboration of LC-VCO design in terms of the inductor Q enhancement and  $K_{\text{VCO}}$  minimization techniques with capacitor tuning with a NV-M and a proper choice of varactor.

### 3 Experimental results

The proposed fractional-N PLL is fabricated in a  $0.18\text{ }\mu\text{m}$   $1.8\text{ V}$  standard CMOS technology. The die micrograph is presented in Fig. 3 (a), where the die size is  $950\text{ }\mu\text{m} \times 515\text{ }\mu\text{m}$ , and a 32-bit 16-program-cycle NV-M with a 2-transistor memory cell utilizing a hot-electron trapping at the sidewall of memory transistor stores  $D_{\text{FXC}}$  and  $D_{\text{DAC}}$  [6]. Fig. 3 (b) indicates the measured transient waveforms of FSK modulation, and obtained settling times are  $4.42\text{ }\mu\text{sec}$  and  $4.13\text{ }\mu\text{sec}$  for  $315\text{ MHz}$  and  $433\text{ MHz}$  band, respectively. The measured  $V_{\text{CTRL}}$  waveform in the PLL start-up sequence for  $315\text{ MHz}$  band is presented in Fig. 3 (c), and the start-up time is derived as  $14.6\text{ }\mu\text{sec}$  by observing the PLL output frequency rather than this  $V_{\text{CTRL}}$ . The start-up time for  $433\text{ MHz}$  is typically higher than that of  $315\text{ MHz}$  due to the fast settling as shown in Fig. 3 (b).

The measured results of the phase noise and reference spurious level for  $315\text{ MHz}$  band are shown in Fig. 3 (d) and Fig. 3 (e), respectively. The phase noise for  $315\text{ MHz}$  band is worse than that for  $433\text{ MHz}$  band due to the smaller Q in LC-VCO and smaller  $I_{\text{CP}}$  [1]. The phase noises at  $10\text{ kHz}$  and



**Fig. 3.** Experimental results (a) Die micrograph of the proposed PLL, (b) Setting time measurement results for 315 MHz and 433 MHz band, (c) Start-up time measurement for 315 MHz band, (d) Phase noise measurement for 315 MHz band, (e) Reference spurious level measurement for 315 MHz band, (f) Comparison of PLL characteristics.



100 KHz offset for 315 MHz band are  $-108.7$  dBc/Hz and  $-98.3$  dBc/Hz, respectively, and the obtained spectrum well corresponds to the calculated result [1]. From the analysis it is clarified that for the offset frequencies below 10 kHz the contribution from CP is dominant to the entire phase noise, and over 1 MHz that from DDSM becomes most significant, while between these frequencies, the contribution from the OTA in the loop filter dominates. The reference spurious level observed at 26 MHz offset is  $-81.6$  dBc, and remarkable fractional spurious tones are not observed.

Fig. 3 (f) compares characteristics of the proposed and published PLLs for low-power and fast settling/start-up applications. The proposed fractional-N PLL overwhelms other PLLs in terms of the settling time, start-up time and power consumption with comparable phase noise results.

#### 4 Conclusion

A 3.5 mW fractional-N PLL synthesizer with 5  $\mu$ sec settling time and 15  $\mu$ sec start-up time is successfully developed by the elaboration of LC-VCO, optimized loop design methodology and the open-loop calibration method featuring the VCO capacitor coarse setting and subsequent  $V_{CTRL}$  setting enabled by an on-chip nonvolatile memory. A prototype fractional-N PLL fabricated in a standard 0.18  $\mu$ m CMOS technology satisfies the required phase noise and reference spurious level.

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