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A novel RC time constant tuning technique utilizing programmable current sources for continuous-time delta-sigma modulators

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Abstract: A novel RC time constant tuning technique for continuous-time delta-sigma modulators is proposed to alleviate the systematic time constant shift originating from process variations. The proposed tuning technique uses programmable current sources instead of capacitor banks in order to reduce the implemented die area. MATLAB/Simulink simulation results demonstrate that this technique can achieve the desired SQNR even with ±30% RC time constant shifts.

Keywords: continuous-time delta-sigma modulator, RC time constant tuning

Classification: Integrated circuits

References

[1] S. Yan and E. Sánchez-Sinencio, "A Continuous-Time ΣΔ Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, Jan. 2004.

[2] A. Hastings, *The Art of Analog Layout*, ch. 7, Prentice Hall, 2006.

[3] S. Pavan and N. Krishnapura, "Automatic Tuning of Time Constants in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, pp. 308–312, April 2007.

[4] R. Schreier and G. C. Temes, *Understanding Delta Sigma Data Converters*, ch. 9, John Wiley & Sons, 2005.

[5] B. Xia, S. Yan, and E. Sánchez-Sinencio, "An RC Time Constant Auto-Tuning Structure for High Linearity Continuous-Time ΣΔ Modulators and Active Filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 11, pp. 2179–2188, Nov. 2004.

[6] R. Schreier, The Delta-Sigma toolbox for MATLAB. [Online] http://www.mathworks.com/matlabcentral/fileexchange

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1 Introduction

The implementation of continuous-time delta-sigma modulators (CTDSMs) became popular in the mid-1990s because CTDSMs exhibit better power efficiency and can realize very high sampling rates. However, CTDSMs that incorporate continuous-time integrators [1] suffer from process-dependent RC time constant variation. Current CMOS technology has large process variations, which could result in a systematic RC time constant shift of up to $\pm 30\%$ [2] in a chip. Thus, a tuning circuit is essential in order for CTDSMs to realize the desired performance [3]. However widely used conventional tuning techniques using capacitor banks [1] are not perfectly suitable for active-RC integrators in CTDSMs, because the capacitor banks tend to require large area. In this paper, we propose a novel RC time constant tuning technique for an active-RC integrator that uses programmable current sources instead of capacitor banks in order to reduce the implemented die area.

2 Proposed tuning technique

2.1 Basic concept of the proposed tuning technique

Fig. 1 (a) shows a block diagram of the m-th order CTDSM implementing the proposed technique. Coefficients of m-th order DAC and integrator show $k_m\alpha^m$ and $\frac{1}{\tau_m}$, respectively. k_m shows m-th DAC coefficient which is decided by the DAC fullscale current. τ_m indicates RC time constant of m-th integrator. In the proposed technique, a part of DAC coefficient which is a tunable value, α, is used to compensate for the systematic time constant shift. Usually, k_m and τ_m are designed to realize delta-sigma modulator which satisfies desired specifications, and these are fixed values. The change of coefficient α means tuning fullscale current value of DAC.

If the 1st stage's time constant τ_1 shifts to $\tau_1 D$, where the time constant shift ratio D is a chip-dependent value, the block diagram can be redrawn mathematically as shown in Fig. 1 (b). In m-th stage DAC, α^m is utilized in order to suppress $(m-1)$-th stage's input gain modifier, $\frac{1}{D^{m-1}}$, and m-th stage's time constant shift $\frac{1}{D}$. Therefore m-th order CTDSM can be expressed for Fig. 1 (c) from Fig. 1 (a). The time constant shift ratio D changes the feedback DAC coefficients, as well as the input gain from their designed component magnitudes. However the input gain modifier $\frac{1}{D^m}$ can be neglected, because the effect of the modifier is cancelled by commonly used automatic gain control circuit at the front of the analog-to-digital converter. In the proposed technique, the DAC coefficient modifier cancels the systematic time constant shift by tuning $\alpha{=}D$ without the capacitor banks occupying a large die area. Fig. 1 (d) shows a tunable DAC coefficient that uses programmable current sources $I_1 \sim I_N$ connected through switches and a conventional-current DAC [4]. The amount of current is related to fullscale of the DAC and the fullscale value means the coefficient of each DAC. Therefore the coefficient of each DAC can be tuned by using switches in order to provide the appropriate compensation coefficient α^m, which realizes the implementation of the proposed tuning technique on a chip.

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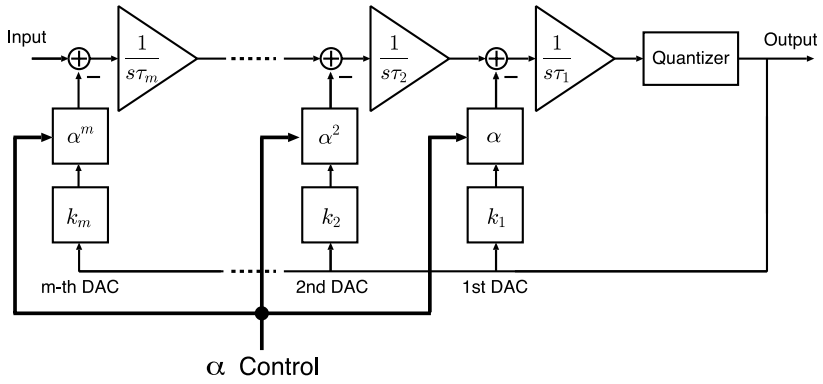
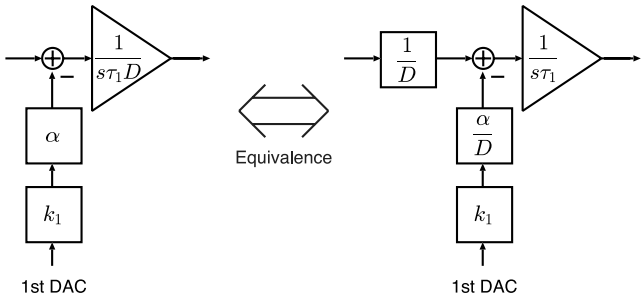
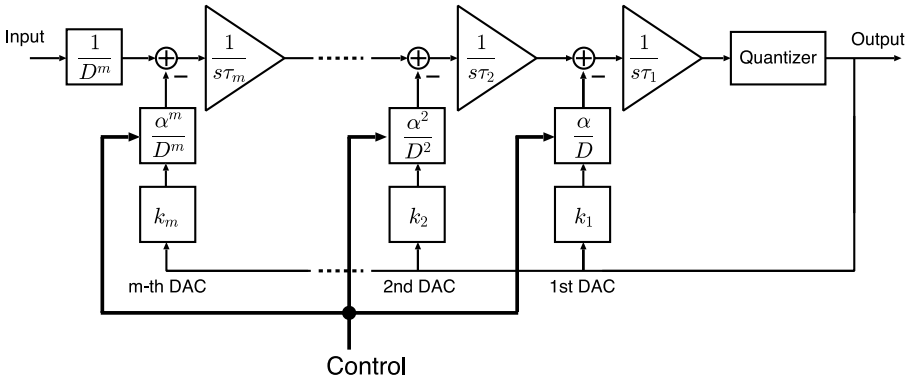


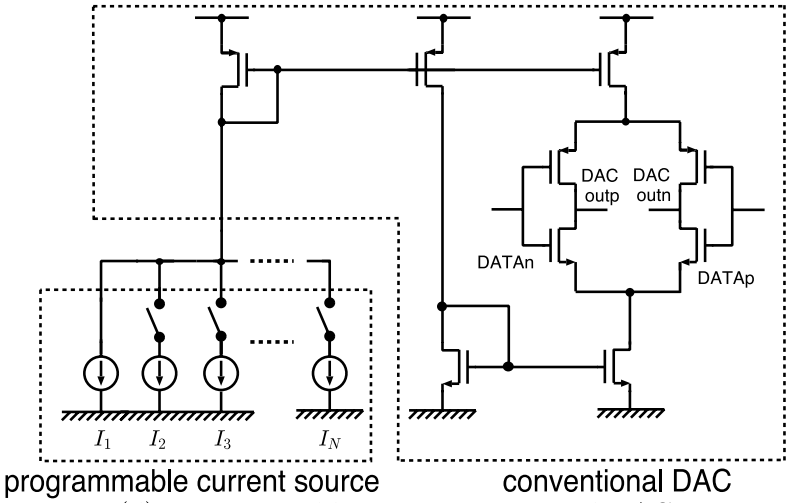
(a) m-th order CTDSM implementing the proposed tuning technique.



(b) Equivalent conversion.



(c) Block diagram including the process shift ratio D.



(d) Programmable current source and DAC.

Fig. 1. Proposed tuning technique

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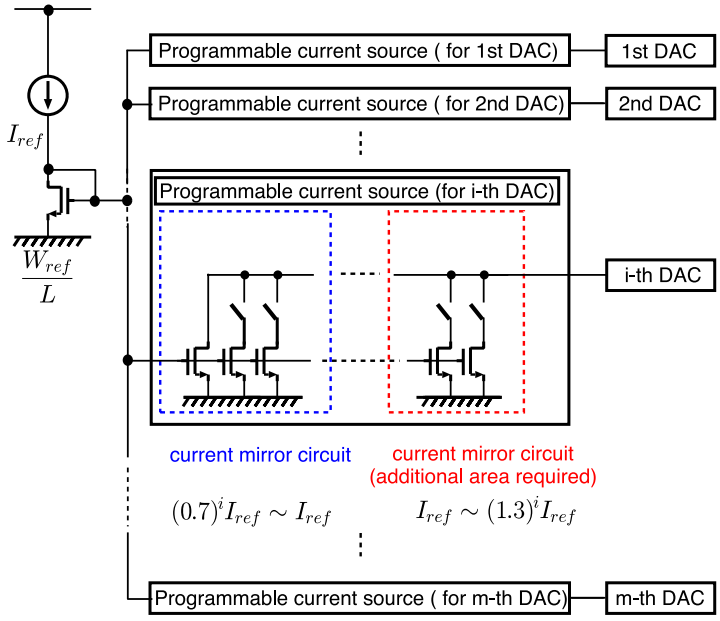
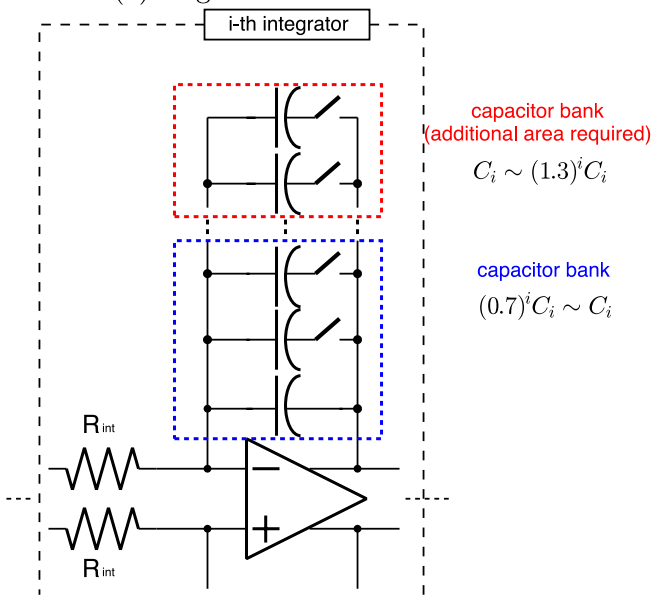
The time constant tuning is only operated during the LSI start up time. At the LSI's power "ON" time, value of time constant shift D is detected by using conventional time constant shift detection circuit (e.g. [5]).

2.2 Die area discussion

First, the occupation area of the programmable current sources is estimated in order to compare with that of the conventional capacitor banks. In this analysis, fixed DAC coefficient values, $k_m = k_{m-1} = \cdots = k_1 = 1$, are assumed. It is reasonable because we prepare only one type reference current and it means that implementation bias circuit can be simply. Fig. 2 (a)



(a)Programmable current sources



(b)Conventional capacitor banks

Fig. 2. Die area discussion (Each red boxed area shows additional area.)

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shows the programmable current sources and a detailed explanation about i-th programmable current source which supplies a feedback current for the i-th DAC. The number of the programmable current sources is the same as the number of the feedback DACs. Required current sources in feedback DAC is based on copying current from a reference current I_{ref}. The left part of Fig. 2 (a) shows diode connected transistor whose drain current is reference current, and the gate voltage is provided for each programmable current sources. The programmable current sources are consisted of two part, the blue boxed one which is normally used in conventional CTDSMs to provide reference current for each DACs and the red boxed one which requires additional silicon die area. In this technique, the blue boxed transistors are divided into some units in order to realize tunable α which is less than one. By selecting switches, DAC current can be reduced and it means small α can be gained without extra silicon die area. On the other hand, the curent mirror circuit boxed by red dot is utilized in order to compensate for the other range, from 0% to +30% process-dependent time constant shift. The number of selected "ON" switches increase in proportional to the time constant shift ratio in order to increase the value of α. For +30% time-constant shift, all the switches are "ON" and the output current is chosen as $(1.3)^i I_{ref}$. Thus, additional area of i-th programmable current sources can be expressed as $10L\{(1.3)^i - 1\}W_{ref}$. In this paper, the transistor size including drain, source and separation area is assumed to be 10 times larger than the transistor channel area. The total additional area of all programmable current sources A_p of the m-th order CTDSM is given as

$$A_p = 10L\sum_{i=1}^{m}\{(1.3)^i - 1\}W_{ref} \quad (1)$$

$$= \frac{20L^2 I_{ref}}{\mu C_{ox}{\Delta_{ov}}^2}\sum_{i=1}^{m}\{(1.3)^i - 1\}. \quad (2)$$

Here, eq. (2) can be expressed by square-law MOSFET model from eq. (1), where μ is the mobility of charge carriers, C_{ox} is the gate oxide capacitance per unit area and Δ_{ov} shows over drive voltage of current mirror circuit. I_{ref} can be decided by integrator's resistor R_{int} and maximum amplitude voltage of input signal for CTDSM, V_{max}. Additional programmable circuit area can be estimated as

$$A_p = \frac{20L^2 V_{max}}{R_{int}\mu C_{ox}{\Delta_{ov}}^2}\sum_{i=1}^{m}\{(1.3)^i - 1\}. \quad (3)$$

From the above equation, it is clear that the additional area can be reduced with the development in microfabrication evolution, because small size L and large μ and C_{ox} can be realized. In this analysis, die area of switches is not considered because same number of switches is also used in conventional capacitor tuning technique in same tuning resolution.

Second, the additional silicon area of capacitor bank is estimated as fol-

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lows. The additional capacitor bank area A_c can be given as

$$A_c = 2\sum_{i=1}^{m}\{(1.3)^i - 1\}\frac{C_i}{C_0}, \tag{4}$$

where C_i is the capacitance composing the i-th active-RC integrator, and C_0 is the unit capacitance $[F/m^2]$. The additional area of the i-th integrator's capacitor bank is $\{(1.3)^i - 1\}C_i$, which tolerates a +30% RC time constant shift. Normally, differential circuit must be considered, therefore $2C_i$ is chosen. The value of C_i in (4) can be derived from the i-th integrator's coefficient of CTDSM. C_i is given as (5),

$$C_i = \frac{\tau_i}{R_{int}}. \tag{5}$$

In this paper, each resistor of integrators is same, because feedback current of each DAC is set to same value, $k_m = k_{m-1} = \cdots = 1$. The area of capacitor bank A_c is derived from eq. (4), and (5)

$$A_c = \frac{2}{R_{int}C_0}\sum_{i=1}^{m}\{(1.3)^i - 1\}\tau_i. \tag{6}$$

Finally, the area comparison equation can be derived as

$$\frac{A_p}{A_c} = \frac{10L^2V_{max}C_0\sum_{i=1}^{m}\{(1.3)^i - 1\}}{\mu C_{ox}{\Delta_{ov}}^2\sum_{i=1}^{m}\{(1.3)^i - 1\}\tau_i}. \tag{7}$$

In fact, die area size A_p and A_c are strongly related with device parameters. Eq. (7), however, provides good indications of architecture decision. Here, an example result of area comparison $\frac{A_p}{A_c}$ between the proposed tuning technique and the conventional capacitor bank tuning technique is discussed. In order to advance concrete discussions, application is assumed for Wideband Code Division Multiple Access (W-CDMA) which a CTDSM is utilized for. The parameters used in the present study are $C_0 = 2\times10^{-3}$ [F/m^2], L=5 [μm], Δ_{ov}=0.25 [V]. The maximum voltage of the process is 1.8 [V], therefore V_{max}=0.9 [V] is chosen. The values of μ and C_{ox} are referred from 0.18 μm CMOS process information, and τ_i is designed using $\Delta\Sigma$ ToolBox [6] in order to gain SQNR around 75 dB and bandwidth is 2 MHz. 1-bit quantizer is utilized in the study and sampling frequency is 174 MHz. In the case of the forth-order modulator, tuning circuit area of the proposed technique can be reduced by 54.9% compared to that of conventional capacitor bank. It is well known that integrator's occupation area is dominant of total modulator area. This paper discusses the reduction area ratio of the total modulator's loopfilter area by using the proposed tuning technique. For example, it is assumed that the area of load capacitor is occupied a half of integrator's total area. Therefore conventional tuning circuit area of total modulator area is $\frac{1}{2}\times\frac{3}{10}$ because capacitor bank area consumes 30% of capacitor area, which is already mentioned before. By using the proposed technique, we can reduce around 55% of tuning area compared to conventional capacitor bank. It means that the reduction area of the total modulator's loopfilter area can be estimated around 8%. We have to estimate the ratio carefully before designing delta-sigma modulators because it is clear that the reduction area ratio depends on CMOS technology and design architectures.

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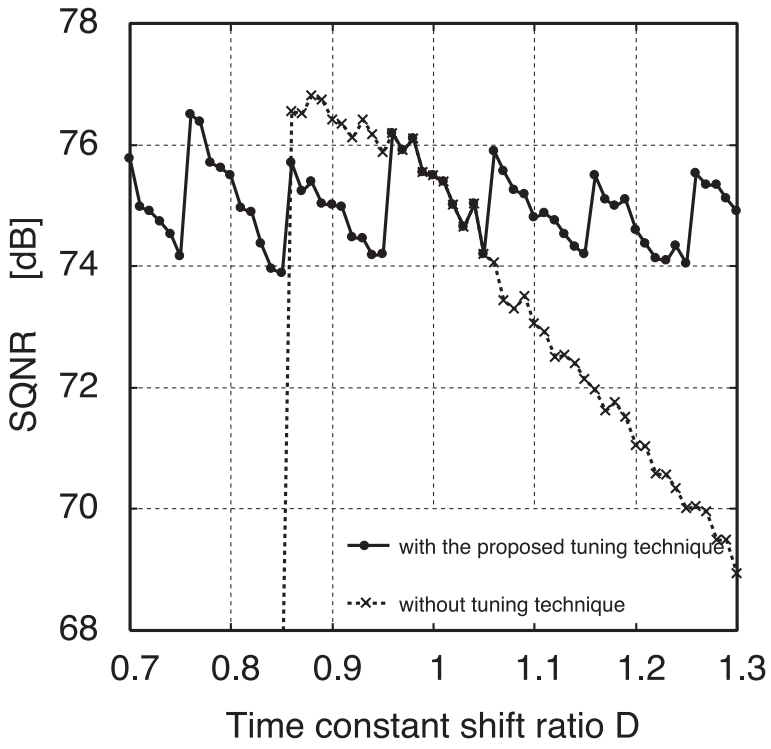

Fig. 3. Simulation results

3 Simulation results

In this section, simulation results obtained with and without the proposed technique are presented. The simulation results of a fourth-order 1-bit CTDSM with demonstrated that the tuning circuit area can be reduced 54.9% using the proposed technique, as compared to the conventional capacitor bank tuning technique. In the simulation, we use time constant shift ratios D of from 0.7 to 1.3 and a step value of 0.1 for the DAC tuning coefficient α.

Fig. 3 shows the results of a MATLAB/Simulink simulation with and without the proposed current tuning technique as a function of the systematic time constant shift ratio D due to process variation. The solid line, which indicates the simulation results for the modulator with the proposed technique, exhibits a stable SQNR performance around 75 dB and no instability, even if the possible variation of the RC time constant shifts up to +30% and −30%. Some discontinuous points, where α is changed at $D = 0.75$, 0.85, 0.95, 1.05, 1.15, 1.25, are appeared in Fig. 3.

In contrast, the SQNR of the modulator without any tuning technique decreases to 69 dB with a +30% process shift, and the modulator becomes unstable with a process time constant shift of less than −15%. These results demonstrate the effectiveness of the proposed tuning technique.

4 Conclusion

For CTDSMs, we proposed a novel RC time constant tuning technique using simple programmable current sources to compensate for the effect of systematic time constant shift. The proposed technique has an advantage in implemented die area over the conventional capacitor bank technique in

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a modulator for W-CDMA application. MATLAB/Simulink simulation results demonstrate that this technique can achieve the desired SQNR even with ±30% RC time constant shifts.

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