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An accurate track-and-latch comparator

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Abstract: In this paper, a new accurate track and latch comparator circuit is presented. The Offset voltage of latch is compensated by negative feedback loop and the low offset voltage is achieved without pre-amplifiers. The pull up devices in modified regeneration latch is turned off to reduce quiescent current of comparator within the tracking phase. The Monte-Carlo simulation results for the designed comparator in 0.18 μm CMOS process show that equivalent input referred offset voltage is 200 μV at 1 sigma while it was 26 mV at 1 sigma before offset cancellation. The comparator dissipates 400 μW from a 1.8 V supply while operates in 500 MHz clock frequency. The power consumption improvement is up to 33% over previously reported structure.

Keywords: latch comparator, offset cancellation, low offset, negative resistance, high speed
Classification: Integrated circuits

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1 Introduction

Making a fast and accurate decision is one of the fundamental needs in many applications, such as Analog to Digital Converters, data receivers and memory circuits. In common, this is accomplished by a high speed and high resolution comparator block using the preamplifier stages followed by dynamic latch circuit. High resolution comparator needs to amplify a small input voltage to a large enough level, detectable by regenerative latch within short time. Therefore, high-gain and high-bandwidth is required in accurate and high-speed comparators [1]. Realizing the high voltage gain amplifiers is very difficult because of low drain resistance caused by technology scaling. The design of accurate comparator circuit without preamplifier stages has been taken into account, recently [2, 3].

In this paper an offset compensated latch comparator is proposed which improves the accuracy by offset cancellation on latch stage instead of using the preamplifier stages.

2 Proposed low offset track and latch comparator

Fig. 1 (a) shows the circuit diagram of a conventional track and latch comparator [1, 2, 5]. The positive feedback of latch is ceased by choosing appropriate drain-source conductance of M_{sw} in comparison with transconductance of inverters. The latch makes correct decision if its initial voltage at output nodes be larger than latch's offset voltage. The proposed track and latch comparator is shown in Fig. 1 (b). Input signal differential pair (M1-M4), offset cancellation negative feedback loop (M15-M18, S5-S6 and C_H), modified regeneration latch (M5-M12) and a voltage controlled regeneration switch (M_{sn}, M_{sp}) form the comparator circuit. The proposed comparator has three operating modes: offset cancellation, input tracking and latch regeneration modes. Within offset cancellation phase, the input differential pair is disconnected from analog inputs (V_{in+}, V_{in-}) by S1 and S2 switches and connected to common mode voltage level (V_{icm}) by S3 and S4 switches. At the same time, the S5 and S6 switches close the negative feedback loop. This loop consists of a differential pair same as input one and offset storage capacitor, C_H. Both of analog input differential pair and offset cancellation differential pair are connected to output nodes through the cascode devices (M3-M4 and M17-M18) to reduce the kick back noise effect of regeneration latch. During offset cancellation phase, the M_{sn} and M_{sp} transistors are turned on and act as small resistive load to prevent latch regeneration. The M5-M8 transistors are the main devices of modified regeneration latch. Before each comparison cycle, the voltage of output nodes (V_{out+} and V_{out-}) are equalized by reset signal (Rst) within a short time. This makes the comparator's recovery time as short as possible for next comparison cycle. The M9 and M10 transistors are cross coupled devices and the gate-source voltage equation are as follow:

$$\begin{cases} V_{gs9} = V_{out+} - V_{out-} \\ V_{gs10} = V_{out-} - V_{out+} \end{cases} \quad (1)$$

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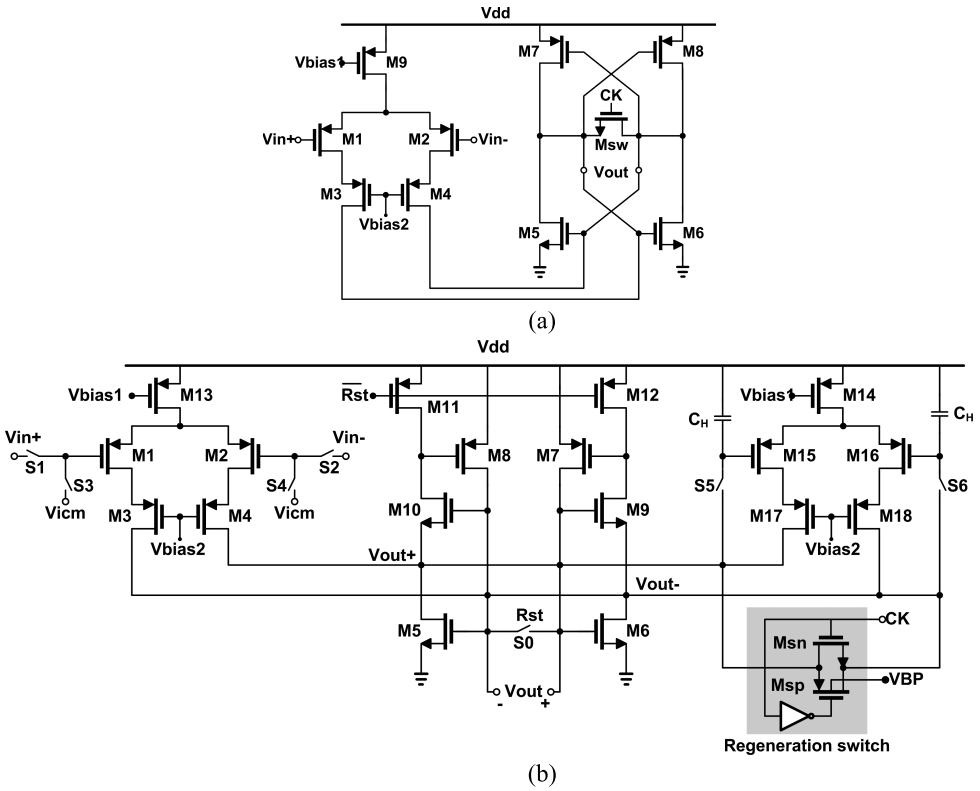

Fig. 1. (a) Conventional track and latch comparator (b) Proposed offset cancelled track and latch comparator

Owing to reset the output nodes ($V_{out+} - V_{out-} = 0$), both of the M9 and M10 transistors are turned off and disconnect the strong pull-up devices (M7 and M8) from output nodes. The gate voltage of M7 and M8 transistors are also charge to supply voltage to turn off these devices at the beginning of each offset cancellation and comparison cycle. This idea reduces the static current steering and power consumption in comparison with conventional regeneration latch.

All M7-M12 transistors are turned off during offset cancellation phase, and the M5 and M6 devices make a negative resistive load at output nodes. But the effect of positive feedback is ceased by high drain-source conductance of M_{sn} and M_{sp} transistors. Using simplified half circuit small signal model for proposed comparator, the voltage gain can be calculated as follow [3]:

$$A_{vf} = \frac{g_{m1,2}R_o}{1 + g_{m15,16}R_o} = \frac{g_{m1,2}}{2g_{sw} + g_{out} + g_{m15,16} - g_{m5,6}} \quad (2)$$

Where R_o is the equivalent resistance seen at the output nodes to ground, g_{sw} is the drain-source conductance of regeneration switch ($g_{ds\_Msn} + g_{ds\_Msp}$) and g_{out} is the drain-source conductance of M5 and M6 transistors (All M7-M12 transistors are turned off during offset cancellation phase). If the total equivalent offset voltage of comparator has been modeled as V_{off} on its input, the remained equivalent input referred offset voltage after offset cancellation

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is as below:

$$\hat{V}_{off,in} = \frac{2g_{sw} + g_{out} - g_{m5,6}}{2g_{sw} + g_{out} + g_{m15,16} - g_{m5,6}} \times V_{off} \quad (3)$$

As above equation, the input referred offset voltage can be eliminated by zeroing the numerator term. This is accomplished by choosing appropriate regeneration switch (M_{sn} and M_{sp}) size in comparison with the size of M5 and M6 transistors to minimize $2g_{sw}+g_{out}+g_{m15,16}-g_{m5,6}$ term. The values of g_{out} and $g_{m5,6}$ are not constant through temperature and process variations. Therefore the g_{sw} is assumed adjustable conductance. This is implemented by adjusting bulk voltage of M_{SP} transistor (V_{BP}) which affects the drain-source conductance of M_{SP} transistor through body effect. The bulk voltage is determined by a Schmitt-trigger oscillator similar to proposed one in [4]. Based on proposed comparator circuit, a Schmitt-trigger oscillator is implemented with V_{BP} voltage feedback as shown in Fig. 2. Increasing the bulk voltage of regeneration switch (M_{SP}) reduces the switch conductance and makes the $(2g_{sw}+g_{out}+g_{m15,16})$ value be closer to M5 and M6 transconductance. When $g_{m5,6}$ is equal to $(2g_{sw}+g_{out}+g_{m15,16})$ value, the voltage gain of replica comparator becomes infinitely large and comparator develops hysteresis and behaves as a Schmitt-trigger. If the oscillation has not been started, the V_{BP} voltage is increased and causes the g_{sw} value be decreased. This makes $g_{m5,6}$ be greater than $(2g_{sw}+g_{out}+g_{m15,16})$ and oscillation will be started in replica comparator based Schmitt-trigger oscillator. If the oscillation be still with large amplitude ($g_{m5,6}$ is too greater than $2g_{sw}+g_{out}+g_{m15,16}$), the V_{BP} voltage will be decreased to cause g_{sw} increasing and finally the determined V_{BP} value in oscillator feedback will still cause oscillation with small amplitude in Schmitt-trigger oscillator. The size of Msp transistor in main comparator circuit is considered something greater than its size in replica circuit. This increases the value of g_{sw} in main circuit and guarantees the $(2g_{sw}+g_{out}+g_{m15,16})$ term be closely greater than $g_{m5,6}$ and makes the value of equation (2) be positive and high regardless of temperature and process variations.

Adjusting the conductance of regeneration switch not only helps to minimize the input referred offset voltage, but also increases the gain of comparator within the input tracking phase. During tracking mode, the output nodes track the input signal to initialize the latch before regeneration. The regeneration phase is started by opening the regeneration switch and the positive feedback of M5 and M6 transistors toggle the output nodes, consequently. If the voltage difference of output nodes be closer to device threshold voltage, one of the M9 and M10 transistors is turned on (equation (1)) and connects the M7 or M8 device to pull up appropriate output node, strongly. To speed up the regeneration process, it is required to turn on the M7-M8 transistors as soon as the output voltage difference dominates the remained offset voltage at output nodes. In general, this is so smaller than device threshold voltage and medium threshold devices (with lower threshold voltage) are used as M9 and M10 transistors in proposed latch.

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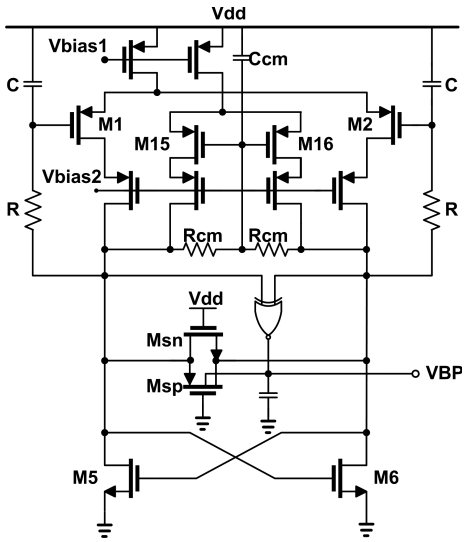

Fig. 2. The Schmitt-trigger oscillator based on replica circuit of proposed latch comparator to tune the bulk voltage of regeneration switch

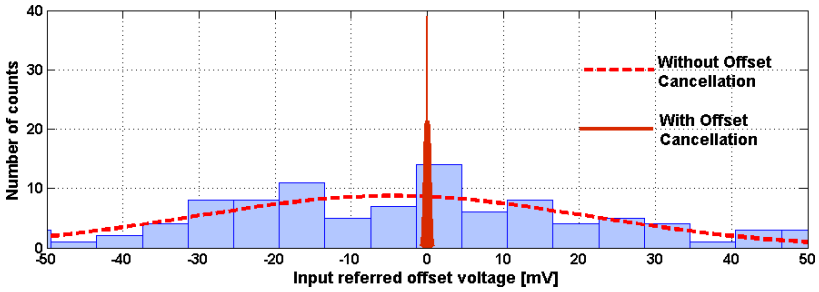

Fig. 3. Histogram of equivalent input referred offset voltage before and after offset cancellation

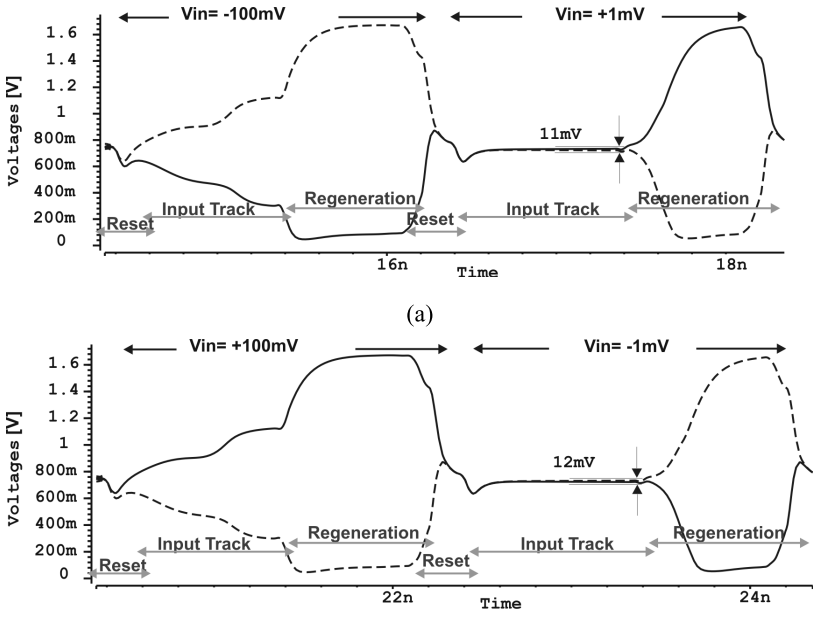

Fig. 4. (a) Overdrive recovery test (1 mV input proceeded by −100 mV). (b) Overdrive recovery test (−1 mV input proceeded by +100 mV)

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3 Simulation results and comparison

The proposed low offset latch comparator has been designed and simulated in HSPICE using a 0.18 μm CMOS process. To model the mismatch offset voltage, the series voltage sources with Gaussian-distributed values were placed on gate node of each paired transistors as well as regeneration switches in main comparator and replica circuits and Monte-Carlo simulation was performed. The equivalent input referred offset voltage was measured by applying slowly varying slope signal to comparator input. Absolute Gaussian-distributed 80 mV at 3 sigma offset voltage was applied to all transistors and 100 samples transient Monte-Carlo simulations were accomplished. Fig. 3 shows the histogram of equivalent input referred offset voltage for proposed comparator before and after offset cancellation. The illustrated histogram shows 26 mV at 1 sigma equivalent input referred offset voltage before calibration. This value achieved 200 μV at 1 sigma after offset cancellation. To evaluate the dynamic performance of the designed comparator, two overdrive recovery tests were performed. Fig. 4 (a) shows the simulation result of comparator output nodes voltage when -100 mV input signal followed by $+1$ mV after offset cancellation. The offset voltage of all transistors in this test were also modeled by similar series voltage source with Gaussian-distributed 80 mV at 3 sigma and transient Monte-Carlo simulation was performed. The similar overdrive test was done by applying -1 mV proceeded by $+100$ mV input signal and the output waveform is depicted in Fig. 4 (b). The proposed comparator can successfully resolve difference of 1 mV at 500 MHz clock frequency without any preamplifier stage. It consumes about 400 μW from a 1.8 V supply.

As the performance comparison of the proposed approach with previously reported works, the standard deviation of input referred offset voltage (V_{off_σ}) is listed in Table I before and after offset cancelation. Overall power consumption and comparison speed is also compared. Reference [2] does not require any amplifier for offset cancellation and utilizes a charge pump circuit to self-calibrating process. The remained input referred offset voltage (standard deviation) is reported 1.69 mV while it was 13.7 mV before calibration. In report [5], the achieved input referred offset voltage (V_{off_σ}) is 3.8 mV while it was 12.8 mV before cancellation. The difficulty of producing an optimum value for this bias voltage can be introduced as a drawback of [5] approach. Digital calibration method is used in [6] to equalize the current mismatch of

Table I. Performance comparison

Parameter	[2]	[5]	[6]	[3]	This work
$V_{off\_1\sigma}$ (mV) before cancellation	13.7	12.8	31.8	26	26
$V_{off\_1\sigma}$ (mV) after cancellation	1.69	3.8	4.3	0.2	0.2
f_{ck} (MHz)	250	500	1400	500	500
Power Consumption	40μW/GHz	39 μW	350 μW	600 μW	400 μW
Process (nm)	90	90	180	180	180

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dynamic latch due to input transistors mismatches. It achieves 4.3 mV for V_{off_σ} after performing calibration procedure where it was 31.8 mV before calibration. Notwithstanding the perfect accuracy of proposed comparator, the drawbacks with it are high transistor counts/silicon area and power consumption in comparison to [2, 5] and [6] works. However, the modified offset cancellation loop and regeneration latch structure which turns off the pull up devices, introduces the saving of more than 33% power consumption compared to previously reported structure [3].

4 Conclusions

A new accurate latch comparator was presented. The proposed topology employs conventional negative feedback to store the latch offset voltage on holding capacitors and eliminates the usage of preamplifier stages before latch. A gain enhancement technique based on latch positive feedback and bulk voltage controlled regeneration load has been utilized to provide sufficient gain for offset cancellation. A modified regeneration latch with no quiescent current was also presented. The Monte-Carlo simulation results for the designed comparator in 0.18 μm CMOS process show that equivalent input referred offset voltage is 200 μV at 1 sigma while it was 26 mV at 1 sigma before offset cancellation.

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