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A superior-order curvature corrected bandgap reference with less sensitivity of mismatch

Jing-Hu Li[1a)], **Xing-Bao Zhang**[1], **Jie Ma**[2], **Ming-Yan Yu**[1], **and Xue-Jun Sha**[3]

[1] *School of information science and engineering, Harbin Institute of Technology (Weihai), Weihai city, Shandong Province, China*

[2] *Tianjin Vast Technology, co, ltd, Tianjin city, China*

[3] *School of information and communication engineering, Harbin Institute of Technology, Harbin city, Heilongjiang Province, China*

a) *tigerlihit@sohu.com*

Abstract: A superior-order curvature corrected bandgap reference (BGR) is proposed. The BGR features itself by adding only an extra NMOS transistor to a first-order BGR. The extra transistor generates a piecewise nonlinear corrected current to reduce its temperature coefficient (TC) and forms a negative feedback to decrease the variation of offset and TC caused by mismatch. Measurement result shows the proposed BGR achieves most optimal TC of 2.8 ppm/°C in the temperature range of −40∼125°C. The variation of offset and TC among different samples are reduced by the negative feedback effectively.

Keywords: piecewise nonlinear curvature corrected, temperature coefficient, offset

Classification: Integrated circuits

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1 Introduction

Bandgap references (BGRs) are essential functional modules for most analog and mixed-signal integrated circuits, which will generate a reference voltage with low temperature coefficient (TC) [1]. To increase its precision and decrease the TC further, some curvature-corrected BGRs utilizing the piecewise linear [2], piecewise nonlinear curvature correction [3], temperature dependant resistor ratio technique [4] have been reported in standard CMOS process to be integrated with other very large scaled integrated circuits. But the mismatch of transistor and resistor omni presented in any fabricated process will generate offset voltage and increase the TC of different samples [5, 6], which will deteriorate the precision of the BGRs dramatically.

In this paper, a curvature corrected BGR is proposed by adding an extra transistor to a first-order BGR, which also forms a negative feedback to decrease the sensitivity of precision caused by mismatch.

2 Proposed circuit

The circuit of proposed BGR is shown in Figure 1, which is implemented by adding an extra transistor to a first-order BGR. The first-order BGR includes startup, bias and core of the BGR. The startup and bias circuit will provide bias voltage for the cascade current mirror when the power supply is on. Then a current proportional to absolute temperature (PTAT) is generated,

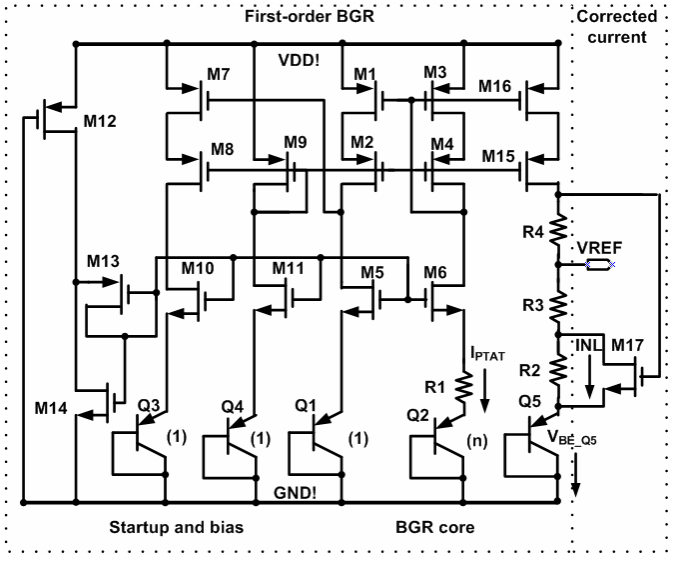

Fig. 1. The proposed superior-order BGR circuit

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which is

$$I_{PTAT} = \frac{V_T \ln(n)}{R1} = \frac{KT \ln(n)}{qR1} \tag{1}$$

Here V_T is the thermal voltage, K is the Boltzmman's constant (1.38×10^{-23} J/K), T is the absolute temperature in degrees Kelvin (°K), q is the electronic charge (1.6×10^{-19} C), n is the area ratio of Q1 and Q2. The PTAT current is mirrored and transferred into a PTAT voltage by resistor R2 and R3. The first-order BGR is achieved by combining the PTAT voltage and the base-emitter voltage of Q5 complementary to absolute temperature (CTAT) in first-order [1]. The output voltage of the first-order BGR is expressed as

$$VREF_{First\text{-}order} = V_{BE\_Q5} + \frac{(R2 + R3)V_T \ln(n)}{R1} \tag{2}$$

The simulated most optimized TC of the first-order BGR is 23 ppm/°C in the TR of −40–125°C. To reduce the TC further, an extra transistor M17 is added to the first-order BGR to implement a superior-order BGR. The gate-source voltage of M17 is proportional to absolute temperature, which is given as

$$V_{GS\_M17} = I_{PTAT}(R2 + R3 + R4) \tag{3}$$

In the lower temperature range (TR), VGS_M17 is less than or near its threshold. NMOS transistor M17 works in the sub threshold region, the nonlinear piecewise corrected current I_{NL} is given as

The correction is:

$$I_{NL} = \frac{W}{L} I_t \exp\left(\frac{V_{GS\_M17} - |V_{THN}|}{\xi V_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{4}$$

The temperature dependence of the nonlinear current is given as $I_{NL} \propto \exp(V_T)$ [3]. When the temperature is higher than its threshold, M17 works in the linear region, I_{NL} is expressed as

$$I_{NL} = \mu_n C_{OX} W/L(V_{GS\_M17} - V_{TH})(I_{PTAT} - I_{NL})R2 \tag{5}$$

Here μ_n is the electron mobility, C_{OX} is the gate capacitance per unit area, V_{TH} is the threshold voltage. $(I_{PTAT} - I_{NL})R2$ is the drain-source voltage of M17. The temperature coefficient of electronic mobility is approximately as $\mu_n \propto T^{-\frac{3}{2}}$. Considering the high-order temperature dependence and neglecting the lower one in (5), the approximate temperature dependence of $I_{NL} \propto T^{\frac{1}{2}}$ is achieved. In a word, the piecewise curvature-corrected current is outlined as

$$I_{NL} = \left\{ \begin{array}{cc} \propto \exp(T) & V_{GS\_M17} \leq V_{TH} \\ \propto T^{\frac{1}{2}} & V_{GS\_M17} > V_{TH} \end{array} \right\} \tag{6}$$

Then the output reference voltage for the proposed BGR is given as

$$VREF = V_{BE\_Q5} + \frac{V_T \ln(n)(R2 + R3)}{R1} - I_{NL}R2 = V_{First\text{-}order} - I_{NL}R2 \tag{7}$$

The simulated TC of the proposed BGR is only 1.8 ppm/°C in the TR of −40–125°C, nearly 10 times better than that of the first-order BGR. Theoretically, curvature corrected technique proposed in this paper and than in

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[2, 3, 4] can decrease the temperature drift significantly. However, mismatch of the resistor and transistor will be omni presented in any fabrication process, which will increase the offset voltage and decrease the measured TC among different chips dramatically. As a result, trimming after fabrication is often be used in most of high-precision BGRs [5, 6] to reduce its variation of offset and TC.

Another advantage of the proposed BGR is that a negative feedback loop is formed between the reference voltage (VREF) and the curvature corrected current I_{NL}. The variation in VREF will be sensed by I_{NL}, which will be subtracted from the output voltage. In all, the negative loop will exist and function properly to reduce reference error caused by resistor and transistor mismatch.

Assume a mismatch $+\Delta R$ existed between R1 and (R2 + R3), then the variation of the reference voltage for the first-order BGR is calculated as

$$\Delta VREF = \frac{\Delta R}{R1} V_T \ln(n) \tag{8}$$

Then the gate-source voltage of M17 will also be affetecd by the mismatch, which is

$$V_{GS\_M17\_Mis} = \frac{V_T \ln(n)(R2 + R3 + R4 + \Delta R)}{R1} \tag{9}$$

According to (5), the variation of the nonlinear current is

$$\Delta I_{NL} = \mu_n C_{OX} \frac{W}{L} \frac{\Delta R}{R1} \tag{10}$$

Then the variation of the proposed BGR due to mismatch is

$$\Delta VREF = \left(V_T \ln(n) - \mu_n C_{OX} \frac{W}{L} R2 \right) \frac{\Delta R}{R1} \tag{11}$$

As given in (11), the offset voltage caused by resistor mismatch is reduced by the negative feedback loop, which will also decrease the variation of TC among different samples.

3 Experiment result

The proposed BGR is fabricated in global foundry 0.35-μm mixed-signal CMOS process with effective chip area of $300\mu \times 200\mu$m. The measured most optimal TC and line regulation of the proposed BGR is shown in Figure 2. Figure 2 (a) shows its temperature dependence in the TR of −40–125°C. The maximum and minimum output voltage is 1.2928 V and 1.2922 V respectively. So the measured TC is only 2.8 ppm/°C. The line regulation of the proposed BGR is shown in Figure 2 (b). The reference voltage (VREF) will increase when the supply voltage (VDD) is less than 2 V. The maximum and minimum output voltage is 1.2926 V and 1.2940 V in the supply voltage range of 2–4 V. So the line regulation is 0.7 mV/V.

The variation of the offset voltage and that of TC among 10 different samples is shown in Figure 3. Figure 3 (a) shows the measured offset voltage of the first-order BGR and that of the proposed BGR among ten different samples for the temperature of 25°C. The maximum and minimum offset voltages

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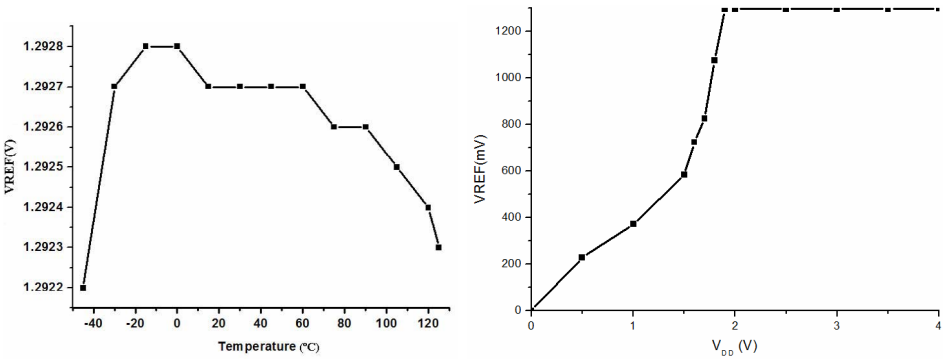
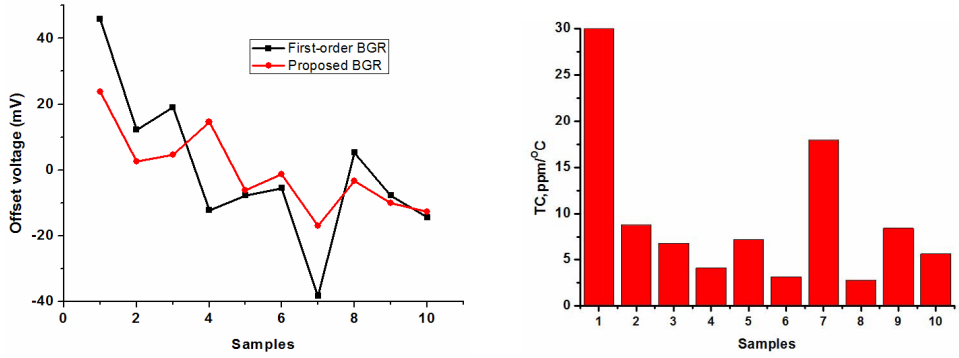


(a) (b)

Fig. 2. (a) Temperature dependence of the proposed BGR when VDD = 2 V (b) VREF varying with VDD from 0 to 4 V



(a) (b)

Fig. 3. (a) Offset voltage variation of the first-order and proposed BGR (b) Variation of the measured TC

of the first-order BGR are 45.8 mV and −38.3 mV respectively. While the maximum and minimum offset voltages of the proposed BGR are 23.7 mV and −16.8 mV respectively. As given in Figure 3 (a), the offset voltage range of the proposed BGR is reduced nearly 50% than that of the first-order BGR. Figure 3 (b) lists the variation of measured TC of ten different samples. Among them, the TC of sample 1 and sample 7 are 30 ppm/°C and 18 ppm/°C respectively. The TC of other samples is less than 10 ppm/°C.

4 Conclusion

A superior-order BGR with TC of 2.8 ppm/°C in the TR of −45–125°C is proposed. The nonlinear piecewise curvature corrected current generator in the proposed BGR also forms a negative feedback to reduce its offset and TC variation caused by mismatch.

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