Design a 10-Bit 100 MHz pipelined ADC using RB-OTA in 90 nm CMOS technology

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Abstract: In this paper a low consumption 10 bits pipelined analogue to digital converter (ADC) by using a new operational transconductance amplifier (OTA) is introduced. The ADC is designed to work at 100 MHz with 1 volt bias voltage in a CMOS 90 nm technology. The simulation results at frequency of 5 MHz show the spurious free dynamic range and signal to noise ratio of 66 dB and 58.4 dB (9.4 ENOB) respectively. The power consumption for the designed ADC including digital and analogue parts is 14.4 mW.

Keywords: multiplying digital-to-analogue converter (MDAC), Resistive Bias OTA (RB-OTA), Switched capacitor (SC)

Classification: Integrated circuits

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1 Introduction

In high speed pipelined analogue to digital converters there are many techniques to decrease the power consumption. Some of these techniques are stage scaling, resolution per stage optimization and Op-amp sharing. Although these techniques have lowered the power consumption to some extend but more power consumption reduction is a major challenge for the circuit designers.

However, using alternative methods in which the power consumption is lowered by replacing Op-amp with open loop amplifier and incorporating digital calibration has been also successful [1]. Track and hold Amplifier (THA) which is placed at the input of the pipelined ADC to improve the overall performance of the circuit consumes considerable amount of the power. Another circuit in the pipelined converter which has huge power consumption is multiplying digital-to-analogue converter (MDAC). Suggesting a proper technique to lower the power consumptions for these two circuits can save huge amount of consumed power of the operational transconductance amplifier (OTA). Op-amp as a main element in the ADC is one of the most power consumer. In this paper to reduce the power consumption we suggest a proper circuit technique. To further decrease the power consumption we also used stage scaling technique in combination with modified dynamic comparator.

2 Design of the basic block of pipelined ADC

MDAC as a repeating circuit block is a basic subsystem of pipelined ADC. This block in turn consists of few elements such as OTA, comparator and switches.

2.1 Selection of sampler capacitor value

In order to reduce the thermal noise associated with switches, the sampler capacitor should have a proper capacitance. However, due to the other noise sources such as quantization noise, selecting capacitance with higher than a certain value does not affect the signal to noise ratio (SNR). The value of the sampler capacitor should be selected in such a way that the thermal noise associated with the switches to be less than 25 percent of the quantization noise power. It means:

$$\frac{KT}{\beta C} = \frac{1}{4}\frac{\Delta^2}{12} \qquad (1)$$

Where $\Delta^2/12$ is quantization noise, K is Boatman's constant, T is temperature in Kelvin and β is a feedback factor. Using this assumption, the sampler capacitor is selected to be $0.2\,pF$. However in practice, the value for the sampler capacitor is chosen to be $1\,pF$ to reduce the effect of its parasitic.

2.2 Design of OTA

In this section a modified two-stage OTA to satisfy the requirements of 10 bits pipelined ADC is designed. In order to design an operational amplifier, we

should first know the DC gain and the required bandwidth. However, large signal characteristics of OTA such as settling time and slew rate normally affect the bandwidth requirement. The non-complete settling error due to the limited unity gain bandwidth causes a linear error component while the limitation in the slew rate capability associated with OTA can give rise to nonlinear error.

During the time that the input voltages difference of OTA or $|V_{id}|$ is greater than $V_{dsat} = 1.4(2/g_m I_D)$, the OTA operates in its nonlinear region that called nonlinear settling time. The rest of the time is called linear settling time. The duration of linear settling time is a function of the unity gain bandwidth. This parameter is of great important in the circuits having high gain since in these circuits the input signal is not high enough to cause OTA to operate in the nonlinear region while in low gain circuits such as $MDAC$ used in 1.5-bits per stage circuits, nonlinear settling time is dominant part of the settling time.

2.2.1 Loop gain

The quantization noise at each stage is determined by DC gain. The maximum allowable quantization noise for each stage should be less than $\pm 1/2\,LSB$ of that stage. Value of LSB at stage i is equal to:

$$LSB_i = \frac{V_{FS}}{2^{N-(i-1)}} \tag{2}$$

Where V_{FS} maximum input voltage variation and N is is the number of bits for ADC. For example the maximum allowable quantization error (noise) for the first stage $(i = 1)$ is:

$$\epsilon_Q = \pm\frac{1}{2}\frac{V_{FS}}{2^N} \tag{3}$$

Therefore, the required loop gain for OTA for this stage is:

$$T_1 = A_{ol}\beta = \frac{2^{N+1}}{V_{FS}} \tag{4}$$

Hence:

$$A_{ol} = \frac{2^{N+1}}{V_{FS}\beta} \tag{5}$$

Where A_{ol} is "open loop gain" of OTA, and β is feedback factor.

2.2.2 Unity gain bandwidth

In cascode compensation method [2], in addition to the low frequency real poles, two complex conjugate poles are also created and calculation of the frequency response of the system is complicated. In the proposed Miller's compensation method we can assume that the compensated system is a single pole. Using this assumption, error due to the finite value of settling time is:

$$\epsilon_S = V_{FS} - V_{OUT} \tag{6}$$

This error should be less than $0.5\,LSB$. For this system, the step response can be expressed as:

$$V_{OUT} = V_{FS}(1 - e^{-T_S/\tau}) \tag{7}$$

Where T_S is settling time of OTA and τ is time constant of the system. In the first stage, one can write:

$$e^{-T_S/\tau} = \frac{1}{2}LSB = \frac{V_{FS}}{2^{N+1}} \tag{8}$$

As a result:

$$T_S = \tau Ln\frac{2^{N+1}}{V_{FS}} = \frac{1}{2\pi f_T}Ln\frac{2^{N+1}}{V_{FS}} < \frac{1}{2}T_{CLK} = \frac{1}{2f_{CLK}} \tag{9}$$

Therefore,

$$\frac{f_{T1}}{f_{CLK}} \geq \frac{1}{\pi}ln\frac{2^{N+1-i}}{V_{FS}} \quad \xrightarrow{yields} \quad f_{T1} \geq \frac{1}{\pi}ln\frac{2^{N+1-i}}{V_{FS}}f_{CLK} \tag{10}$$

In practice due to the environment condition and fabrication process variations, unity gain bandwidth is considered to be twice of what is required.

2.2.3 OTA topology and proposed OTA

As the required gain is $72\,dB$ and due to this fact that intrinsic gain at $90\,nm$ $CMOS$ technology is around $20\,dB$, we can conclude that gain function for OTA should be of third order. It means $A_V \approx (g_m r_o)^3$. Therefore, we should implement two stages amplifier whose first stage's intrinsic gain is $(g_m r_o)^2$. Considering this fact, there are two options for the first stage which are either telescopic or folded cascade.

Due to low voltage value of $1\,V$, we cannot use more than four transistors in the cascode topology since the design procedure becomes very complicated. In addition, using telescopic topology reduces the common mode input voltage and CMR. Thus, we proposed folded cascode for the first stage. The second stage is a simple source follower with active load. In request to a voltage level shifter which increases the voltage swing of second stage, a capacitive level shifter is preferred to source follower for its lower power consumption. However for this structure it is required to charge the coupling capacitor with an appropriate and constant voltage. To do this, the capacitor is connected to a constant voltage during common mode adjusting time. This coupling capacitor is placed between first stage's output and second stage's input as shown in Fig. 1 (a). The coupling capacitor is charged in common mode adjusting time. In this time, top plate is charged with first stage CMFB and as it is shown in Fig. 1, two switches, two resistors and input transistor of second stage determine the voltage of capacitor's bottom plate when the op-amp is in common mode adjusting period.

Fig. 1 (a) shows proposed OTA called Resistive Bias OTA (RB-OTA) [3] which is used in 10 bits pipelined ADC stages. Fig. 1 (b) shows AC responses of the designed OTA respectively.
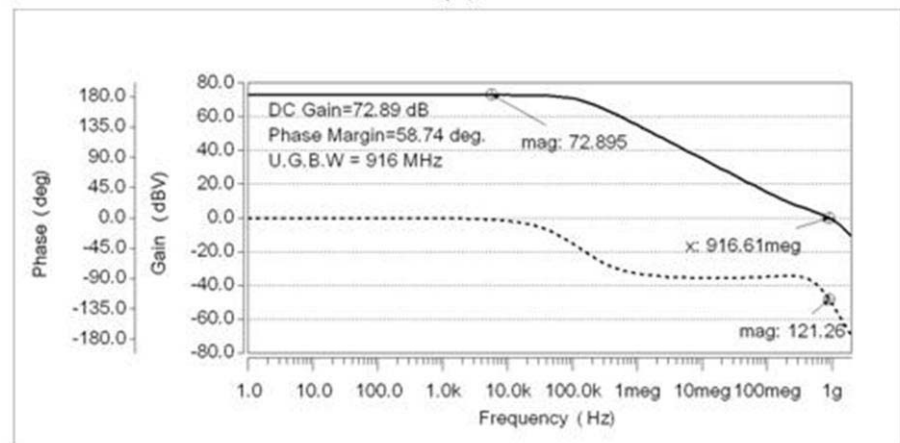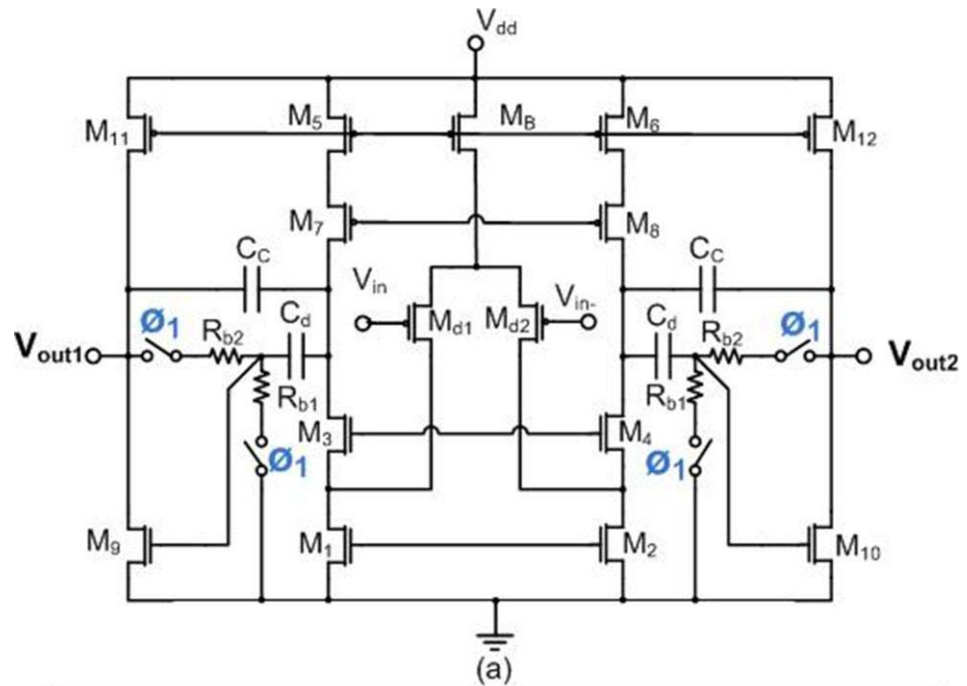
Fig. 1. (a): Proposed RB-OTA circuit (b): AC response of the designed OTA

3 Simulated results

The designed ADC was simulated by H-Spice software using L90_SP10_V051 model in CMOS technology with MIM capacitor and P'POLY resistors. The supply voltage and maximum input peak-to-peak voltage were 1 V and 0.8 V respectively. The simulation results show that the power consumption for all digital and analogue part is 14.4 mW. The SNDR and SFDR at the frequency of $(13/256) \times 100\,\text{MHz} = 5.78125\,\text{MHz}$ are 66 dB and 58.4 dB (9.4 ENOB) respectively. Fig. 2 shows the 1024 point FFT spectrum in part (a) and effective number of bit as a function of input frequency in part (b) SNDR, SFDR and THD parameters as a function of frequency are showing in part (c). In addition to investigate the nonlinearity we implemented Mont-Carlo analysis. This analysis showed that the values of INL and DNL at 93% of the time are less than 0.5 LSB. Table I shows the summary of our proposed OTA
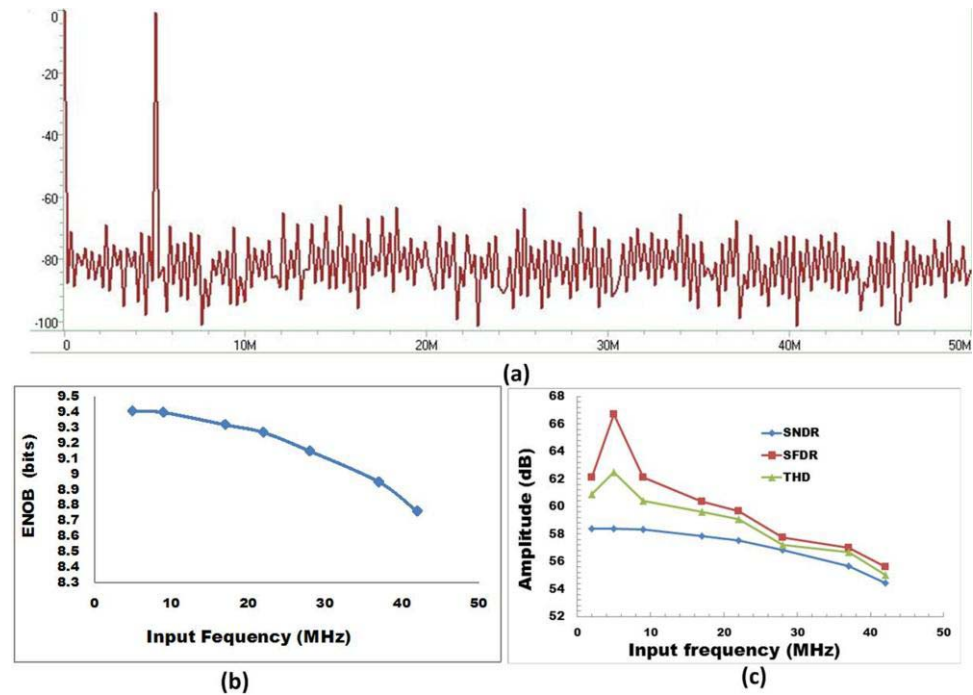
Fig. 2. (a): 1024 point FFT Spectrum for 5 MHz input frequency (b): Effective Number of bits versus input frequency (c): SNDR, SFDR and THD versus input frequency

performances, and Table II shows the summary of the ADC performances. In Table III we compared the performances of our proposed ADC with those of other 10 bits ADCs reported in the literature. In this table the figure of merit (FOM) of the designed ADC was also compared with that of the other

Table I. Summary of OTA performance

Process (nm)	V_{DD}	DC Gain	Unity Gain Band Width	Phase margin @1pF (β=1)	Slew Rate	Output voltage swing (Vp-p dif.)	Input CMR	Settling time (0.05%)	SFDR
90	1 V	72.89 dB	916 MHz	58.7º	130 V/us	1.2 V	0.8 V	3.6 nS	73.37 dB

Table II. Summary of ADC performance

Technology	UMC090 nm Digital CMOS technology
Resolution	10 bits
Architecture	Pipelined
Conversion Rate	100MHz
Input Range	0.8 V $_{p-p}$
Supply Voltage	1 V
DNL	0.82/-0.45
INL	0.63/-0.56

Table III. Comparison with 10-bit Reported Pipelined ADCs

Reference	Process (nm)	V_{DD} (V)	F_S (MHz)	SNDR (dB)	Power (mW)	FoM (pJ.V/step)
[4]	90	1	30	58.4	4.7	**0.23**
[5]	90	1	100	55.3	33	**0.69**
[6]	90	0.8	80	51.4	6.5	**0.21**
[7]	90	0.9	100	59	15.8	**0.19**
This work	90	1	100	58.1	14.4	**0.17**

ADC circuits.

$$FoM = \frac{POWER}{2^{ENOB}.F_s}V_{DD} \qquad (11)$$

4 Conclusion

Low-voltage and low-power RB-OTA 1.5 bit MDAC for low-power low-voltage Pipelined ADC was presented. By employing the proposed OTA in 90 nm CMOS process and 1 V supply voltage, the simulation results show that the power consumption for all digital and analogue part is 14.4 mW. The SNDR and SFDR at the frequency of $((13)/256) \times 100$ MHz $= 5.78125$ MHz are 66 dB and 58.4 dB (9.4 ENOB) respectively. In addition to investigate the nonlinearity we implemented Mont-Carlo analysis. This analysis showed that the values of INL and DNL at 93% of the time are less than 0.5 LSB.