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Simulation study on scaling limit of silicon tunneling field-effect transistor under tunneling-predominance

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Abstract: In this work, a strategic methodology to determine the channel length limit for the predominance of tunneling mechanism in the operation of a tunneling field-effect transistor (TFET) is suggested and validated for silicon (Si) nanowire TFET device. For quantitative analyses that can be graphitized as a function of channel length, a set of evaluating functions were defined and properly applied. Based on the suggested methodology, the upper limit for keeping the Si TFET under the tunneling-predominant operation turned out to be approximately 65 nm in a nanowire structure.

Keywords: methodology, channel length limit, tunneling field-effect transistor, silicon nanowire, evaluating function, tunneling-predominance

Classification: Electron devices, circuits, and systems

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1 Introduction

Recently, tunneling field-effect transistors (TFETs) are under intensive researches due to its steep switching characteristics and low-power consumption aiming green technology [1, 2, 3]. Efforts for higher on-state current (I_{on}) are also widely made in parallel to overcome the drawback of low I_{on} silicon (Si) TFET has [4, 5]. We verified by simulation works that there is a limit in channel length of Si TFETs below which I_{on} is not governed by the channel mobility [6]. By knowing this boundary, one can design either a longer Si TFET with higher I_{on} driven by both tunneling and drift-diffusion (DD) currents or a shorter one screening out DD components to bear higher robustness to the process and performance variations.

2 Device structure and simulation approach

Qualitatively speaking, there are factors determining TFET's I_{on}: effective mass (m_{eff}), bandgap energy (E_G), and channel electron mobility (μ_n) [7]. The effect of μ_n is rather indecisive compared with the other two factors. In other words, it does not emerge as a prominent factor until DD mechanism dominates in driving currents. Channel radius and oxide thickness were 10 nm and 2 nm, respectively, while the channel lengths were varied from 30 nm to 5 μm. The doping concentrations of p^+ type source and n^+ type drain were boron (B) $1\times10^{20}\,\mathrm{cm}^{-3}$ and arsenic (As) $1\times10^{18}\,\mathrm{cm}^{-3}$, respectively, and the channel was undoped to fully eliminate the effect of impurity scattering on μ_n which was a control variable in this work. The on-state operation condition was $V_{GS} = V_{DS} = 0.9\,\mathrm{V}$ (V_{GS}: gate-to-source voltage, V_{DS}: drain-to-source voltage). A gate workfunction of 4.7 eV was presumably used.

Multiple models were included for higher simulation accuracy: Shockley-Read-Hall (SRH) recombination, Fermi statistics, non-local band-to-band tunneling, and quantum effects. To identify the maximum channel length by which I_{on} is driven predominantly by tunneling, the channel mobilities were controlled. This is definitely a fictitious manipulation in a sense that there is no such an intrinsic material having all the same characteristic material parameters except μ_n. However, we would like to put an emphasis that this

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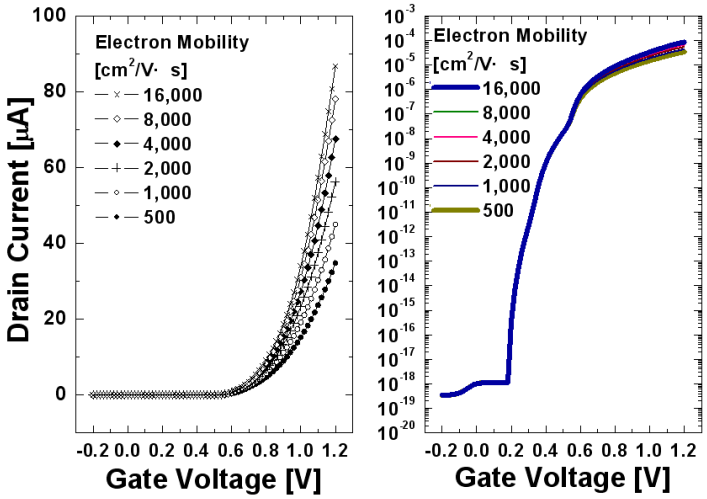
approach is a very effective strategy that can be achieved only by simulation works with genuineness.

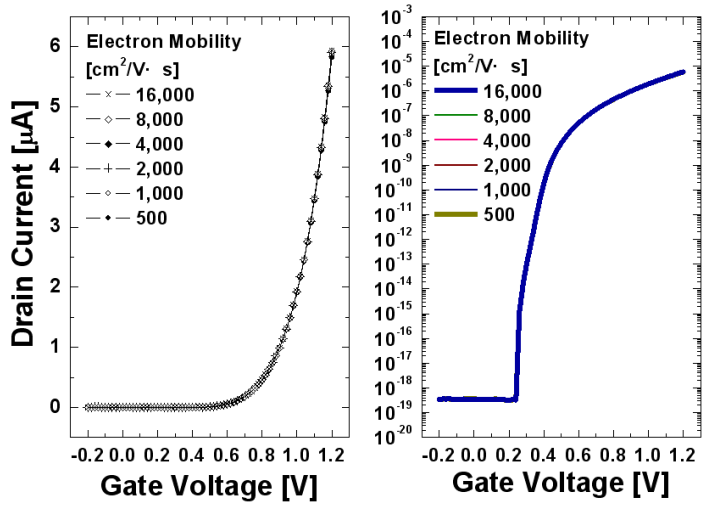
3 Simulation results

There would be change in I_{on} in accordance with the variation on μ_n in the regime that where the TFET device is governed by DD mechanism. On the other hand, I_{on} would not vary with voltage or channel length if tunneling plays a predominant role in driving I_{on}. We could trace the V_{GS} where the boundary between two mechanisms, tunneling and DD, is formed and identify the limiting channel length where DD begins to emerge.

Fig. 1 (a) shows the I_D-V_{GS} curves of a Si nanowire TFET with a channel length of 250 nm. It is observed that I_{on} is significantly varied by change in μ_n (left, linear scale) but the deviation occurs above a voltage point where



(a)



(b)

Fig. 1. Transfer characteristics in linear (left) and logarithmic (right) scales for device with channel lengths of (a) 250 nm and (b) 30 nm. Here, $V_{DS} = 0.9$ V.

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the DD comes into effect (right, logarithmic scale). μ_n was changed from 500 to 16,000 $\mathrm{cm}^2/\mathrm{V{\cdot}s}$ as can be seen in the legends. However, when the channel length is highly scaled down to 30 nm (Fig. 1 (b)), there is no hump at which I_{on} splits by μ_n values. To quantify the splitting, V_{GS} where the maximum upward curvature occurs (V_{MUC}) is defined as:

$$V_{MUC} = V_{GS} \text{ at } \mathrm{Max}[d^2(\log I_D)/dV_{GS}^2] \tag{1}$$

As the curvature at V_{MUC} and the dependence of I_{on} on μ_n get larger, the current splitting becomes more remarkable. Thus, the product of these two terms can be formulated as degree of splitting (DOS) for the quantitative evaluation as follows:

$$DOS = (dI_{on}/d\mu_n) \cdot [d^2(\log I_D)/dV_{GS}^2]|_{V_{GS}=V_{MUC}} \tag{2}$$

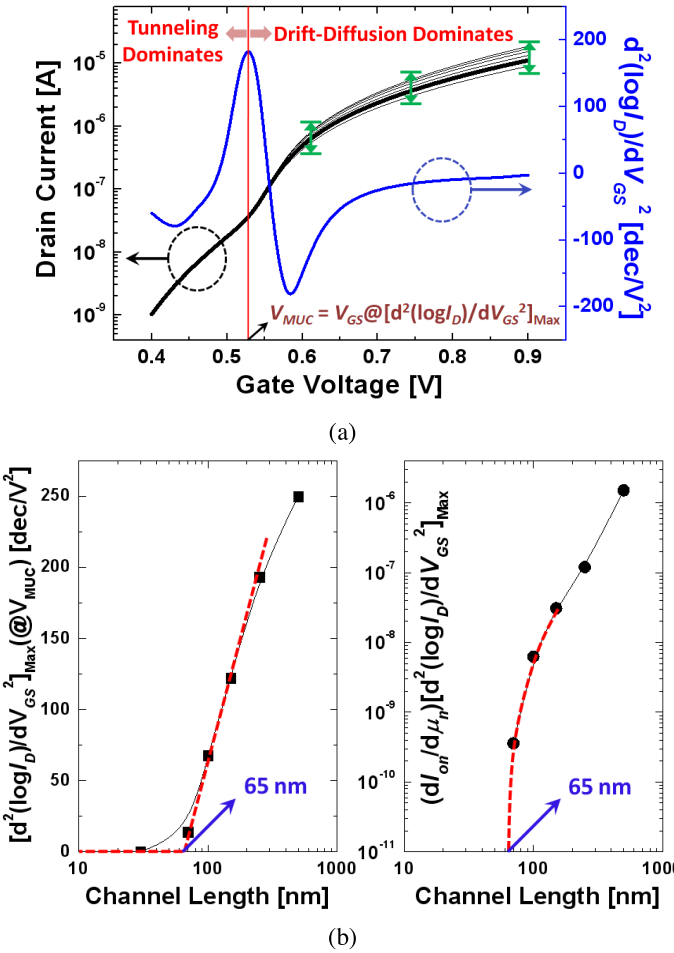

Fig. 2. Qualitative analyses. (a) Evaluating functions. (b) Maximum second derivatives (left) and DOS (right) ($V_{DS} = 0.9\,\mathrm{V}$, $\mu_n = 1{,}000\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$).

The regions that are mainly governed by different mechanisms are divided by V_{MUC} as shown in Fig. 2 (a), where Eq. (1) and (2) are more illustratively defined. Each term of right-hand side of Eq. (2) is a function

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of channel length. It shows a monotonic decrease as the device is shrunken. Fig. 2 (b) depicts the maximum second derivatives in the second term in Eq. (2) as the channel length is varied from 500 nm down to 30 nm. Below a certain channel length, there is no hump caused by DD emergence, or equivalently, by μ_n manipulation. Thus, V_{MUC} does not exist until reaching $V_{GS} = 0.9$ V. The second derivative is asymptotically zero under this condition. By an extrapolation, the breaking point in the channel length where $[d^2(\log I_D)/dV_{GS}^2]|_{V_{GS}=V_{MUC}} = 0$ begins to hold is traced to be approximately 65 nm (left). DOS is also plotted as a function of channel length, which confirms that the solid predominance of tunneling is also maintained below 65 nm (right).

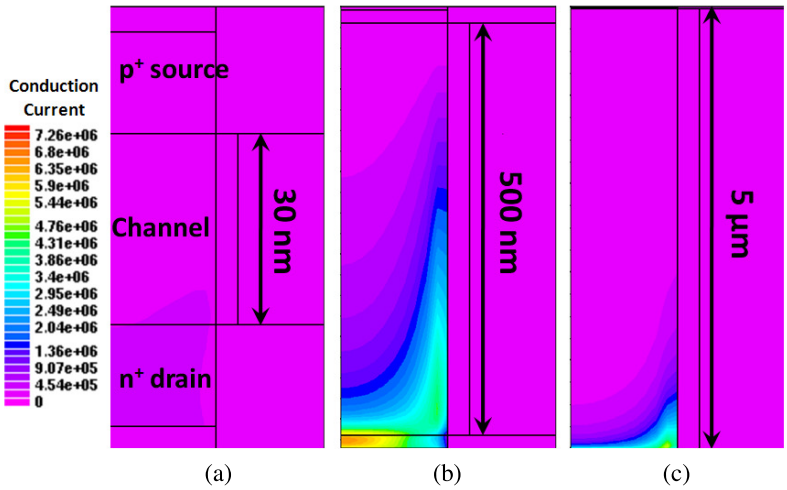

Fig. 3. Graphical analyses on DD components in devices with different channel lengths of (a) 30 nm, (b) 500 nm, and (c) 5 μm at $V_{GS} = V_{DS} = 0.9$ V.

The humps for a long-channel device might not be observed experimentally. Rather, it is a strong evidence for existence of a point distinguishing the regions by current-drive mechanisms of different phases: tunneling-predominance and tunneling combined with DD. When current was driven solely by tunneling in a channel no longer than 70 nm in the simulation, I_{on} was quite low but it increased as the channel gets longer up to 500 nm with enhanced DD. As can be confirmed by Fig. 3 (a) and (b), when DD is brought into driving current, the conduction current density increases. However, when the channel length gets much longer, the TFET device begins to act as a resistor since I_{on} is driven dominantly by DD, by which I_{on} monotonically decreases. Fig. 3 (c) demonstrates that most of the channel region of a very long-channel device is seen as a resistor and degrades I_{on}.

4 Conclusion

In this work, the upper limit in channel length of a Si TFET in a nanowire structure has been proven to be approximately 65 nm. Knowing the existence of length limitation and a method to identify it would be helpful in designing

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a Si nanowire TFET device with either higher current drivability or less sensitiveness to length.

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