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A 2-bit/step SAR ADC structure with one radix-4 DAC

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Abstract: In this letter, a high speed compact structure for 2-bit/step successive approximation (SAR) ADC is presented. Using modified algorithm yields to a simple radix-4 DAC with half bit and a resolution independent Reference Generator unit in the proposed design. This in term caused to extend the resolution of SAR ADC structure for double bit resolutions. An 8-bit SAR ADC is implemented and simulated based on the proposed structure in 300 MHz clock frequency and 50 MS/s sampling rate. The target design has SNDR = 43 dB and SFDR = 52 dB for f_{in} = 4 MHz at 50 Ms/s. The achieved power consumption at this sampling rate is 1.04 mW and the Figure of Merits of proposed design will be 175 fJ/Conversion-step.

Keywords: successive approximation, 2-bit/step SAR ADC, radix-4 DAC
Classification: Electron devices, circuits, and systems

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1 Introduction

Binary search is an approximation algorithm in conventional SAR ADC, where requires to N clock cycles for conversion. Therefore, the use of SAR architecture is mainly limited to mid-range frequency applications. Because

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of small chip area and low power consumption advantages of SAR ADC, recently, designers focused to reconstruct the conventional structure for overcoming the conversion rate problem.

One solution to speed up the SAR ADC is the M-bit ($M > 1$) extraction in each clock cycle. It may increase the speed of ADC by factor M, but $2^M - 1$ comparators are required, which causes to increase on the chip area and power consumption for $M > 3$ and degrade the linearity of ADC due to comparators offset and mismatch. The recent approach is the resolving two bits in each clock cycle in SAR ADC conversion procedure [1, 2, 3, 4]; thereby the conversion rate of SAR ADC by this solution is increased two times faster. The main drawbacks of the known [1, 2, 3, 4] 2-bit/step SAR ADC are the big and complex structures with several DAC networks in [1, 2] and multiplexers in [3] or the thermal noise and process variation sensitive comparators design in [4], which limits them to only low-bit resolution applications.

In the present letter, a new compact structure of SAR ADC is introduced with a modified 2-bit/step algorithm. The proposed architecture consists of only one small N/2-bit radix-4 DAC and a novel resolution independent Reference Generator. Due to using the half-resolution radix-4 DAC, the new design can be used in a higher range of resolutions and because of using 2-bit/step algorithm this structure is two times faster than conventional SAR ADCs.

2 Proposed SAR ADC architecture

The architecture overview of proposed SAR ADC is shown in Fig. 1 (a). This structure consists of three comparators and one sample and hold (S/H) circuit like to other structure designs based on conventional 2-bit/step algorithm. The outputs of comparators are decoded in 2-bit digital binary code by Thermometer to Binary decoder. The internal DAC with radix 4 has N/2 bits resolution where N is the SAR ADC output resolution. Control logic unit is designed by $N + N/2$ flip-flops for control and final output registers, which results in N/2 flip-flops less than the conventional SAR ADC's control logic unit. The Reference Generator is used for preparing the reference voltages of comparators in each search state. This unit consists of three analog adders, one simple 4-input analog multiplexer and one internal Sample and Hold circuit.

2.1 DAC radix-4

The previous 2-bit/step designs [1, 3] have two or more full-scaled internal DACs, while the proposed SAR ADC comes with one simple N/2-bit radix-4 DAC as modeled in Fig. 1 (b). Therefore, it has small chip area penalty in the capacitive array implementation and the mismatch error between internal elements is reduced. All inputs of DAC in proposed design are coded to "One-Hot code", so, it can be specified DAC for this code, which doesn't need to "all of input weights were active" and stay "not connected to others" or "sleep mode". Therefore, the activity factor of dynamic power minimized and

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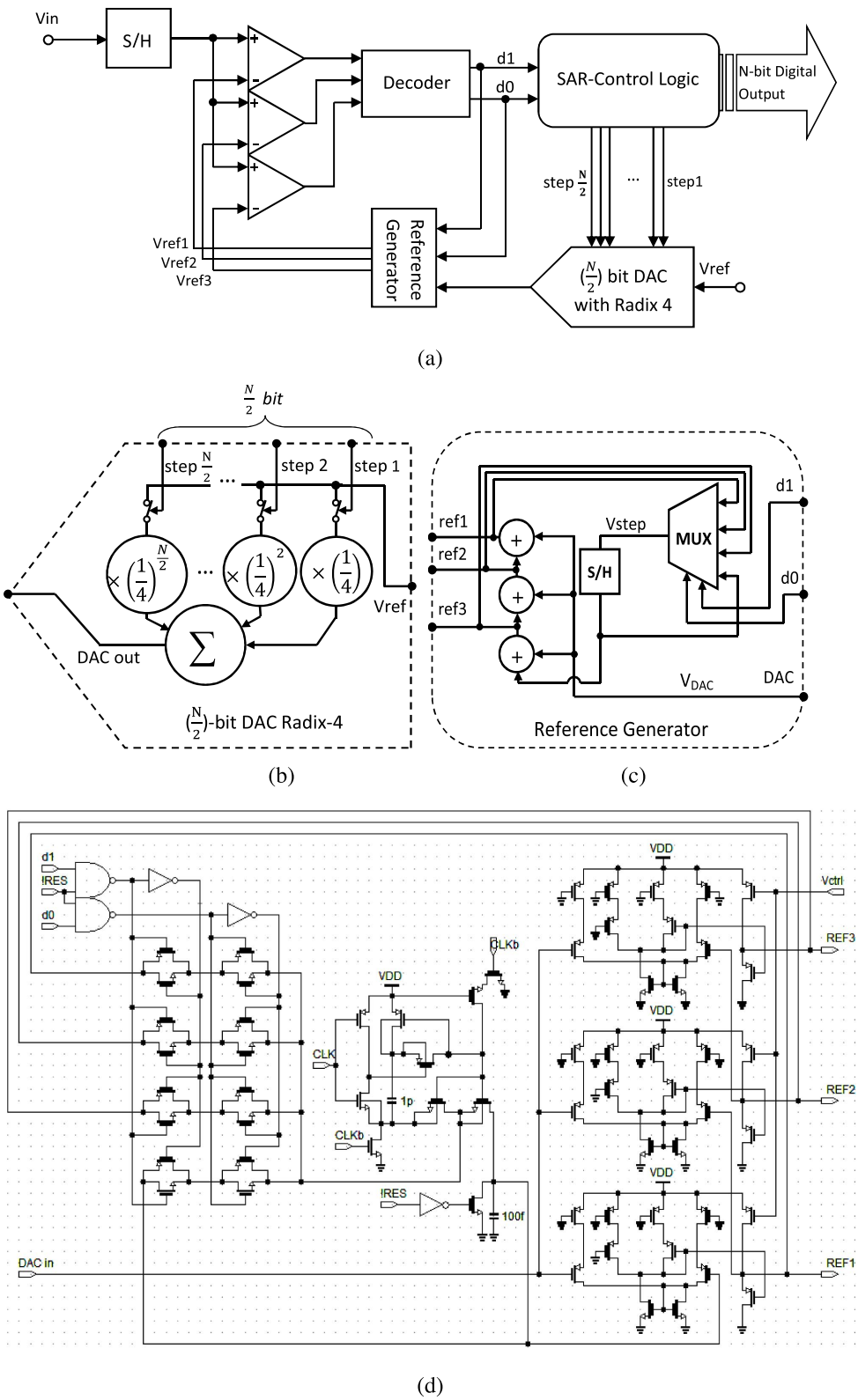

Fig. 1. Proposed 2-bit per step SAR ADC architecture: (a) Global structure (b) N/2-bit DAC with radix-4 (c) Reference Generator (d) Reference Generator Internal Circuit

specified DAC can be "power aware". In the other word, for iteration step 'i', only one input port (i) of DAC is valid and used. Therefore, other capacitors are not required to remain charged and total charge and power consumption

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of proposed DAC are decreased. Also, when the all input weights aren't active in the same time, so, all weights mismatches will be not affected on the output of proposed DAC at the same time. Moreover, the linearity parameters INL and DNL will be improved. Finally, based on input location, a voltage with value of ($V_{ref}/4^i$) is sent to Reference Generator.

2.2 Reference generator

The general conceptual model of the Reference Generator unit is illustrated in Fig. 1 (c). Based on Fig. 1 (c) reference voltages $ref_1(i)$, $ref_2(i)$ and $ref_3(i)$ are generated in each iteration state 'i' by V_{step} and V_{DAC} of previous state. The V_{step} is the output of the analog multiplexer and in each state, MUX selects one of its inputs according to two bits binary address of $d_1d_0(i)$ produced by decoder unit.

Since, the output of MUX is buffered by another sample and hold (S/H) so, during the operation of MUX, a direct combinational loop between output and input of MUX is being prohibited. The V_{step} generated by previous step is held by S/H circuit as a basis for new reference voltages generation.

Fig. 1 (d) shows the circuit implementation of proposed Reference Generator unit which includes one analog multiplexer (MUX) and track and hold circuit and three DC-matched analog adders. MUX is an array of analog switches based on Transmission-Gates structure in Fig. 1 (d). The two bit binary inputs address are encoded in One-Hot code array, and just one switch line corresponding to input address is turned on.

The reference Generator unit is "resolution independent". In the other word, for all output resolution range of SAR ADC for e.g. between 6-bit to 24-bit, the number of switches and adders of proposed design will stay constant and without considerable changes, therefore for all resolution range, the chip area variance of this unit will be neglected. For example, in the proposed circuital implementation of Reference Generator unit which shown in Fig. 1 (d), only 74 transistors used for this structure, so, for all resolution range of proposed 2-bit/step SAR architecture, between 6-bit to 24-bit output resolution, its Reference Generator unit implemented by only 74 transistors with accurate sizes.

Therefore, in the comparison with other works [1, 2, 3, 4], our proposed 2-bit/step SAR ADC structure hast more compact structure, because it used only "one DAC" with "radix-4" with "half resolution" and small control logic unit with N/2 flip-flops less than conventional architecture and in the other side, its Reference Generator is "resolution independent" and its transistor counts will be constant for all resolution range.

2.3 Timing considerations

The timing metric in the proposed structure for 8-bit SAR ADC is shown in Fig. 2. For a reasonable reliability, the voltage V_{DAC} must be settled and reference voltages must be ready before the output flip-flops are triggered on. For this purpose, at the start of conversion, the V_{DAC} is settled through half cycle of a clock. Furthermore, the input flip-flops of MUX select lines and

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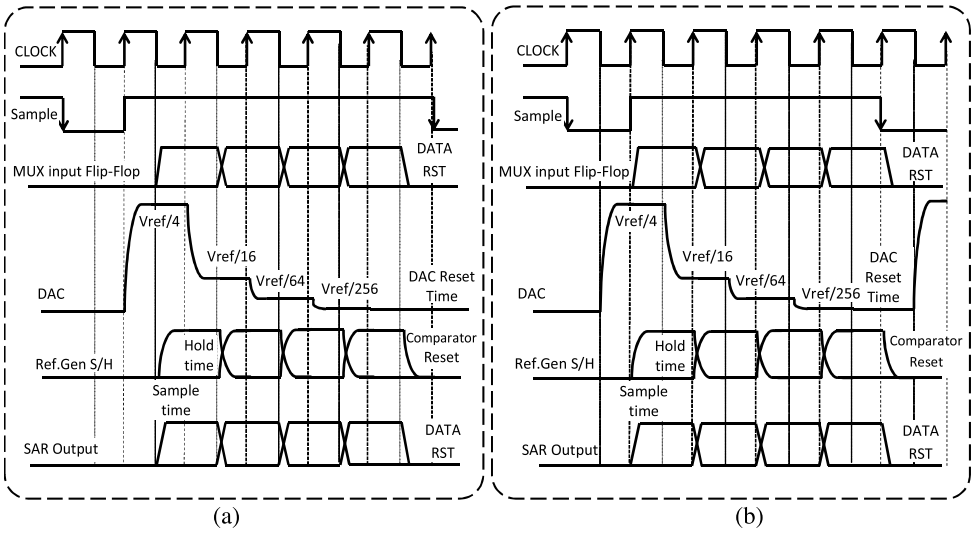

Fig. 2. Conversion map of proposed SAR ADC: (a) one extra clock cycle required for validity of V_{DAC} at start of conversion. (b) DAC is prepared before starting the conversion in half of cycle of sampling time; extra clock cycle will be removed

the output registers are triggered by negative edge of a clock, which is shown in Fig. 2 (a). By each trigger, the sample and hold of Reference Generator samples from new output of MUX and hold it so that the new voltage of V_{DAC} settles. When the new V_{step} and new V_{DAC} are stable, new reference voltages are generated and the comparators compare the input sample with the new references and the decoded results are latched by output registers and MUX address flip-flops at the next step. The total required steps or clock cycles for complete conversion without sampling time is $N/2+1$. Moreover, this timing strategy requires one more clock cycle for preparing the DAC output at the start of conversion. Instead, Fig. 2 (b) introduces the new timing strategy, which doesn't require a one extra clock cycle. In the new strategy, the V_{DAC} is produced and settled in the half cycle of a clock during the sampling time of ADC before the conversion operation is started. Therefore, the extra clock time of conversion will be vanished.

3 Proposed algorithm

We suppose that the "S[n]" is the sampled input of the analog input "f(t)" with the sampling period "T" which is achieved by Eq. (1) where "τ" is the period of the system clock. Required steps for approximating the sampled input are indicated by "α" which consists of the conversion operation step and "k" extra steps for sampling, offset calibration and internal blocks preparing.

$$S(n) = f(nT) \quad n = 1, 2, 3 \ldots \quad \text{“}n\text{” is the sample sequence's index}$$
$$f_{sample} = \frac{1}{T}, \quad T = \alpha\tau, \quad \tau = \frac{1}{f_{clk}}, \quad \alpha = \frac{N_{res}}{2} + k \tag{1}$$

In each iteration step 'i', the parameters V_{step} and V_{DAC} as well as reference voltages will be updated, therefore each parameter in the specified state

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must be indexed by 'i'. The V_{DAC} provides the required voltage for generating references and achieves in each search progress by dividing the previous state value of V_{DAC} by 4. Alternatively, it can be calculated in the state 'i' by dividing the total system reference voltage V_{ref} on 4^i without need to the previous of V_{DAC}, This is formulated in Eq. (2). It must be noticed that the total system reference is equal with the full scale range of ADC.

$$V_{DAC}(i) = V_{ref} \times 4^{-i} \quad \text{i: } 1,2,3\ldots.(\alpha - \text{k}), \quad V_{ref} = V_{FS} \tag{2}$$

Regularly, The parameter V_{step}(i) is calculated with previous iteration 'i-1' and dictates which sub-interval in state 'i-1' must be selected as a search region in step 'i'. Upon the comparison completion among input sample and reference voltages $ref_1(i)$, $ref_2(i)$ and $ref_3(i)$ in each state 'i', two digital bits d_1d_0(i) are resolved according to Eq. (3).

$$d_1d_0(i) = \begin{cases} 11 & S(n) > ref_1(i),\ ref_2(i),\ ref_3(i) \\ 10 & S(n) > ref_2(i),\ ref_3(i) \text{ and } S(n) < ref_1(i) \\ 01 & S(n) > ref_3(i) \text{ and } S(n) < ref_1(i),\ ref_2(i) \\ 00 & S(n) < ref_1(i),\ ref_2(i),\ ref_3(i) \end{cases} \tag{3}$$

Indeed, d_1d_0(i) determines which reference voltages or previous value of V_{step} can be selected as next value of V_{step} for the next search progress; in other word, the V_{step}(i) is multiplexed between references voltages on step 'i' and previous state V_{step}(i-1) which addressed by 2-bit digital input d_1d_0(i) in each state. So, V_{step} can be written as a multiplex function in Eq. (4):

$$V_{Step}(i) = d_1d_0ref_1(i-1) + d_1\bar{d}_0ref_2(i-1) + \bar{d}_1d_0ref_3(i-1) + \bar{d}_1\bar{d}_0V_{Step}(i-1) \tag{4}$$

The reference voltages are also reproduced according to values of V_{DAC}(i) and V_{step}(i) in each search progress 'i' which are showed in Eq. (5). The V_{DAC} determines the voltage difference between new reference voltages and V_{step} indicates the base voltage for generating them in new search step to determine with previous values of references according to Eq. (4).

$$\begin{aligned} ref_3(i) &= V_{DAC}(i) + V_{Step}(i) \\ ref_2(i) &= ref_3(i) + V_{DAC}(i) \\ ref_1(i) &= ref_2(i) + V_{DAC}(i) \end{aligned} \tag{5}$$

The digital output of SAR ADC is an array of b_j bits that set in two bits of it by d_1d_0(i) in each search state 'i', is shown in Eq. (6).

$$\begin{aligned} OUT_{Digital} &= (b_1b_2b_3b_4\ldots b_{N_{res}-1}b_{N_{res}}) \\ OUT_{Digital} &= b_1 \times 2^{N_{res}-1} + b_2 \times 2^{N_{res}-2} + b_3 \times 2^{N_{res}-3} + \ldots + b_{N_{res}-1} \times 2 \\ &\quad + b_{N_{res}} \\ d_1d_0(i) = b_{2i-1}b_{2i} &\Rightarrow b_j = \begin{cases} d_1\left(\dfrac{j+1}{2}\right) & \text{j: odd} \\ d_0\left(\dfrac{j}{2}\right) & \text{j: even} \end{cases} \\ \text{i} &= 1,2,3\ldots\frac{\text{N}_{\text{res}}}{2},\ \text{j} = 1,2,3\ldots N_{\text{res}} \end{aligned} \tag{6}$$

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The final output in terms of $d_1(i)$ and $d_0(i)$ is shown in Eq. (7):

$$OUT_{Digital} = (d_1(1)d_0(1)d_1(2)d_0(2)\ldots d_1(\alpha-k)d_0(\alpha-k))_{(\alpha-k)=\frac{N_{res}}{2}} \quad (7)$$

4 Simulation and performance

The circuit of an 8-bit resolution ADC based on the architecture of the proposed SAR ADC is implemented in 90 nm 1P4M UMC technology 1 volt power supply and simulated by Hspice at $f_{CLK} = 300$ MHz and $f_s = 50$ MS/s.

We expect from our proposed design that due to using half resolution small DAC with lower mismatch errors, the linearity parameters INL and DNL are be improved but offset difference of three comparators can create some mismatches which affected on proposed ADC linearity parameters. It is a common problem in the presented works for 2-bit/step algorithm based design in [1, 2, 3]. However, the achieved static linearity parameters are $-0.8\text{LSB} < \text{INL} < 1.5\text{LSB}$ and $-1\text{LSB} < \text{DNL} < +0.99\text{LSB}$ which shows in Fig. 3 (a).

At the input frequency $f_{in} = 4$ MHz and 50 MS/s sampling frequency, the SFDR = 52 dB and SNDR = 43 dB are achieved. Therefore, the effective number of bits (ENOB) will be 6.9 bit based on this equation

$$ENOB = \frac{SNDR - 1.76}{6.02} = \frac{43 - 1.76}{6.02} = 6.9\,bit \quad (8)$$

Proposed design has low power consumption. The dissipated power of simulated circuit at 1volt supply and 50 MS/s sampling frequency is about 1.04 mW which is a good power factor in this sampling rate. In Fig. 3 (c) the percent of power usage of each sub-unit is shown and describes that the most power of ADC (about 68% of total power) is consumed by analog comparators. Based on ADC power dissipation and ENOB and its bandwidth the Figure of Merit will be achieved about 175 fj/conversion-step based on this formula:

$$FoM = \frac{P}{2 \times B \times 2^{ENODB}} = \frac{1.04 \times 10^{-3}}{2 \times 25 \times 10^6 \times 2^{6.9}} = 175\,fJ/C - step \quad (9)$$

5 Conclusion

A new design of SAR ADC based on the use of modified 2-bit/step algorithm is presented. Based on the proposed algorithm, the small and compact structure of new 2-bit/step SAR ADC is introduced with one small N/2 bit DAC radix-4 and a novel Reference Generator unit. Proposed structure has small control logic unit with N/2 fewer number counts of flip-flops. Therefore, proposed design is suitable for high speed and high resolution applications.

Because of using one DAC N/2 bit with radix-4, the total capacity of proposed architecture is less than the similar counterpart designs, which is another effective factor for high speed capability and resolution extendibility of this design. The individual feature of proposed Reference Generator as a very small, compact and low complexity architecture can be stressed on high frequency range extension of the 2-bit/step SAR ADC. Another major factor

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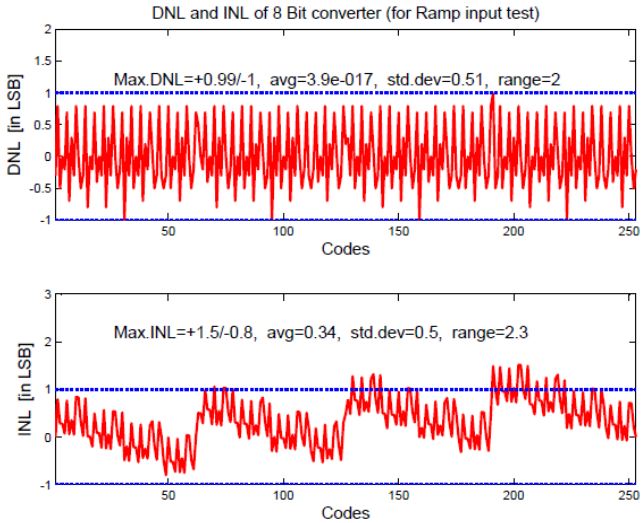
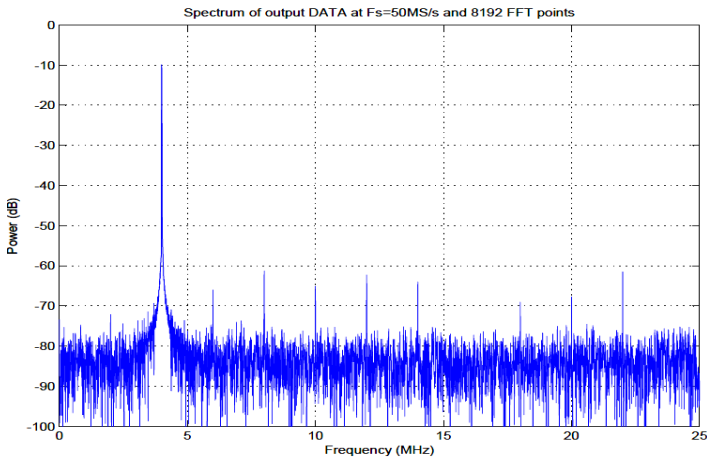


(a)



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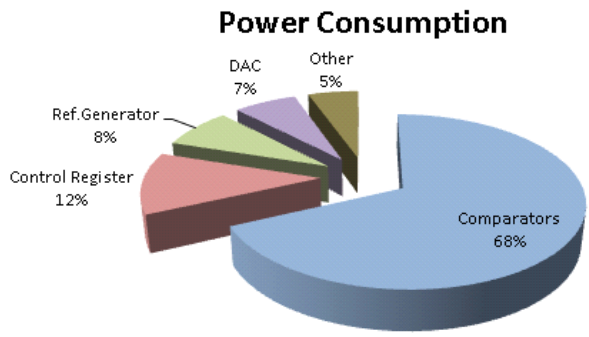

(c)

Fig. 3. Simulation of 8-bit proposed 2-bit/step SAR ADC: (a) INL and DNL results (b) SNDR and SFDR at $f_{CLK} = 300\,\text{MHz}$, $f_s = 50\,\text{MS/s}$ and $f_{in} = 4\,\text{MHz}$ (c) Power Consumption distribution diagram of different units

of this unit is its resolution independent operation, which gains less limitation on resolution of the target system, opposite to the known counterpart structures.

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The proposed design works between "SAR ADCs family" and "Flash ADCs family", so, this design has better performance than Conventional SAR ADCs and better power consumption and chip area than Flash ADCs.

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