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A switchless reconfigurable transformer CMOS power amplifier

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Abstract: A reconfigurable dual-mode monolithic transformer is presented, which avoids the use of switches for load adaptation. The number of turns of primary winding is varied according to power mode control so that load impedance can be optimized for each operation. The concept of the reconfigurable transformer is demonstrated through the design of a multi-mode power amplifier using bulk CMOS process. Electromagnetic and circuit simulation results validate the operation and performance improvements using the proposed transformer. Low power efficiency at 18 dBm is substantially improved from 5.5% to 17.5% using multi-mode control.

Keywords: power amplifier (PA), transformer, passive efficiency, impedance transformation, low-power mode

Classification: Integrated circuits

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1 Introduction

To extend battery lifetime, high efficiency in the low-power (LP) level is required because PAs are mostly operated at LP level rather than the peak output power according to the probability distribution function of the transmitted power. Accordingly, there has been increasing interest in a multi-mode operation to increase LP efficiency. The load impedance control to a higher value is essential to improve LP efficiency [1, 2]. Among reported methods for multi-mode operation, a transformer-based method is an attractive solution, because it provides impedance transformation and converts a differential signal into a single-ended signal simultaneously.

A switched variable transformer has been introduced in [3], as shown in Fig. 1 (a). However, the loss induced by the additional switches degrades the

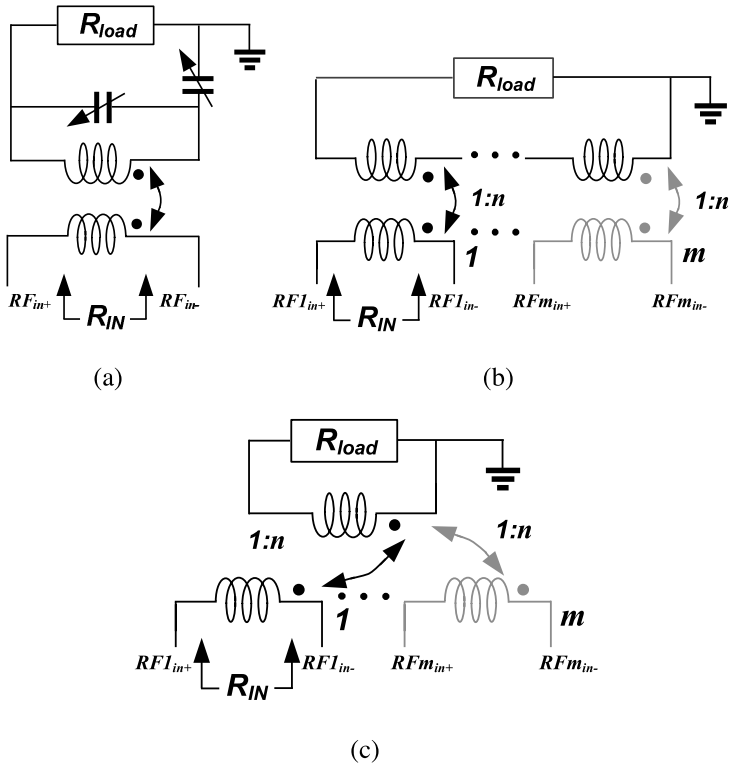

Fig. 1. (a) Switched variable transformer (b) series power combining transformer (c) parallel power combining transformer

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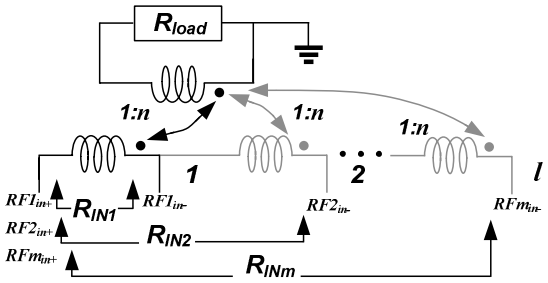

Fig. 2. Proposed reconfigurable transformer

efficiency improvement in the LP mode. Another challenge is that switch devices need to sustain high voltage swings to avoid a breakdown incidence. On the other hand, multiple primary windings can be combined in series or parallel so that multiple primary windings can be discretely controlled at LP mode [4, 5, 6]. However, these types of the transformers are optimized mainly for high-power (HP) mode. In series power combining transformer, shown in Fig. 1 (b), the coupling between primary and secondary windings is weak in LP mode, because the part of secondary winding does not participate in the coupling when nearby primary winding is turned off. In parallel power combining transformer, shown in Fig. 1 (c), the provided load impedance for each device is calculated as follows [5, 6]:

$$R_{INm} = m\left(\frac{1}{n}\right)^2 R_{load} \tag{1}$$

When some primary windings are turned off in LP mode, m is decreased and the provided load impedance is also decreased, resulting in non-optimal operation.

This letter proposes a reconfigurable transformer, shown in Fig. 2, which is optimized both for low- and high-power modes without any switches.

2 Proposed switchless reconfigurable transformer

The proposed reconfigurable transformer consists of the number of effective l segment with relation $l : n$ [l: number of segments in primary winding, n: number of secondary turns]. Therefore, the impedance looking into the transformer input is calculated as follows:

$$R_{INl} = \left(\frac{l}{n}\right)^2 R_{load} \tag{2}$$

For HP mode operation, only the first pair amplifier ($RF1_{IN+}$ and $RF1_{IN-}$) works and the other pairs are turned off, making $l = 1$ and providing low impedance. The provided load impedance, R_{IN1}, is $(1/n)^2 R_{load}$. For LP mode operation, higher l ($l > 1$) will be selected to provide higher load impedance, resulting in efficiency improvement of LP mode.

The provided load impedance, R_{INl}, will be higher from (2). Fig. 3 (a) and (b) show an exemplary physical layout and the equivalent circuit model. Lateral transformer structure has been adopted for the implementation of the

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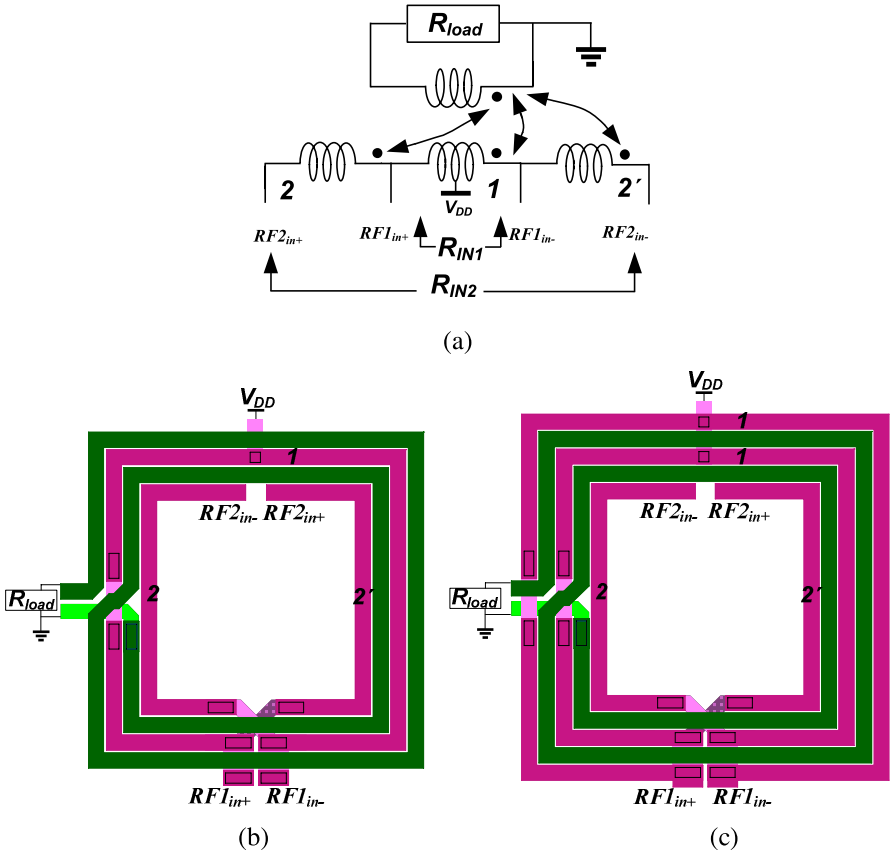

Fig. 3. (a) Circuit diagram (b) layout, and (c) modified layout of the reconfigurable transformer

reconfigurable transformer because only a single thick metal layer is available in a typical bulk CMOS process. The physical length of primary winding in HP mode is between $RF1_{IN+}$ and $RF1_{IN-}$ and is located between each turn of the secondary winding to maximize the coupling between primary and secondary windings. For LP operation, an additional turn is extended at the end of primary winding considering symmetrical geometry and coupling magnitude. Physical length of primary winding in LP mode is between $RF2_{IN+}$ and $RF2_{IN-}$. Therefore, equivalent input impedance looking into transformer assuming ideal transformer is 12.5 Ω in HP mode, while it is 50 Ω in LP mode. Transformer efficiency performance can be optimized for both mode operations. In addition, the parallel segment method in the first segment of the primary winding is adopted to improve efficiency performance [7], as shown in Fig. 3 (c). The parasitic resistance of the first segment is decreased and the power loss dissipated in the primary winding can be minimized.

3 Design of a switchless reconfigurable transformer CMOS PA

To verify the feasibility of the designed reconfigurable transformer, the dual-mode PA is designed with a 0.18-μm CMOS process. It is composed of three parts, which denote an input balun transformer, a power transistor, and a reconfigurable output transformer, as shown in Fig. 4 (a). The transformer

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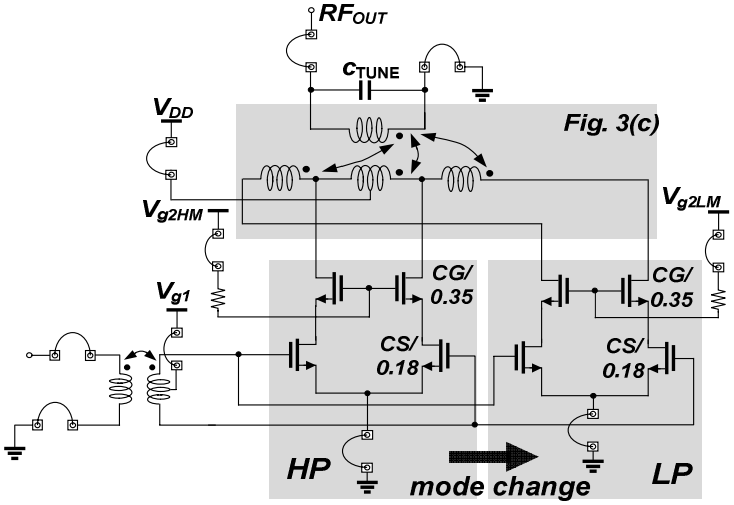
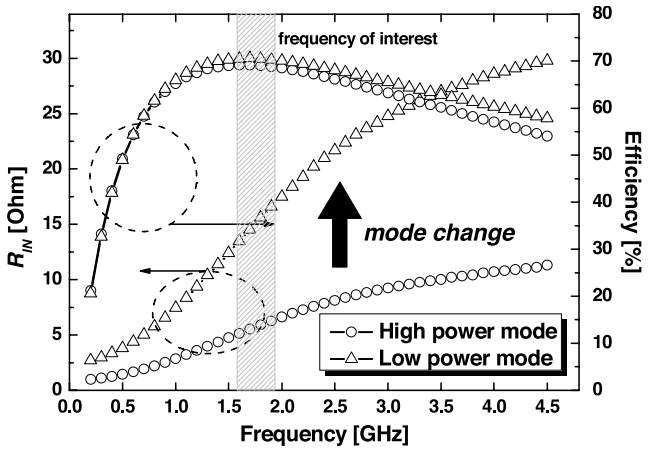
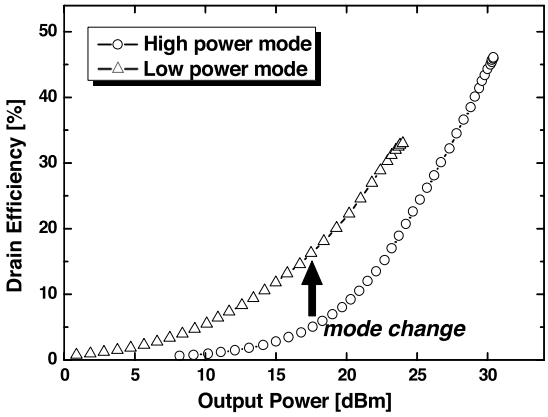


(a)



(b)



(c)

Fig. 4. (a) Schematic of the reconfigurable transformer CMOS power amplifier, (b) EM simulation results of the reconfigurable transformer and (c) simulated drain efficiency of the reconfigurable transformer CMOS power amplifier

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is also designed in a standard 0.18-μm CMOS process with an *Al* top-metal thickness of 2.34 μm. The PA core was realized with two differential pairs for HP and LP modes. Cascode topology is adopted to avoid excessive voltage stress on each device. Each cascode stage is a stack 0.35 μm thick-oxide devices for common-gate (CG) stages, and 0.18 μm thin-oxide devices for common-source (CS) stage, distributing the voltage stress. The total gate widths of CS and CG in HP are 6144 μm, and 8192 μm, while those in LP are 768 μm, and 1024 μm, respectively. With a supply voltage of 3.3 V, the gate bias voltage of the CS and the CG device are set to 0.6 and 3.3 V, respectively, for both mode operations. The bond wired inductances are included in a total circuit simulation using Ansoft HFSS. The outer dimensions of the transformer are adjusted considering the frequency band of interest, resulting in 0.54 mm^2 at 1.8 GHz. Only the top metal layer was used for the winding while the underpass connections were realized with the low thin metal layers. Full wave electromagnetic simulations have been performed using Agilent Momentum. The same tools and simulation environments in the previous works [5, 6, 7] are used in this work. Fixed MIM capacitor (C_{TUNE}) of 1.9 pF is put on the secondary side to resonate out the secondary inductance to maximize efficiency. The optimized simulated transformer insertion loss of 1.61 dB (69%) for HP mode and 1.52 dB (70.5%) for LP mode at 1.8 GHz, respectively, is shown in Fig. 4 (b). The 50-Ω load impedance is transformed into 5.89 Ω in HP mode at 1.8 GHz. While it is transformed into high value 15.6 Ω in LP mode to improve efficiency. HP and LP differential pairs are selectively chosen for each mode. The drain efficiencies of both modes with 1.8-GHz single-tone signal are shown in Fig. 4 (c). The saturation output power (Psat) of the HP and LP mode are 30.4 dBm and 24 dBm, respectively. The drain efficiencies at Psat are 46.1% in HP mode and 33.4% in LP mode, respectively. When the output power is reduced simply by reducing input drive, the efficiency is degraded to 5.5% at 18 dBm in HP mode. However, it is possible to improve the backed-off efficiency to about 17.5%. The introduced LP mode improves the efficiency significantly in the low-power region. The efficiency improvement in the back-off range can be covered between 10 and 20 dBm output power. The simulation results presented in Fig. 4 (c) demonstrate the effectiveness of the proposed reconfigurable transformer.

4 Conclusions

A switchless reconfigurable transformer is presented to improve LP mode efficiency and the effectiveness of the proposed transformer is validated in electromagnetic and circuit simulations. The impedance ratio between HP and LP mode is about 1 : 3 and the maximum efficiency improvement in the back-off region is more than 10%. The reconfigurable transformer will be a suitable component to achieve a full integration of compact multi-mode PA.

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