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Switching activity reduction for scan-based BIST using weighted scan input data

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Abstract: This paper proposes a new scan-based BIST scheme that implements weighted random pattern testing by loading different scan input data into scan chains with proper probabilities. These scan input data include previous scan values into the scan chains, pseudorandom data generated by test pattern generator, test responses collected by the scan chains, and the complement of test responses. Due to increasing the correlation among adjacent test stimulus bits, the proposed method decreases the switching activity during scan shift. Meanwhile our method applies the four kinds of test data with different probabilities to maximize test effectiveness. A greedy procedure is proposed to select the proper probabilities that the four kinds of data are selected for each scan chain. When comparing with an existing method called LT-RTPG, experimental results for larger benchmark circuits of ISCSAS89 show that the proposed method can significantly reduce shift test power while providing higher fault coverage.

Keywords: scan-based BIST, testability, test power, weighted random testing, scan input

Classification: Integrated circuits

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1 Introduction

Build-In Self-Test (BIST) [1] is commonly used in integrated circuit (IC) testing since the methodology does not need to store pre-computed test patterns in tester and can be built with little area overhead. In BIST, pseudorandom test stimuli are generated by test pattern generator (TPG) such as linear feedback shift register, and test responses are compacted by multiple input shift register (MISR) for comparison. Due to the low correlation between consecutive random patterns generated by a TPG, it causes extremely higher switching activity during self-test than that during normal operation [1]. In scan-based BIST, this issue seems to be particularly striking. Higher switching activity might cause IR-drop resulting in undesired yield loss, and even cause hot spots damaging the circuit under test (CUT) [2].

Recently, many techniques are developed to reduce switching activity of scan-based BIST, especially for the scan shift power. Methods proposed in [3, 4] insert extra gates to freeze the outputs of the scan cells during scan shift. These extra logics may degrade circuit performance. Huang and Lee [5] use token scan chain to reduce switching activity during scan testing. Since each token scan cell is comprised of two flip-flops and additional logic gates, hardware overhead can be significant. M. Elm et al. [6] cluster the scan chains into multiple groups and shift power reduction is achieved by limiting scan shift to a portion of scan chains. The method presented in [7] is based on a modified clock scheme for TPG and the clock tree feeding the TPG. Two LFSRs are used to generate pseudorandom test patterns achieving shift power reduction, especially in clock tree. The techniques proposed in [8, 9] apply highly correlated test stimulus bits to adjacent scan cells in each scan chain resulting in the significant reduction of shifting transitions. However, increasing the correlation among adjacent scan cells degrades the uniformity

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of distribution and may decrease fault coverage for a given test length.

In this paper, we propose a new scan-based BIST scheme. The scheme inherits the advantage of the technique that applies highly correlated test stimulus bits among adjacent scan cells for shift power reduction, and meanwhile improves the tradeoff between shift power reduction and fault coverage loss, i.e., reduces shift power while avoiding the significant fault coverage loss. In the proposed scheme, the scan input data of each scan chain is loaded through a multiplexer that selects one of the four data sources: previous scan value into the scan chain, TPG, test responses collected by the scan chain, and inverted test responses. By assigning proper probabilities to the control signals of the multiplexers in separate scan chains, shift power reduction is achieved on the premise of high test effectiveness.

2 The proposed test scheme

We present a novel scan-based BIST scheme shown in Fig. 1 (a). In this scheme, the scan cells are divided into N scan chains. At the scan-in port of each scan chain there is a multiplexer that selects one from four data sources at each clock cycle. The multiplexer has four inputs which are connected to the output of the flip-flop adjacent to scan-in port, TPG output, the output of the flip-flop adjacent to scan-out port and the inverted output of the flip-flop adjacent to scan-out port respectively. The multiplexer has 2-bit control

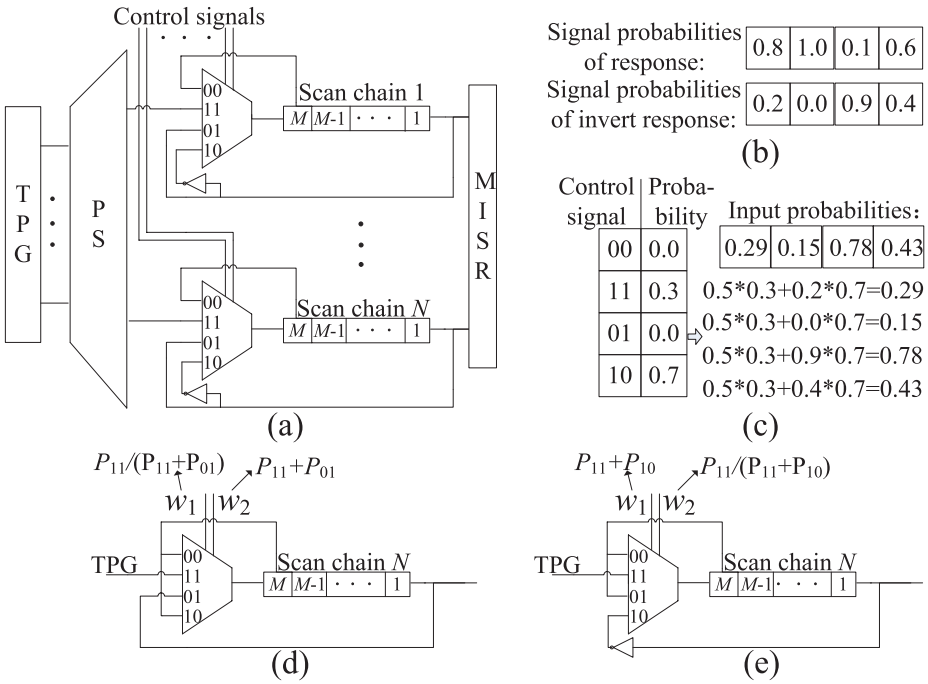

Fig. 1. The proposed test scheme. (a) The architecture of the proposed test scheme. (b) The signal probabilities of test response and invert response in the example. (c) Weighted scan input example. (d) The equivalent architecture when $P_{10} = 1$. (e) The equivalent architecture when $P_{01} = 1$.

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signals. When the control signals are 00, 11, 01 and 10, previous scan value into the scan chain, pseudorandom data generated by TPG, test response collected by the scan chain, and the complement of test response are loaded into the scan chain respectively. When the previous scan value is delivered repetitively, test stimulus bits among adjacent scan cells become correlated and thus shift power reduction can be achieved.

Random pattern resistant (RPR) faults which are usually tested by a very small proportion of input patterns have a great impact on test coverage for any given test length. Weighted random pattern testing can be effective for a CUT with a large number of RPR faults [10].

The internal nodes in a circuit including pesudoprimary outputs (PPOs) and primary outputs (POs) usually have a biased signal probability, i.e. their probability being 1(0) may be larger or smaller than 0.5. We implement weighted random pattern testing by properly determining the probabilities that all the scan input data are selected into the scan chains. To make a simple explanation, consider a scan chain containing 4 scan cells. We assume reasonably the probability of pseudorandom data being 1(0) is 0.5. Suppose that the signal probabilities of test responses and their complement being 1 are shown in Fig. 1 (b). If the probabilities of scan control signals being 00, 11, 01 and 10 are 0.0, 0.3, 0.0, and 0.7 respectively. Thus, the input probabilities being 1 of the 4 scan cells are 0.29, 0.15, 0.78, and 0.43 respectively, instead of 0.5, as shown in Fig. 1 (c).

3 Selection of input control signal probabilities

Input control signal probabilities for scan chains, which determine the weighted values of scan inputs, bring a profound impact on test effectiveness. The section will show how to compute the control signal probabilities of scan chains.

Testability for all internal nodes can be estimated based on the controllability/observability programs (COP) measure [11]. The v-controllability $C_v(l)$ measure of a node l is defined as the probability of a randomly selected input pattern setting l to value v. The observability $O(l)$ is defined as the probability of a randomly selected input pattern propagating the value of l to a PO or PPO. The controllability and observability of a node in CUT are related to the weights of inputs.

The signals PPI_j and PPO_j are the PPI and PPO of the j th scan flip-flop in a scan chain from scan out for $j = 1, 2, \ldots, k$. After probabilities P_{00}, P_{11}, P_{01} and P_{10} are assigned to the four kinds of data, the signal probabilities of PPIs can be calculated as follows:

$$C_1(PPI_1) = P_{00} \times C_1(PPO_1) + P_{11} \times 0.5 + P_{01} \times C_1(PPO_1) + P_{10} \times (1 - C_1(PPO_1)) \quad (1)$$

$$C_1(PPI_j) = P_{00} \times C_1(PPI_{j-1}) + P_{11} \times 0.5 + P_{01} \times C_1(PPO_j) + P_{10} \times (1 - C_1(PPO_j)), j = 2, 3, \ldots, M \quad (2)$$

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Signal controllability calculation for other combinational nodes and observability for all combinational nodes is the same as the conventional COP measure [11].

Selection of the probabilities on the input control signals of the scan chains is determined by the following testability cost function [12]:

$$G = \sum_{l/i \in F} \frac{|C_1(l) - C_0(l)|}{O(l)} \tag{3}$$

where l/i represents the stuck-at i ($i \in 0, 1$) fault at line l. In (3), F is the hard-to-detect fault set that determine test length for a given fault coverage. Our method tries to minimize the cost function in (3). Since (2) can be transformed:

$$\begin{aligned} C_1(PPI_j) &= P_{00} \times C_1(PPI_{j-1}) + P_{11} \times 0.5 + P_{01} \times C_1(PPO_j) + P_{10} \\ &\quad \times (1 - C_1(PPO_j)) \\ &= P_{00} \times C_1(PPI_{j-1}) + (P_{11} + 2P_{10}) \times 0.5 + (P_{01} - P_{10}) \\ &\quad \times C_1(PPO_j) \\ &= P_{00} \times C_1(PPI_{j-1}) + (P_{11} + 2P_{01}) \times 0.5 + (P_{10} - P_{01}) \\ &\quad \times (1 - C_1(PPO_j)), j = 2, 3, \ldots, M \end{aligned} \tag{4}$$

So we will construct equivalently the weighted test data with either test responses or the complement of test responses and the other two kinds of data. To reduce test power significantly, we select the value of P_{00} from the set $\{0.5, 0.625, 0.75, 0.875\}$. We set $P_{01} = 0$ or $P_{10} = 0$, and thus $P_{10}(P_{01}) + P_{11} = 1 - P_{00}$. We select the value of $P_{10}(P_{01})$ and P_{11} from the set $\{0, 0.25 * (1 - P_{00}), 0.5 * (1 - P_{00}), 0.75 * (1 - P_{00}), 1 - P_{00}\}$.

Our method assigns the value of P_{00} in advance and determines the probabilities of input control signals for scan-chains one by one to minimize the cost function. The detailed procedure to determine probabilities for control signals is presented in Algorithm 1 in Fig. 2.

Note that controllability calculation for PPOs and PPIs are attached to one another. Initially, controllability of the PPIs of the scan flip-flops is set to 0.5. Iterative testability estimation is used for all nodes based on (1)-(2) and the COP measure [11]. It is found that the testability measures for all nodes become stable very quickly.

Input control signals with different probabilities can be provided by assigning weight to each control bit. To implement easily, if $P_{10} = 0$, we make previous scan value selected when control signals is 00 as well as 10, as shown in Fig. 1 (d). Thus, the weight (w_2) of the second control bit can be calculated as $P_{11} + P_{01}$, i.e. $1 - P_{00}$, and the weight (w_1) of the first bit is $\frac{P_{11}}{P_{11}+P_{01}}$. Similarly, the case that $P_{01} = 0$ is shown in Fig. 1 (e).

4 Experimental results

To analyze the effectiveness of the proposed scheme, experiments are conducted on full scan version of larger ISCAS'89 benchmark circuits. We per-

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Algorithm 1
Determine probabilities of input control signals for the scan chains
{
1) Select a value in {0.5, 0.625, 0.75, 0.875} for P_{00}
2) While the scan chain set $S \neq \Phi$, do
a) Select a scan chain *sc* from *S*, and delete *sc* from *S*.
b) Set P_{01}=0. For each probability combination of P_{10} and P_{11} that satisfy $P_{11}+P_{00}+P_{10}=1$, testability estimation as presented in Section 3 is implemented to evaluate the cost function.
c) Set P_{10}=0. For each probability combination of P_{01} and P_{11} that satisfy $P_{11}+P_{00}+P_{01}=1$, testability estimation as presented in Section 3 is implemented to evaluate the cost function.
d) Select the best probabilities for P_{11} , P_{01} and P_{10} that makes the cost function minimum.
}

Fig. 2. Procedure to determine probabilities of input control signals for the scan chains.

Table I. Experimental results for the proposed scheme and comparision with low power scheme in [8].

Circuit	Length	$P_{00}=0.5$		$P_{00}=0.625$		$P_{00}=0.75$		$P_{00}=0.875$		low power [8]	
		FC%	wsa %red	FC%	wsa %red	FC%	wsa %red	FC%	wsa %red	FC%	wsa %red
S5378	65536	98.83	25	98.26	32	97.72	38	**96.68**	45	96.54	43
S9234	524288	93.30	40	93.16	41	93.03	48	**92.34**	63	90.89	62
S13207	132072	97.97	31	96.48	42	**95.46**	51	**94.98**	53	93.66	45
S15850	132072	96.31	37	96.18	43	95.96	50	95.91	57	94.40	58
S35932	128	89.72	32	89.56	50	88.98	55	**88.47**	56	87.84	56
S38417	132072	95.69	35	95.81	44	**95.68**	56	**95.46**	58	94.99	56
S38584	132072	95.70	39	95.24	45	94.94	54	**94.78**	59	93.35	59
AVG	-	95.36	34.1	94.96	42.4	94.54	50.3	94.09	55.8	93.10	54.1

form fault simulation using "HOPE". The weighted switching activity (WSA) is used to evaluate test power.

Table I shows the fault coverage and WSA reduction results for the proposed scheme compared with the low power scheme in [8]. We set the length of the scan chains as 30. The size of LFSR is set as 40 or 50 which is compatible with [8]. We apply the same numbers of test patterns with [8] for every benchmark circuit, which are shown in the second column. The columns under the heading $P_{00} = 0.5(0.625, 0.75, 0.875)$ show simulation results obtained by the proposed scheme that set $P_{00} = 0.5(0.625, 0.75, 0.875)$. The columns labeled WSA red show the savings in WSA per test clock cycle by using the proposed scheme or the scheme [8] compared with conventional BIST. The columns labeled FC show the fault coverage. The results in Table I show that the proposed scheme can achieve significant power reduction while providing high fault coverage. It is clear that, when achieving the same test power reduction or a little more significant than [8], the proposed method can attain higher fault coverage. For the purpose of view, we mark these data with bold. When considering the area overhead, a MUX gate, an NOT gate per scan chain has negligible impact on chip area.

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5 Conclusion

The technique that increases the correlation among adjacent test stimulus bits in pseudorandom test patterns reduces the shift power significantly, however it often decreases fault coverage. In this paper, we propose a scan-based BIST scheme which delivers four data sources: TPG, test responses, inverted test responses, and previous scan value into the scan chains with different probabilities. The scheme inherits the advantage of the technique that applies highly correlated test stimulus bits among adjacent scan cells for shift power reduction, and meanwhile improves the tradeoff between shift power reduction and fault coverage loss. Experimental results demonstrate the effectiveness of the proposed method.

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