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Overview of emerging semiconductor non-volatile memories

Yoshihisa Fujisaki[a)]

Central Research Laboratory, Hitachi Ltd.,

1–280 Higashikoigakubo, Kokubunji, Tokyo 185–8601, Japan

a) *yoshihisa.fujisaki.fh@hitachi.com*

Abstract: In this article, emerging new semiconductor non-volatile memories are reviewed. We are reaching the integration limit of Flash memories and new types of memories replacing Flash have been actively proposed. Each type of memory is briefly introduced and the possibility of replacing Flash is discussed. FeRAMs, MRAMs, and PCRAMs are already in production and the physics behind the operations and reliabilities are well understood. ReRAMs are now approaching to practical use. However, the operation mechanisms of the other memories have not been understood perfectly. Therefore, it is not fruitful to compare the superiority of each technology at this moment because some innovative idea might enhance a specific technology that happened from time to time.

Keywords: non-volatile memory, flash, FeRAM, MRAM, PCRAM, ReRAM, organic

Classification: Storage technology

References

[1] K. Kim, J. H. Choi, J. Choi, and H. Jeong, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 88, 2005.

[2] A. Fazio, *MRS Bulletin*, vol. 29, p. 814, 2004.

[3] T. M. Kowalick, *Vehicular Technology Conference 2001, Spring*, vol. 4, p. 3037, 2001.

[4] H. Shiga, D. Takashima, S. Shiratake, K. Hoya, T. Miyakawa, R. Ogiwara, R. Fukuda, R. Takizawa, K. Matsuda, F. Matsuoka, Y. Nagadomi, D. Hashimoto, H. Nishimura, T. Hioka, S. Doumae, S. Shimizu, M. Kawano, T. Taguchi, Y. Watanabe, S. Fujii, T. Ozaki, H. Kanaya, Y. Kumura, Y. Shimojo, Y. Yamada, Y. Minami, S. Shuto, K. Yamakawa, S. Yamazaki, I. Kunishima, T. Hamamoto, A. Nitayama, and A. Furuyama, *Dig. Tech. Papers, 2009 IEEE Int. Solid State Circuit Conf.*, p. 464, 2009.

[5] N. Nagel, R. Bruchhaus, K. Hornik, U. Egger, H. Zhuang, H.-O. Joachim, T. Röhr, G. Beitel, T. Ozaki, and I. Kunishima, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 146, 2004.

[6] X. Zhang, M. Takahashi, K. Takeuchi, and S. Sakai, *Int. Conf. on Solid State Devices and Materials (SSDM)*, pp. 975–976, 2011.

[7] Y. Arimoto and H. Ishiwara, *MRS Bulletin*, vol. 29, no. 11, p. 823, 2004.

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[8] Y. Fujisaki and H. Ishiwara, *Mater. Res. Soc. Symp. Proc.*, vol. 830, p. 64, 2005.
[9] G. Grynkewich, J. Åkerman, P. Brown, B. Butcher, R. W. Dave, M. DeHerrera, M. Durlam, B. N. Engel, J. Janesky, S. Pietambaram, N. D. Rizzo, J. M. Slaughter, K. Smith, J. J. Sun, and S. Tehrani, *MRS Bulletin*, vol. 29, no. 11, p. 818, 2004.
[10] T. Sugibayashi, T. Honda, N. Sakimura, K. Nagahara, S. Miura, K. Shimura, K. Tsuji, Y. Fukumoto, H. Honjo, T. Suzuki, Y. Kato, S. Saito, N. Kasai, H. Numata, N. Oshima, R. Nebashi, K. Suemitsu, T. Mukai, K. Mori, S. Fukami, N. Ishiwata, H. Hada, and S. Tahara, *IEICE Technical Report ICD*, vol. 106, no. 2, p. 61, 2006, in Japanese.
[11] K. Miura, T. Kawahara, R. Takemura, J. Hayakawa, S. Ikeda, R. Sasaki, H. Takahashi, H. Matsuoka, and H. Ohno, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 234, 2007.
[12] T. Ishigaki, T. Kawahara, R. Takemura, K. Ono, K. Ito, H. Matsuoka, and H. Ohno, *Proc. Int. Symp. on VLSI Technol.*, Hawaii, p. 47, 2010.
[13] Y. M. Lee, C. Yoshida, K. Tsunoda, S. Umehara, A. Aoki, and T. Sugii, *Proc. Int. Symp. on VLSI Technol.*, Hawaii, p. 49, 2010.
[14] A. Driskill-Smith, S. Watts, V. Nikitin, D. Apalkov, D. Druist, R. Kawakami, X. Tang, X. Luo, A. Ong, and E. Chen, *Proc. Int. Symp. on VLSI Technol.*, Hawaii, p. 51, 2010.
[15] D. C. Worledge, G. Hu, P. L. Trouilloud, D. W. Abraham, S. Brown, M. C. Gaidis, J. Nowark, E. J. O'Sullivan, R. P. Robertazzi, J. Z. Sun, and W. J. Gallagher, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 296, 2010.
[16] S. C. Oh, J. H. Jeong, W. C. Lim, W. J. Kim, Y. H. Kim, H. J. Shin, J. E. Lee, Y. G. Shin, S. Choi, and C. Chung, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 300, 2010.
[17] S. Chung, K.-M. Rho, S.-D. Kim, H.-J. Suh, D.-J. Kim, H.-J. Kim, S.-H. Lee, J.-H. Park, H.-M. Hwang, S.-M. Hwang, J.-Y. Lee, Y.-B. An, J.-U. Yi, Y.-H. Seo, D.-H. Jung, M.-S. Lee, S.-H. Cho, J.-N. Kim, G.-J. Park, G. Jin, A. Driskill-Smith, V. Nikitin, A. Ong, X. Tang, Y. Kim, J.-S. Rho, S.-K. Park, S.-W. Chung, J.-G. Jeong, and S.-J. Hong, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 304, 2010.
[18] Y. Kim, S. C. Oh, W. C. Lim, J. H. Kim, W. J. Kim, J. H. Jeong, H. J. Shin, K. W. Kim, K. S. Kim, J. H. Park, S. H. Park, H. Kwon, K. H. Ah, J. E. Lee, S. O. Park, S. Choi, H. K. Kang, and C. Chung, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 210, 2011.
[19] Y. Iba, K. Tsunoda, Y. M. Lee, C. Yoshida, H. Noshiro, A. Akahashi, Y. Yamazaki, M. Nakabayashi, A. Hatada, A. Aoki, and T. Sugii, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 212, 2011.
[20] K. Miura, S. Ikeda, M. Yamanouchi, H. Yamamoto, K. Mizunuma, H. D. Gam, J. Hayakawa, R. Koizumi, F. Matsukura, and H. Ohno, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 214, 2011.
[21] W. Kim, J. H. Jeong, Y. Kim, W. C. Lin, J. H. Kim, J. H. Park, H. J. Shin, Y. S. Park, K. S. Kim, S. H. Park, Y. J. Lee, K. W. Kim, H. J. Kwon, H. L. Park, H. S. Ahn, S. C. Oh, J. E. Lee, S. O. Park, S. Choi, H. K. Kang, and C. Chung, *Tech. Dig. Int. Electron Devices*, Washington, p. 531, 2011.
[22] Y. Huai, *AAPPS Bulletin*, vol. 18, no. 6, p. 33, 2008.
[23] H. Horii, J. H. Yi, J. H. Park, Y. H. Ha, I. G. Beak, S. O. Park, Y. N. Hwang, S. H. Lee, Y. T. Kim, K. H. Lee, U. I. Chung, and J. T. Moon, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 177, 2003.
[24] N. Matsuzaki, K. Kurotsuchi, Y. Matsui, O. Tonomura, N. Yamamoto,

DOI: 10.1587/elex.9.908
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Y. Fujisaki, N. Kitai, R. Takemura, K. Osada, S. Hanzawa, H. Moriya, T. Iwasaki, T. Kawahara, N. Takaura, M. Terao, M. Matsuoka, and M. Moniwa, *Tech. Dig. Int. Electron Devices*, Washington, p. 757, 2005.

[25] T. Morikawa, K. Kurotsuchi, M. Kinoshita, N. Matsuzaki, Y. Matsui, Y. Fujisaki, S. Hanzawa, A. Kotabe, M. Terao, H. Moriya, T. Iwasaki, M. Matsuoka, F. Nitta, M. Moniwa, T. Koga, and N. Takaura, *Tech. Dig. Int. Electron Devices*, Washington, p. 307, 2007.

[26] M. Wuttig and N. Yamada, *Nature Mat.*, vol. 6, p. 824, 2007.

[27] Y. Fujisaki, N. Matsuzaki, K. Kurotsuchi, T. Morikawa, M. Kinoshita, N. Kitai, S. Hanzawa, H. Moriya, N. Takaura, M. Terao, M. Matsuoka, T. Koga, and M. Moniwa, *Mater. Res. Soc. Symp. Proc.*, vol. 997, p. 293, 2007.

[28] Y. H. Ha, J. H. Yi, H. Horii, J. H. Park, S. H. Joo, S. O. Park, U.-I. Chung, and J. T. Moon, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 175, 2003.

[29] Y. C. Chen, C. T. Rettner, S. Raoux, G. W. Burr, S. H. Chen, R. M. Shelby, M. Salinga, W. P. Risk, T. D. Happ, G. M. McClelland, M. Breitwisch, A. Schrott, J. B. Philipp, M. H. Lee, R. Cheek, T. Nirschl, M. Lamorey, C. F. Chen, E. Joseph, S. Zaidi, B. Yee, H. L. Lung, R. Bergmann, and C. Lam, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 777, 2006.

[30] F. Pellizzer, A. Pirovano, F. Ottogalli, M. Magistretti, M. Scaravaggi, P. Zuliani, M. Tosi, A. Benvenuti, P. Besana, S. Cadeo, T. Marangon, R. Morandi, R. Piva, A. Spandre, R. Zonca, A. Modelli, E. Varesi, T. Lowrey, A. Lacaita, G. Casagrande, P. Cappelletti, and R. Bez, *Proc. Int. Symp. on VLSI Technol.*, Honolulu, p. 18, 2004.

[31] F. Pellizzer, A. Benvenuti, B. Gleixner, Y. Kim, B. Johnson, M. Magistretti, T. Marangon, A. Pirovano, R. Bez, and G. Atwood, *Proc. Int. Symp. on VLSI Technol.*, Honolulu, p. 150, 2006.

[32] F. Merget, D. H. Kim, P. H. Bolivar, and H. Kurz, *Microsyst. Technol.*, vol. 13, p. 169, 2007.

[33] T. D. Happ, M. Breitwisch, A. Schrott, J. B. Philipp, M. H. Lee, R. Cheek, T. Nirschl, M. Lamorey, C. H. Ho, S. H. Chen, C. F. Chen, E. Joseph, S. Zaidi, G. W. Burr, B. Yee, Y. C. Chen, S. Raoux, H. L. Lung, R. Bergmann, and C. Lam, *Proc. Int. Symp. on VLSI Technol.*, Honolulu, p. 148, 2006.

[34] W. S. Chen, C. M. Lee, D. S. Chao, Y. C. Chen, F. Chen, C. W. Chen, P. H. Yen, M. J. Chen, W. H. Wang, T. C. Hsiao, J. T. Yeh, S. H. Chiou, M. Y. Liu, T. C. Wang, L. L. Chein, C. M. Huang, N. T. Shih, L. S. Tu, D. Huang, T. H. Yu, M. J. Kao, and M.-J. Tsai, *Tech. Dig. Int. Electron Devices*, Washington, p. 319, 2007.

[35] M. Breitwish, T. Nirschl, C. F. Chen, Y. Zu, M. H. Lee, M. Lamorey, G. W. Burr, E. Joseph, A. Schrott, J. B. Philipp, R. Cheek, T. D. Happ, S. H. Chen, S. Zaidi, P. Flaitz, J. Bruley, R. Dasaka, B. Rajendran, S. Rossnagel, M. Yang, Y. C. Chen, R. Bergmann, H. L. Lung, and C. Lam, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 100, 2007.

[36] D. H. Im, J. I. Lee, S. L. Cho, H. G. An, D. H. Kim, I. S. Kim, H. Park, D. H. Ahn, H. Horii, S. O. Park, U.-I. Chung, and J. T. Moon, *IEEE IEDM Tech. Dig.*, p. 211, 2008.

[37] I. S. Kim, S. L. Cho, D. H. Im, E. H. Cho, D. H. Kim, G. H. Oh, D. H. Ahn, S. O. Park, S. W. Nam, J. T. Moon, and C. H. Chung, *VLSI Tech. Dig.*, p. 203, 2010.

[38] J. T. Kang, T. J. Park, Y. W. Kwon, D. H. Ahn, Y. S. Kang, H. Jeong, S. J. Ahn, Y. J. Song, B. C. Kim, S. W. Nam, H. K. Kang, G. T. Jeong,

DOI: 10.1587/elex.9.908
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Published May 31, 2012

and C. H. Chung, *IEEE IEDM Tech. Dig.*, p. 39, 2011.
[39] J. Y. Wu, M. Breitwisch, S. Kim, T. H. Hsu, R. Cheek, P. Y. Du, J. Li, E. K. Lai, Y. Zhu, T. Y. Wang, H. Y. Cheng, A. Schrott, E. A. Josehp, R. Dasaka, S. Raoux, M. H. Lee, H. L. Lung, and C. Lam, *IEEE IEDM Tech. Dig.*, p. 43, 2011.
[40] J. Liang, R. G. D. Jeyasingh, H.-Y. Chen, and H.-S. P. Wong, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 100, 2011.
[41] Y. Sasago, M. Kinoshita, T. Morikawa, K. Kurotsuchi, S. Hanzawa, T. Mine, A. Shima, F. Fujisaki, H. Kume, H. Moriya, N. Takaura, and K. Torii, *VLSI Tech. Dig.*, p. 24, 2009.
[42] R. Bez, *IEEE IEDM Tech. Dig.*, p. 89, 2009.
[43] R. Waser and M. Aono, *Nature Mat.*, vol. 6, p. 833, 2007.
[44] A. Sawa, *Mat. Today*, vol. 11, p. 28, 2008.
[45] S. Jung, M. Siddik, W. Lee, J. Park, X. Liu, J. Woo, G. Choi, J. Lee, N. Lee, Y. H. Jang, and H. Hwang, *IEEE IEDM Tech. Dig.*, p. 59, 2011.
[46] A. Sawa, R. Fujii, M. Kawasaki, and Y. Tokura, *Appl. Phys. Lett.*, vol. 85, p. 4073, 2004.
[47] I. G. Baek, D. C. Kim, M. J. Lee, H.-J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O. Park, H. S. Kim, I. K. Yoo, U.-I. Chung, J. T. Moon, and B. I. Ryu, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 587, 2004.
[48] Y. You, B. So, J. Hwang, W. Cho, S. Lee, T. Chung, C. Kim, and K. An, *Appl. Phys. Lett.*, vol. 89, p. 222105, 2006.
[49] H. S. Yoon, I.-G. Baek, J. Zhao, H. Sim, M. Y. Park, H. Lee, G.-H. Oh, J. C. Shin, I.-S. Yeo, and U.-I. Chung, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 26, 2009.
[50] B. Lee and H.-S. P. Wong, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 28, 2009.
[51] D. C. Kim, M. J. Lee, S. E. Ahn, S. Seo, J. C. Park, I. K. Yoo, I. G. Baek, H. J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U.-I. Chung, J. T. Moon, and B. I. Ryu, *Appl. Phys. Lett.*, vol. 88, p. 232106, 2006.
[52] I. Park, K. Kim, S. Lee, and J. Ahn, *Jpn. J. Appl. Phys.*, vol. 46, no. 4B, p. 2172, 2007.
[53] B. Gao, H. W. Zhang, S. Yu, B. Sun, L. F. Liu, X. Y. Liu, Y. Wang, R. Q. Han, J. F. Kang, B. Yu, and Y. Y. Wang, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 30, 2009.
[54] Y. S. Chen, H. Y. Lee, P. S. Chen, P. Y. Gu, C. W. Chen, W. P. Lin, W. H. Liu, Y. Y. Hsu, S. S. Sheu, P. C. Chiang, W. S. Chen, F. T. Chen, C. H. Lien, and M.-J. Tsai, *Tech. Dig. Int. Electron Devices*, Baltimore, p. 105, 2009.
[55] J. Lee, J. Shin, D. Lee, W. Lee, S. Jung, M. Jo, J. Park, K. Biju, S. Kim, S. Park, and H. Hwang, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 452, 2010.
[56] G. Bersuker, D. C. Gilmer, D. Veksler, J. Yum, H. Park, S. Lian, L. Vandelli, A. Padovani, L. Larcher, K. M. Shluger, V. Iglesias, M. Porti, M. Nafria, W. Taylor, P. D. Kirsch, and R. Jammy, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 456, 2010.
[57] H. Y. Lee, Y. S. Chen, P. S. Chen, P. Y. Gu, Y. Y. Hsu, S. M. Wang, W. H. Liu, C. H. Tsai, S. S. Sheu, P. C. Chiang, W. P. Lin, C. H. Lin, W. S. Chen, F. T. Chen, C. H. Lien, and M.-J. Tsai, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 460, 2010.
[58] C.-H. Wang, Y.-H. Tsai, K.-C. Lin, F.-F. Chang, Y.-C. King, C.-J. Lin, S.-S. Sheu, Y.-S. Chen, H.-Y. Lee, F. T. Chen, and M.-J. Tsai, *Tech.*

DOI: 10.1587/elex.9.908
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Published May 31, 2012

Dig. Int. Electron Devices, San Francisco, p. 664, 2010.
[59] X. A. Tran, B. Gao, J. F. Kang, L. Wu, Z. R. Fang, K. L. Pey, Y. C. Yeo, A. Y. Du, B. Y. Nguyen, M. F. Li, and H. Y. Yu, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 44, 2011.
[60] X. A. Tran, B. Gao, J. F. Kang, X. Wu, L. Wu, Z. Fang, Z. R. Wang, K. L. Pey, Y. C. Yeo, A. Y. Du, M. Liu, B. Y. Nguyen, M. F. Li, and H. Y. Yu, *Tech. Dig. Int. Electron Devices*, Washington, p. 713, 2011.
[61] Y. S. Chen, H. Y. Lee, P. S. Chen, C. H. Tsai, P. Y. Gu, T. Y. Wu, K. H. Tsai, S. S. Sheu, W. P. Lin, C. H. Lim, P. F. Chiu, W. S. Chen, F. T. Chen, C. Lien, and M.-J. Tsai, *Tech. Dig. Int. Electron Devices*, Washington, p. 717, 2011.
[62] B. Govoreanu, G. S. Kar, Y.-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, and M. Jurczak, *Tech. Dig. Int. Electron Devices*, Washington, p. 729, 2011.
[63] K. Kinoshita, C. Yoshida, H. Aso, M. Aoki, and Y. Sugiyama, *Extended Abstracts of Int. Conf. on Solid State Devices and Materials*, Yokohama, p. 570, 2006.
[64] M. Fujimoto, H. Koyama, M. Konagai, Y. Hosoi, K. Ishihara, S. Ohnishi, and N. Awaya, *Appl. Phys. Lett.*, vol. 89, p. 223509, 2006.
[65] D. S. Jeong, H. Schroeder, and R. Waser, *Appl. Phys. Lett.*, vol. 89, p. 082909, 2006.
[66] Y. H. Tseng, C.-E. Huang, C.-H. Kuo, Y.-D. Chin, and C. J. Lin, *Tech. Dig. Int. Electron Devices*, Baltimore, p. 109, 2009.
[67] M. J. Kim, I. G. Back, Y. H. Ha, S. J. Baik, J. H. Kim, D. J. Seong, S. J. Kim, Y. H. Kwon, C. R. Lim, H. K. Park, D. Gilmer, P. Kirsch, R. Jammy, Y. G. Shin, S. Choi, and C. Chung, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 444, 2010.
[68] Y. H. Tseng, W. C. Shen, C.-E. Huang, C. J. Lin, and Y.-C. King, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 636, 2010.
[69] J. Yi, H. Choi, S. Lee, J. Lee, D. Son, S. Lee, S. Hwang, S. Song, J. Park, S. Kim, W. Kim, J.-Y. Kim, S. Lee, J. Moon, J. You, M. Joo, J. S. Poh, S. Park, S.-W. Chung, J. Lee, and S.-J. Hong, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 48, 2011.
[70] Y. Sakotsubo, M. Terai, S. Kotsuji, Y. Saito, M. Tada, Y. Yabe, and H. Hada, *Proc. Int. Symp. on VLSI Technol.*, Hawaii, p. 87, 2010.
[71] M. Terai, M. Saitoh, T. Nagumo, Y. Sakotsubo, Y. Yabe, K. Takeda, and T. Hase, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 50, 2011.
[72] Y.-B. Kim, S. R. Lee, D. Lee, C. B. Lee, M. Chang, J. H. Hur, M.-J. Lee, G.-S. Park, C. J. Kim, U.-I. Chung, I.-K. Yoo, and K. Kim, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 52, 2011.
[73] Z. Wei, T. Takagi, Y. Kanazawa, Y. Katoh, T. Ninomiya, K. Kawai, S. Muraoka, S. Mitani, K. Katayama, S. Fujii, R. Miyanaga, Y. Kawashima, T. Mikawa, K. Shimakawa, and K. Aono, *Tech. Dig. Int. Electron Devices*, Washington, p. 721, 2011.
[74] I. G. Baek, C. J. Park, H. Ju, D. J. Seong, H. S. Ahn, J. H. Kim, M. K. Yang, S. H. Song, E. M. Kim, S. O. Park, C. H. Park, C. W. Song, G. T. Jeong, S. Choi, H. K. Kang, and C. Chung, *Tech. Dig. Int. Electron Devices*, Washington, p. 737, 2011.
[75] C. H. Ho, C.-L. Hsu, C.-C. Chen, J.-T. Liu, C.-S. Wu, C.-C. Huang, C. Hu, and F.-L. Yang, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 436, 2010.
[76] W. C. Chen, Y. R. Chen, Y. C. Chen, A. T. H. Chuang, F. M. Lee, Y.

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Received May 08, 2012
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Published May 31, 2012

Y. Lin, E. K. Lai, Y. H. Shih, K. Y. Hsieh, and C.-Y. Lu, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 440, 2010.
[77] W.-C. Chien, M.-H. Lee, F.-M. Lee, Y.-Y. Lin, H.-L. Lung, K.-Y. Hsieh, and C.-Y. Lu, *Tech. Dig. Int. Electron Devices*, Washington, p. 725, 2011.
[78] C. H. Cheng, A. Chin, and F. S. Yeh, *Proc. Int. Symp. on VLSI Technol.*, Hawaii, p. 85, 2010.
[79] C. H. Cheng, C. Y. Tsai, A. Chin, and F. S. Yeh, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 448, 2010.
[80] C. H. Cheng, K. Y. Chou, A. Chin, and F. S. Yeh, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 512, 2010.
[81] E. Linn, R. Rosezin, C. Kugeler, and R. Waser, *Nature Mat.*, vol. 9, p. 403, 2010.
[82] B. Choi, S. Choi, K. Kim, Y. Shin, C. Hwang, S. Hwang, S. Cho, S. Park, and S. Hong, *Appl. Phys. Lett.*, vol. 89, p. 012906, 2006.
[83] M. Kund, G. Beitel, C.-U. Pinnow, T. Röhr, J. Schumann, R. Symanczyk, K.-D. Ufert, and G. Mueller, *Tech. Dig. Int. Electron Devices*, Washington, p. 773, 2005.
[84] T. Sakamoto, N. Banno, N. Iguchi, H. Kawamura, H. Sunamura, S. Fujieda, K. Terabe, T. Hasegawa, and M. Aono, *Proc. Int. Symp. on VLSI Technol.*, Kyoto, p. 38, 2007.
[85] M. Wang, W. J. Luo, Y. L. Wang, L. M. Yang, W. Zhu, P. Zhou, J. H. Yang, X. G. Gong, and Y. Y. Lin, *Proc. Int. Symp. on VLSI Technol.*, Hawaii, p. 89, 2010.
[86] Y.-Y. Lin, F.-M. Lee, Y.-C. Chen, W.-C. Chien, C.-W. Yeh, K.-Y. Hsieh, and C.-Y. Lu, *Proc. Int. Symp. on VLSI Technol.*, Hawaii, p. 91, 2010.
[87] Y.-Y. Lin, F.-M. Lee, W.-C. Chien, Y.-C. Chen, K.-Y. Hsieh, and C.-Y. Lu, *Tech. Dig. Int. Electron Devices*, San Francisco, p. 524, 2010.
[88] J. Park, W. Lee, S. Jung, M. Son, S. Kim, S. Park, J. Shin, D. Lee, M. Siddik, J. Woo, G. Choi, E. Cha, T. Lee, and H. Hwang, *Tech. Dig. Int. Electron Devices*, Washington, p. 63, 2011.
[89] F. Nardi, S. Balatti, S. Larentis, and D. Ielmini, *Tech. Dig. Int. Electron Devices*, Washington, p. 709, 2011.
[90] R. Müller, J. Genoe, and P. Heremans, *Appl. Phys. Lett.*, vol. 88, p. 242105, 2006.
[91] S. Fujisaki, H. Ishiwara, and Y. Fujisaki, *Appl. Phys. Lett.*, vol. 90, p. 162902, 2007.
[92] S. Fujisaki, Y. Fujisaki, and H. Ishiwara, *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 54, no. 12, p. 2592, 2007.
[93] J. Karasawa, T. Yasuda, T. Saeki, T. Aoki, S. Moriya, E. Hirai, T. Masuda, T. Kawase, T. Shimoda, D. P. Chu, C. J. Newsome, S. W. Tam, and M. Ishida, *Proc. Int. Symp. on the Application of Ferroelectrics*, Nara, 30B-FR5-I1, 2007.
[94] T. Sekitani, Y. Noguchi, S. Nakano, K. Zaitsu, Y. Kato, M. Takamiya, T. Sakurai, and T. Someya, *Tech. Dig. Int. Electron Devices*, Washington, p. 221, 2007.
[95] Y. Fujisaki, *Jpn. J. Appl. Phys.*, vol. 49, p. 100001, 2010.

1 Introduction

Recently, new types of non-volatile memories have been actively proposed because Flash memories are now approaching to their scaling limit. Among

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the candidates replacing Flash memories, ferroelectric memory (FeRAM; Ferroelectric Random Access Memory), magneto-resistive memory (MRAM; Magneto-resistive RAM), and phase change memory (PCRAM; Phase Change RAM) are already in production and used to various applications although the amount of products remains small. In addition to the above-mentioned three types, resistive change memory (ReRAM; Resistive change RAM), spin transfer MRAM, and organic nonvolatile memories are now under research.

The question is why the research rush takes place on many kinds of non-volatile memories now. This is based on the expectation that Flash cannot be scaled down below 1x nm (1x nm; represents the technologies from 19 nm to 10 nm). The major reason for this limitation is the parasitic effects [1] caused by the electro-static capacitance composed of the neighboring memory cells. In highly integrated memory cells, this capacitance disturbs read and write operations to a memory cell since the space between the neighboring cells become small making large electro-static force and affecting to access to a specific cell [2]. Because the physics of this phenomenon is quite clear, this disturbance can be simulated quantitatively if the cell structure is once determined. In 2012, the most advanced NAND Flash memory is being produced using the 19 nm technology. In 2010, it was produced with 24 nm technology. The aggressive shrinkage has taken place in a couple of years. If this scaling pace would be kept for a while days of Flash are numbered. Therefore, new types of memories replacing Flash have been proposed continuously during the past few years. To avoid the parasitic effect, all of the new memories are based on the different mechanism other than storing charges in a cell. In this paper, the new memories will be categorized in several groups at first and are briefly reviewed.

2 FeRAM

FeRAM was transferred to production for the first time among new types of non-volatile memories. It is now widely used as an embedded memory in a logic LSI for wireless cards including railway passes, automobile equipments such as event data recorders (EDRs) [3], and domestic electronic appliances. The most significant feature of FeRAM is its overwhelmingly low power consumption that cannot be achieved by any other non-volatile memory including Flash. Thanks to this feature, FeRAM has built up its own territory in which even Flash cannot ingress. In addition, low voltage operation less than 2 V is the great advantage against Flash that requires larger than 20 V for write or erase. Therefore, a voltage pump up circuit indispensable for Flash can be eliminated with the use of FeRAM that is advantageous for embedded application in a logic LSI. Moreover, writing speed and the maximum number of rewrites of FeRAM are at least two and six orders of magnitude greater than those of Flash, respectively.

However, the FeRAM in practical use has the cell structure composed of one transistor and one ferroelectric capacitor that is not suitable of ultimate

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scaling. The highest density ever reported is 128 Mb [4] and that of real products remains 4 Mb.

Beside a capacitor type cell, FeRAM has a transistor type and a chain cell [5] type that are more suitable for high density application. A transistor type cell has a structure like a MOS transistor but the gate oxide is replaced with a ferroelectric oxide. This type of FeRAM can compose NAND string [6] like Flash and competitive against Flash in density. However, transistor-type FeRAM has essentially poor retention characteristics [7] and therefore cannot be applicable in practical use ensuring 10 year data retention.

Because the physics behind FeRAM technology is well understood, its performances can be improved with ease if new materials with higher physical parameters would be implemented. In near future, FeRAMs with higher density become in production and the number of applications will increase greatly. For further information, refer to the following reports [7, 8].

3 MRAM

The first product of MRAM was released in 2006 although its density was small. The operating mechanism of MRAM is based on the phenomenon called tunnel magneto-resistance (TMR). There are a lot of studies on TMR phenomenon and the physics behind it is well understood [9]. The memory cell of a MRAM product is composed of one MOS transistor and a device called MTJ (Magnetic Tunnel Junction). A MTJ has a stack structure composing of a thin tunnel insulator such as MgO sandwiched between two magnetic films with electrodes on both outer-side of magnetic films. One of the magnetic films is called a fixed layer or pinned layer in which magnetization is hard to be rotated. The other one is called a free layer in which magnetization is easily rotated. If the directions of magnetization in two magnetic films are parallel, a MTJ becomes low resistive. If they are anti-parallel, a MTJ becomes highly resistive. Writing is performed by introducing current to two adjacent wires for rotating the magnetization direction of the free layer using the magnetic field produced by the current. The most outstanding feature of MRAM is its high operating speed, thus it can replace high speed SRAMs. Furthermore, MRAM has no degradation mode during write operation, it endures infinite rewrite different from Flash and FeRAM. However, writing current of MRAM is too high for portable devices. Therefore, practical application is limited such as drive recorders as advanced EDRs, as mentioned above.

Spin transfer torque MRAMs (STT-MRAM) have been proposed as a solution to solve the problem of high operation current. Unlike the conventional MRAM, STT-MRAM controls the magnetization direction in the free layer of MTJ by inducing a current with aligned spin between fixed layer and free layer. STT type MRAM has several important advantages against the conventional one such as suppression of the increase in the current density with scaling and the reduction in cell area thanks to the simplified structure [10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21]. However, STT-MRAM still

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has a problem of small resistance on/off ratio that is one of the biggest obstacles to realize highly integrated memories. In addition, three-dimensional (3D) integration like Flash is difficult because MRAM operates under bipolar mode in which a transistor with high current drivability is dispensable for a cell selection device.

The operation current of the most advanced STT-MRAM made with the 17 nm technology has been reduced down to 40 μA [21] which is acceptable for memories with medium scale integration. The replacement of a part of DRAMs is a realistic target since MRAM has infinite rewrite endurance like DRAM.

4 PCRAM

PCRAM has a capacitor-like simple structure in which thin chalcogenide semiconductor film composed of group IV elements is sandwiched between electrodes. Therefore it can be miniaturized easily. Most commonly used materials for PCRAM are $Ge_2Sb_2Te_5$ and Sb_2Te_3 but materials doped with impurities such as nitrogen or oxygen also have been studied to improve operation speed or thermal stability [22, 23, 24, 25]. The operating principle of PCRAM is based on the phase change of chalcogenide material from amorphous to crystal, or vice versa, at reasonably low temperature around 600 C [26]. The energy required for phase change is supplied from Joule heat generated by the current through a PCRAM cell itself. Because chalcogenide material is low resistive in crystal phase and relatively highly resistive in amorphous phase, information can be stored with its resistivity. And each phase is stable enough at room temperature to make PCRAM as a non-volatile memory.

It is called set operation, or more simply "set", to make PCRAM from highly resistive amorphous state to low resistive crystal state. Reset operation, or "reset", corresponds to the reverse process against "set". Because set and reset are controlled by Joule heat, these operations are managed with current pulses instead of voltage pulses. Usually, MOS transistors with their current saturation properties are used to make current pulses. Therefore, most PCRAM use MOS transistors as a cell selection device.

In reset operation, chalcogenide material is once heated above its melting temperature and then cooled rapidly to make amorphous state. In set operation, chalcogenide material is heated above crystallization but below melting temperature and cooled gradually to enhance crystallization. Therefore, the maximum current needed to operate PCRAM is reset current. Because reset current is thought to be proportional to the volume of PCRAM, reset current is expected to become smaller due to the scaling down of the device. However, reset current values ever reported are too large to be applied to the most scaled LSIs like 32 Gb Flash, thus significant reduction of reset currents is the most important research item for PCRAMs. To this aim, various types of PCRAMs were proposed intending to miniaturize the device beyond the limitation of the lithography limit. These reports were based on the concept

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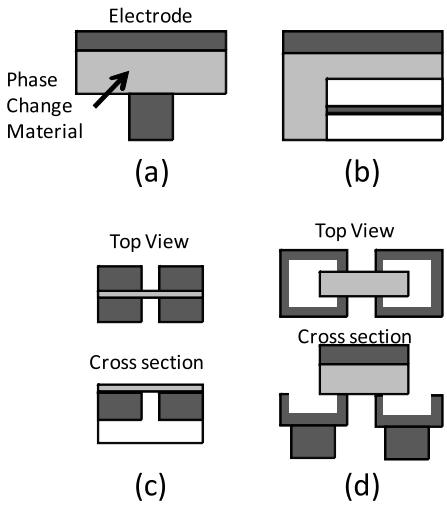

Fig. 1. Schematic drawings of PCRAMs, (a) Bottom contact [27], (b) Edge contact [28], (c) Wire type [29], (d) Micro-trench type [30, 31].

that the reduction of PCRAM volume leads to the reduction of reset current. Some important results will be introduced below.

PCRAM shown in Fig. 1 (a) is a typical example of a bottom contact cell [27]. Bottom contact is the simplest cell and a lot of earlier papers reported using this structure. However, the volume of phase change portion directly depends on the lithography limit but the miniaturization is not enough with this way as mentioned above. A schematic drawing of an edge contact cell is shown in Fig. 1 (b) [28]. In this structure, one of the electrodes is composed of a thin film that is connected to the chalcogenide material. Since phase change volume is defined with the thickness of a film shaped electrode, miniaturization of phase change portion beyond the lithography limit can be possible with this structure. In Fig. 1 (c), a wire type PCRAM structure is shown [29]. In this structure, chalcogenide material is fabricated in a wire shape, bridging two adjacent electrodes. Since the width of chalcogenide wire can be reduced beyond the lithography limit by optimizing fabrication conditions. In addition, thickness control of chalcogenide film directly affects the volume control of phase change portion. Thus, the phase change volume of wire type PCRAM can be reduced beyond the lithography limit. In Fig. 1 (d), schematic drawing of Micro-trench PCRAM structure is shown [30, 31]. In Micro-trench structure, bottom electrodes are made of very thin side walls of a box, thus the contact area to chalcogenide material can be made smaller than the lithography limit. Micro-trench structure was made to deposit chalcogenide material on the bottom electrode just like the conventional bottom contact cells. Due to this well established process, much stable contact between chalcogenide material and electrode can be achieved compared to edge contact cells. In actuality, write endurance as good as 10^{12} cycles was reported with Micro-trench cells.

There are various alternatives such as a bottleneck cell [32] that has a constricted thin chalcogenide layer, a pillar cell [33] that has a small cylin-

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Table I. List of reset currents taken with various kinds of PCRAMs.

Device Structure	Reset Current (μA)	Reset Area (nm^2)	Reference Number	Affiliation
Bottom Contact (With spacer)	100	25,434	27	Hitachi
Edge Contact	200	4,000	28	Samsung
Wire	140	90	29	IBM
Micro-trench	600	1,500	30	STMicro
Micro-trench	400	400	31	STMicro
Bottle Neck	280	3,000	32	Aahen Univ.
Pillar	900	197	33	IBM
Cross Spacer	240	1,000	34	IBM
Pore	450	1,451	35	IBM
Dash	160	488	36	Samsung
Dash	80	128	37	Samsung
Dash	90	180	38	Samsung
Bottom Contact (With a ring electrode)	30	?	39	IBM
Bottom Contact (With CNT electrode)	1.4	?	40	Stanford Univ.

drical chalcogenide bar, a cross-spacer cell [34], a pore cell [35], and a dash cell [36, 37, 38]. For example, the pore cell was made using a small pore that appears in a semiconductor manufacturing process. The dash cell, that is made by depositing chalcogenide material using CVD into a 7 nm width slit, also uses a tricky process to make such a small structure. All of the examples listed above are to make the cells smaller beyond the lithography limit. In spite of these challenges, the minimum reported value of reset currents is 80 μA. At present, there seems to be no obvious relationship between reset current and the size of a cell, although everyone believed that reset current could be reduced due to the miniaturization of a cell. Recently, drastic reduction of reset current were reported with a ring electrode cell, that has a small ring shaped bottom electrode, and with a cell using a CNT as a bottom electrode, but the operations are quite unstable. These miniaturizations are useful to examine the ultimate structure of PCRAM technology but not realistic at present. The reported reset values are summarized in Table I.

The author's group recently demonstrated a highly integrated cross point PCRAM composed of one diode and one phase change cell (Fig. 2) [41]. In this challenge, we found that poly-Si diode can afford to supply 8 MA/cm^2 as the maximum current density. Therefore, it was quantitatively proved that the reduction of reset current is the first priority item to realize Gb scale integrated PCRAMs. In Fig. 3, an example how the reset currents can be reduced due to miniaturization is shown. In the figure, the calculated current densities are also plotted. Since reset current depends on the device structure, current scaling is discussed using the devices with the same Micro-trench structure [42]. In this case, reset current can be reduced below 100 μA if the minimum feature size f is made as small as 20 nm. However, the current density becomes larger than 20 MA/cm^2 at the same time. Such high current density is not acceptable for wires in LSIs. Assume that 8 MA/cm^2 is the maximum tolerable current density for cell selection devices, reset current has

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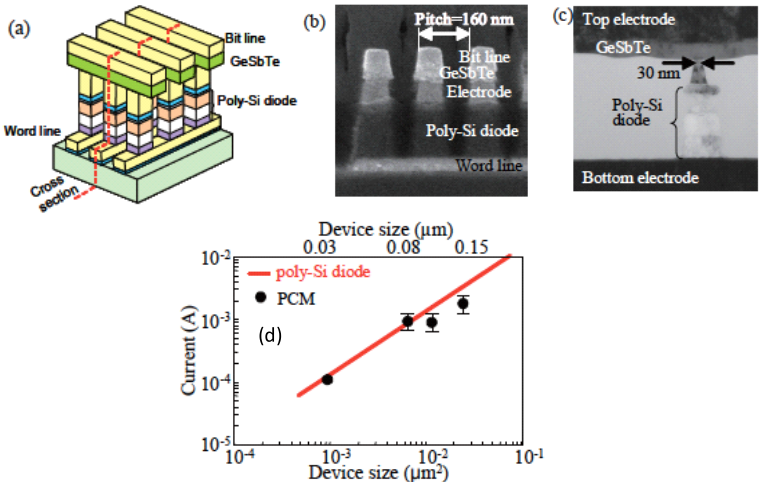

Fig. 2. PCRAM with cross point memory cell. (a) Structure, (b), (c) Cross sectional TEM images, (d) Relationship between reset current and current drivability of a diode [41].

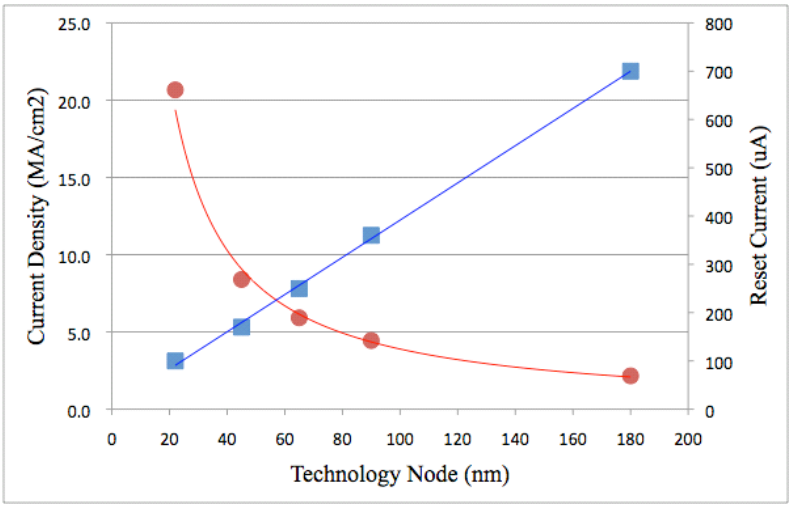

Fig. 3. Scalability of reset current on Mirco-trench PCRAMs. Current densities calculated from reset current values are also plotted [42].

to be reduced below 32 μA in the devices made with f = 20 nm technology.

Although PCRAM has been thought to be the most promising device replacing Flash, reset current is too large to realize highly integrated memories like Flash. Thus, some innovative idea is required before achieving LSIs like Flash.

5 ReRAM

Recently, resistive switching memories with the structure in which thin oxide film or solid electrolyte is sandwiched by two electrodes are actively researched. ReRAM is categorized in two types. One is the device that uses the resistive switching phenomena of oxide materials, and the other one uses

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the chemical reaction of metal ions in solid electrolyte.

ReRAM uses resistive switching phenomena is further classified in two groups. One is the memory using Perovskite oxides such as PCMO ($Pr_{0.7}Ca_{0.3}MnO_3$) or STO ($SrTiO_3$) and the other one is the group that uses binary oxides such as NiO or HfO_2. Most of ReRAMs using Perovskite oxides operate with bipolar modes, on the other hand most of ReRAMs using binary oxides operate with non-polar modes. However, operating mechanisms of both types of ReRAMs are not clearly understood, thus the studies on the device physics are the main items before practical use. In the following sections, reports representing each type of ReRAMs are briefly introduced. Details of each device can be summarized in other reports [43, 44].

5.1 ReRAM using Perovskite oxides

ReRAMs with the structure like Ti/PCMO/Pt have hysteresis in their I-V characteristics, thus they can be used for non-volatile memories. In general, this type of memories requires the initializing process called "forming" before the practical use. Recently, a lot of papers repot forming free operation by adopting thin oxide multi-layers in their structures [45]. With the use of thin oxide layers, large electric field can be applied to the resistive switching oxide layer with low voltage that is required for forming process.

The origin of resistive change of a ReRAM in [45] is reported to be caused by the change of Schottky barrier height due to the carrier capture and emission process at the interface between PCMO and an electrode (Fig. 4). Contrary to this model, there are several other models based on SCLC (Space Charge Limited Current), bulk Mott transition, filament Mott transition,

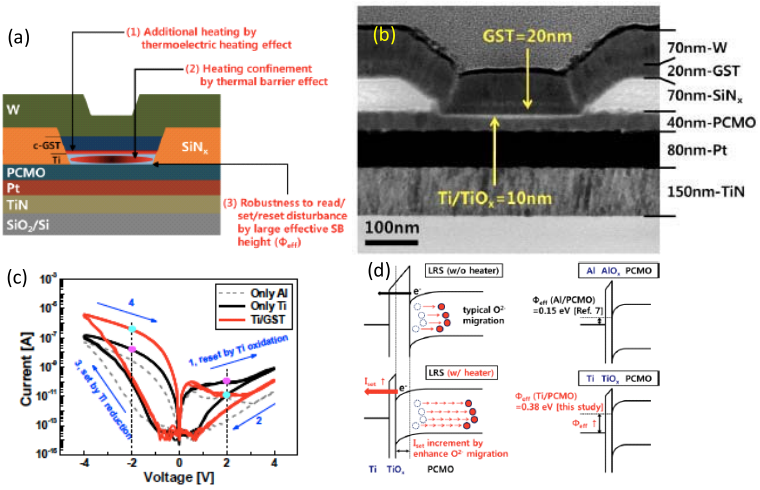

Fig. 4. ReRAM using Perovskite PCMO. Hysteresis appears in I-V characteristics can be used for non-volatile memory. Authors explained that switching takes place due to Schottky barrier height change at PCMO and a top electrode. In this case, PCMO is covered with GST (GeSbTe) that works as a heater to enhance switching phenomena.

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Received May 08, 2012
Accepted May 09, 2012
Published May 31, 2012

interface Mott transition, etc. The true mechanism of this type of ReRAMs still remains to be disclosed. Anyway, the concept that a part of oxide-electrode interface changes its resistivity making a filament shaped conductive pass seems to be more persuasive compare to the idea that some uniform change takes place at oxide-electrode interface.

Though filament conduction model seems to be more realistic, the actual form of filament is not revealed yet to date. Therefore, the disclosure of physics behind the resistive change is the first priority item of this type of ReRAMs.

5.2 ReRAM using binary oxides

ReRAMs using many kinds of binary oxides begun to be reported since a paper on a cross point cell with a Pt/NiO/Pt structure published in 2005 [46]. After that, a lot of materials such as NiO [47, 48, 49, 50], HfO [51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62], TiO_2 [63, 64, 65, 66, 67, 68, 69], Ta_2O_5 [70, 71, 72, 73, 74], WO [75, 76, 77], and GeO [78, 79, 80] are proposed as other candidates. Most of reports use Pt as an electrode but papers using other metals like Ru, Ni, and IrO_2 are increasing.

In general, ReRAMs using binary oxides operate in a non-polar mode (Fig. 5). Taking advantage of non-polar operation, this type of ReRAM has the possibility to construct a highly integrated 1D1R (one diode combined with one resistor) cross point cell. However, there are few examples that operate in a bipolar mode. It was believed that a bipolar ReRAM should use a transistor as a selection device but E. Linn proposed a new structure, in which two ReRAMs are combined in series, can compose one memory cell without any other selection device [81]. An example of this new concept is shown in Fig. 6 [55]. In this case, two ReRAMs made of HfO related materials are connected in series. It shows symmetrical I-V characteristics

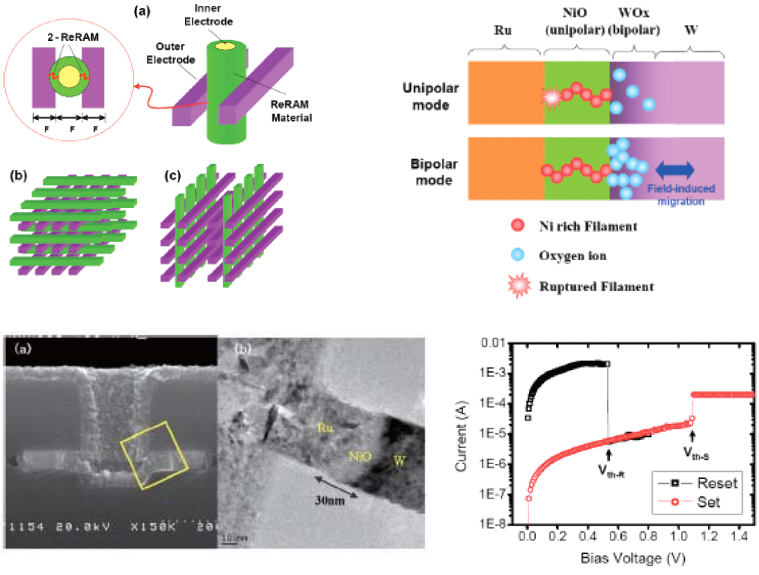

Fig. 5. Non-polar ReRAM using NiO as a switching layer [49].

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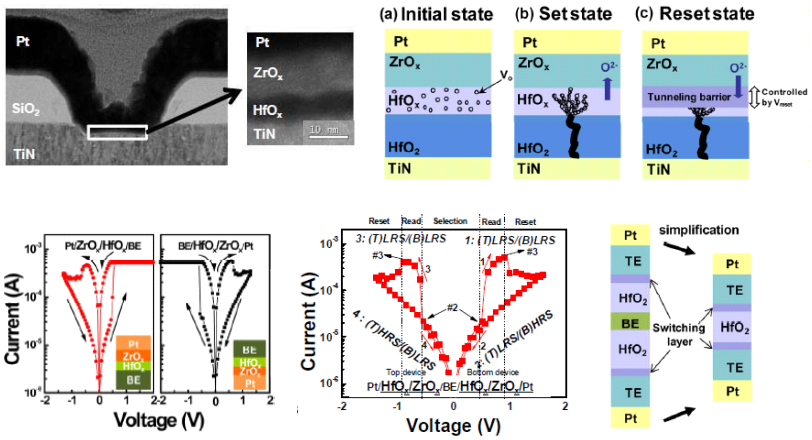

Fig. 6. Bipolar ReRAM using HfO. Two ReRAMs connected in series realizes I-V characteristics suitable for a diode free cell [55].

with high resistivity around 0 V. Therefore, a cross point memory cell can be composed without any cell selection device because half selection cell always in highly resistive regardless to its stored state. In [55], authors manufactured this structure but the number of rewrites was limited about 3,000 cycles although a single HfO ReRAM cell made in the same substrate endures 10^6 cycles. The authors explained that a slight difference in I-V characteristics of two combined cells causes unstable operation and limits the number of rewrites.

The operation mechanisms of binary oxide ReRAMs are also unclear and a lot of studies on the device physics should be carried out before practical use. A vague picture how the resistive switch takes place is as follows. Resistive switching is caused by growth and rupture of thin conductive filaments in an oxide film where large electric field helps to reduce oxide to make a filament and large current going through a filament fuses the conductive path [82]. However, there still remain not a few unexplained items with this model. To establish a reliable model is the main issue of this type of ReRAMs.

5.3 ReRAM using solid electrolyte

Solid electrolyte is the organic or inorganic material in which metal ions can move easily. If mobile ions such as Ag [83] or Cu [84, 85, 86, 87, 88] are diffused into solid electrolyte, the movement of these ions can be controlled by electric field made by two electrodes sandwiching the electrolyte. There are a lot of papers on ReRAMs using many kinds of solid electrolyte in which a conductive filament is formed or ruptured under the control of electric field. Especially, the device using Ag/Ag_2Se+GeSe/W operates at low voltage and helped to understand the operation mechanisms of this type of ReRAMs. Recently, electrolytes such as HfO, ZrO, and TiO, which are familiar with Si LSI process, tend to be chosen taking into account how easily technology can be transferred to production. A ReRAM using TiO/HfO multilayer as an electrolyte is shown in Fig. 7 [88]. At first, solid thicker conductive filament

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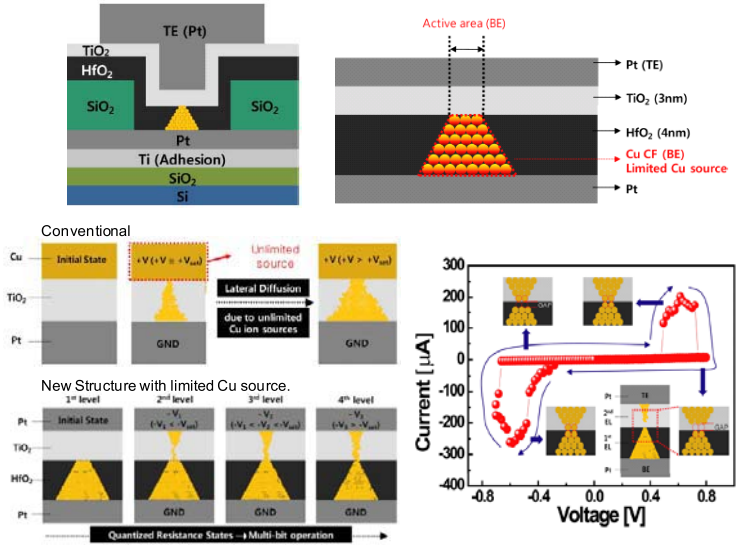

Fig. 7. ReRAM using Cu ions in solid electrolyte. Bi-layer HfO/TiO electrolyte makes it easier to make very thin conductive filament, that is suitable for multi-level storage.

was made in HfO layer during a fabrication process and then, thinner Cu filament was made in TiO layer using electric field. Thin filament in TiO layer can be ruptured by electric field, thus resistive switching is controlled by the applied voltage between two electrodes. The very thin Cu filament in TiO layer is suitable for multi-level information storage.

Because ReRAMs using solid electrolyte operate in bipolar mode, high density memories with 1D1R cross point cells cannot be fabricated with this type of ReRAMs. As mentioned in the previous section, the idea proposed by E. Linn can be applied to realize a cross point cell [89]. This structure might be more suitable to this type of ReRAMs because maldistribution of ions in electrolyte, that takes place after multiple rewrite operations, can be suppressed with Linn's structure.

In general, ReRAMs using solid electrolyte operate as fast as 50 ns and as many as $10^4 \sim 10^6$ cycles. In addition, the physics behind the device operation is well understood. Therefore, this type of ReRAMs is superior to ReRAMs using oxide materials. However, metal ions such as Ag or Cu have large thermal diffusion coefficient that makes quite difficult to control thermal stress during device fabrication process. This is the biggest problem of this ReRAM before practical use.

6 Organic memory

Aggressive studies have been carried out to merge organic materials into Si LSIs. Non-volatile memories using organic materials can be divided into three groups. Three groups are composed of memories using chemical reactions of organic materials, those using growth and rupture of conductive filaments in organic materials, and those using ferroelectricity of organic materials.

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A thin CuTCNQ (Cu-tetoracyanoquinodimethane) film sandwiched by Cu and Al electrodes shows resistive switch like a ReRAM. The origin of resistive switch was explained that Cu in a CuTCNQ film is reduced by current from electrodes making Cu conductive filaments in a film [90]. The I-V characteristics resemble to those of oxide ReRAMs operate in bipolar mode. In [90], I-V hysteresis appears at the voltage as large as 3 V.

Random co-polymer composed of VDF (Vinylidene Fluoride) and TrFE (Tri-fluoroethylene) shows ferroelectricity just like oxide ferroelectric materials. Our group succeeded to fabricate a ferroelectric capacitor using P(VDF-TrFE) with remnant polarization as large as 10 μC/cm^2 although the film thickness is below 60 nm. Thanks to thin film thickness, this capacitor can be operated below 2 V [91]. Recently, several papers repot ferroelectric memories made on a flexible substrate using P(VDF-TrFE) [92, 93]. Since organic memories generally have features of low cost, low temperature process, printability, etc., they try to explore new application field different from conventional non-volatile memories [94].

Organic non-volatile memories can be merged to Si LSIs but they can be applied to organic transistors, TFTs, and flexible devices.

7 Summary

A part of emerging new semiconductor non-volatile memories is reviewed in this article. You can find how fast the technologies are being developed if you compare this article with the author's previous report in 2010 [95]. Beside those introduced in this report, there are a lot of new promising concepts that might open future semiconductor industries and many of bran new ideas are now being proposed today. To brush them up to practical use, it is requested to ensure the non-volatility. In the memories for general purposes, the information stored should be saved as long as 10 years.

To ensure the non-volatility, some kind of acceleration test should be developed. Without understanding of the physics behind data storage, correct choice of acceleration factor, which predicts 10 year later, becomes impossible. Therefore, the total scheme of device operation including switching mechanism, endurance, retention, and failure modes have to be understood before practical use. This requirement makes the development of non-volatile memories quite difficult compare to other semiconductor devices. All the emerging new non-volatile memories should overcome this very high hurdle before being transferred to production. This is because FeRAMs, MRAMs, and PCRAMs required long term development. It is better to find a small application field, in which a new memory is much superior to other types of memories, and brush up technology through mass production even though the market is not large enough.

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Yoshihisa Fujisaki

He received his M.E. degree in physics and applied physics in 1981 from the Faculty of Science and Engineering, Waseda University. He also received a doctorate in engineering from the University of Tokyo in 1994. He joined Hitachi, Ltd., in 1981. He has been involved in the development of lasers used for optical fiber communication, semi-insulating GaAs substrate crystals, ferroelectric non-volatile memories, and new types of non-volatile memory in the Central Research Laboratory, Hitachi, Ltd.

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