PAPER Special Section on Solid-State Circuit Design — Architecture, Circuit, Device and Design Methodology

Design and Calibration of a Small-Footprint, Low-Frequency, and Low-Power Gate Leakage Timer Using Differential Leakage Technique

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SUMMARY This study proposes a design and calibration method for a small-footprint, low-frequency, and low-power gate leakage timer using a differential leakage technique for IoT applications. The proposed gate leakage timer is different from conventional ones because it is composed of two leakage sources and exploits differential leakage current for the charging capacitor. This solution alleviates the inherent trade-off between small-footprint and low-frequency in the conventional gate leakage timer. Furthermore, a calibration method to suppress variations of the output frequency is proposed in this paper. To verify the effectiveness of the proposed gate leakage timer, a test chip was fabricated using 55-nm-DDC-CMOS technology. The test chip successfully demonstrates the highest figure of merit (FoM) of the product of the capacitor area ($0.072\,\mu m^2$) and output frequency (0.11 Hz), which corresponds to an improvement by a factor of 2,121 compared to the conventional one. It also demonstrates the operation with 4.5 pW power consumption. The total footprint can be reduced to be $28\,\mu m^2$, which enables low-cost and low-power IoT edges. The scaling scenario shows that the proposed technique is conducive to technology scaling.

key words: *biosensor, CMOS, healthcare IoT, low-power technique, supply sensing*

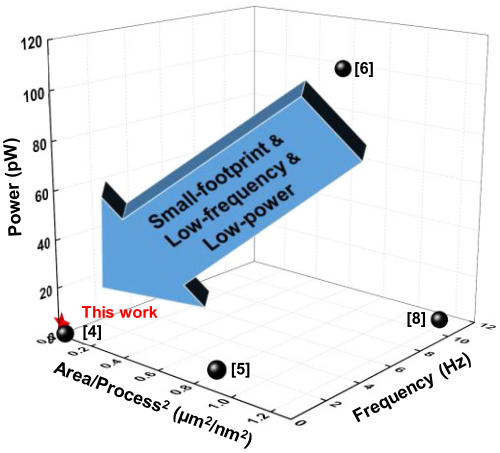

Fig. 1 Performance comparison of previously developed timers.

1. Introduction

Implantable IoT applications, such as the ingestible sensor [1], neural dust [2], [3], and body dust, have been recently developed. However, it is necessary to reduce the circuit size to implant these devices in the human body. Furthermore, the total power consumption of the system must be low because a large amount of power cannot be supplied for these implanted systems. To address this issue, we focus on the development of a small-footprint and low-frequency timer because the timer is one of the most critical components that determines the device size and total power consumption. Although many timers have been previously developed [4]–[8], they all had a technical limit for power consumption, frequency, and footprint because of the trade-off between these characteristics. However, a timer that has a small-footprint, low-frequency, and low-power consumption is in high demand for state-of-the-art implantable IoT applications. Figure 1 compares the performance of the previously developed timers. Ring oscillators are simple and easily designed, but as their output frequency decreases, the footprint and power consumption increase because the inverter stages determine frequency, footprint, and power consumption. Conventional gate leakage timers also have an inherent trade-off between circuit size and output frequency because their output frequency is determined by the ratio between the gate leakage current and capacitance of the storage capacitor. The timer proposed in this study solves the trade-off between circuit footprint, output frequency, and consumption power, as shown in Fig. 1. Compared to the conventional gate leakage timer [4], the proposed timer has achieved a smaller footprint at the same level of output frequency and power consumption. The figure of merit (FoM) (the product of total capacitor area and output frequency) of the proposed gate leakage timer is also better than the conventional one. This technique will be beneficial for cost-aware, power-aware healthcare IoT applications.

The gate leakage timer is inherently susceptible to process variations because its output frequency is determined by the ratio of the leakage current and capacitance, which strongly depends on the process variations. As one of the solutions to this problem, we introduce eFUSE to control the capacitor array, which determines the output frequency. Since extra area is required for this calibration method, we designed a small gate leakage timer that is robust in handling variations with the same level of circuit footprint as a conventional gate leakage timer.

This paper introduces a gate leakage timer using dif-

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ferential leakage techniques with calibration architecture. Compared to previous timers, the required circuit area, especially the capacitance area, can be dramatically reduced at the same level of output frequency and power consumption.

This paper describes the benefits from process scaling. In addition to the contribution in conference publication [9], the present paper introduces the calibration method for property variations because steady operation is essential for the timer, and a gate leakage timer is susceptible to the characteristic variations.

This paper is organized as follows. The proposed gate-leakage timer based on the differential gate leakage technique is introduced in Sect. 2. The calibration method is proposed in Sect. 3. The test chip design and its measurement setup are summarized in Sect. 4. Section 5 demonstrates the measurement results. The scaling scenario is introduced in Sect. 6. Finally, Sect. 7 concludes this paper.

2. Proposed Gate Leakage Timer Using Differential Gate Leakage

2.1 Concept

Figure 2 shows a conceptual diagram of the conventional and proposed gate leakage timers. Both timers consist of the leakage source, storage capacitor, and hysteresis comparator, but the proposed timer is different from the conventional one, in that the proposed timer utilizes two leakage sources and the conventional one uses only one. By using this proposed structure, it becomes possible to exploit differential leakage current.

The output frequency and capacitance of the conventional gate leakage timer have the following relationship:

$$f_{conv.} \propto \frac{I_{leak_{conv.}}}{C_{conv.}} \tag{1}$$

where $f_{conv.}$, $C_{conv.}$, and $I_{leak_{conv.}}$ are output frequency, capacitance, and leakage current from the leakage source, respectively, as shown in Fig. 2 (a). Since the output frequency of the conventional gate leakage timer is determined by the capacitance, small-footprint and low-frequency timers cannot be realized by the conventional gate leakage architecture. To solve this problem, the proposed gate leakage timer utilizes the differential leakage current for charging the capacitor. Therefore, the output frequency of the proposed gate leakage timer can be expressed as

$$f_{prop.} \propto \frac{I_{leak_{prop.top}} - I_{leak_{prop.bottom}}}{C_{prop.}} = \frac{\Delta I_{leak_{prop.}}}{C_{prop.}} \tag{2}$$

where $f_{prop.}$, $C_{prop.}$, $I_{leak_{prop.top.}}$, and $I_{leak_{prop.bottom}}$ are output frequency, capacitance, and leakage current from the top and bottom leakage sources, respectively, as shown in Fig. 2 (b). $\Delta I_{leak_{prop.}}$ is defined as the differential current of the two leakage sources, which can be much smaller than the single leakage current adopted in the conventional timer because the minimum of the differential leakage current has a weaker relationship with the process scaling than the minimum of the single leakage current. From Eqs. (1) and (2), the capacitance of the proposed gate leakage timer required to realize the same frequency as the conventional one can be derived as

$$C_{prop.} = \frac{\Delta I_{leak_{prop.}}}{I_{leak_{conv.}}} \cdot C_{conv.} \tag{3}$$

Since it is possible to make much smaller $\Delta I_{leak_{prop.}}$ than $I_{leak_{conv.}}$, the required capacitance can be much smaller than the conventional one, achieving compatibility between small-footprint and low-frequency. This is the operational principle of the proposed differential gate leakage technique.

In the conventional architecture, the storage capacitor consists of the gate capacitor of thick-gate transistor to avoid undesirable leakage current [4]. While, in our proposal, the storage capacitor consists of the thin-gate transistor, which generates large leakage current for exploiting differential leakage current. This transistor operates the storage capacitor, as well as a current source, which also contributes to the area reduction.

In addition to the small footprint, the proposed technique is advantageous from a production yield standpoint. Since the relative process variation is inherently relaxed, rather than an absolute one, our structure using two leakage sources is highly immune to process variations. Furthermore, since the circuit footprint of the proposed timer is much smaller than the conventional one, there is space to introduce the calibration architecture. This will be helpful for implementation in the variation-inevitable scaled CMOS technology, especially for the gate leakage timer, because its variations strongly depend on the process variations.

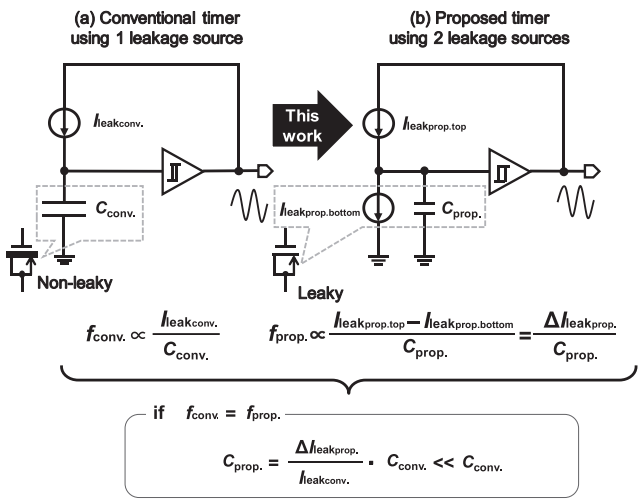

Fig. 2 Conceptual diagram of (a) conventional timer [4] and (b) proposed timer.

2.2 Schematic

Figure 3 shows the schematic diagram of the proposed timer. The fundamental structure is the same as the previous

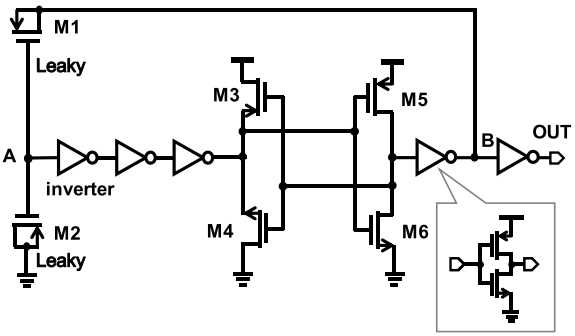

Fig. 3 Schematic diagram of the proposed timer.

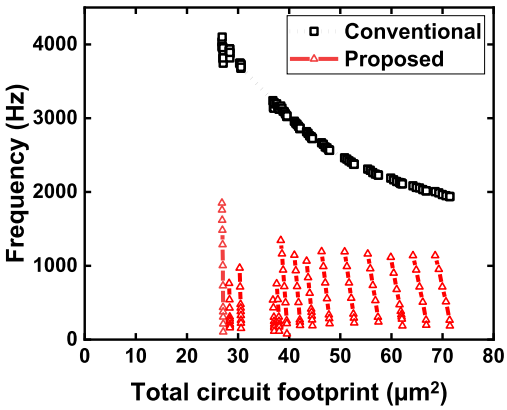

Fig. 4 Simulated results of the output frequency as a function of the footprint.

work [4]. Two leakage sources are composed of two transistors, M1 and M2. M2 functions as both a leakage source and a storage capacitor. A hysteresis comparator is composed of four transistors, M3, M4, M5, and M6. Since the modification from the conventional timer is slight, the proposed timer does not eliminate the advantages of the conventional timer, such as low power consumption and temperature stability.

In order to achieve dual leakage capability, we have adopted instead of the low-leakage thick gate transistor in the conventional timer. This modification enables the proposed differential leakage technique, which results in the reduced footprint. Optionally, the additional non-leaky capacitor, such as the thick-gate transistors and metal-insulator-metal (MIM) capacitors, can also be implemented for achieving lower output frequency. This flexibility allows scalability of the proposed technique.

2.3 Simulation

In order to verify the effectiveness of the proposed approach, SPICE simulation was performed in 55-nm-DDC-CMOS technology. Figure 4 shows the simulated frequency as a function of the footprints of the conventional and proposed timers. The supply voltage in the simulation is 0.2 V. In the conventional timer design, the method to obtain lower output frequency is increasing the capacitance of the storage capacitor, as shown in Eq. (1). Thus, there is a clear trade-

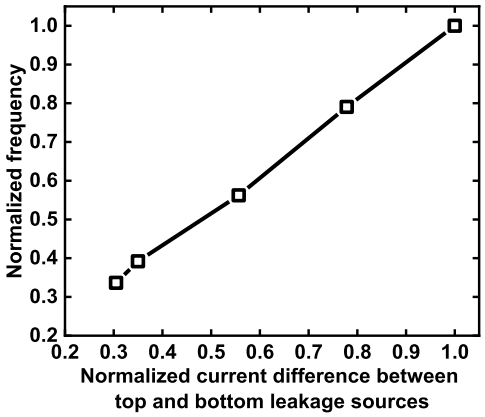

Fig. 5 Simulated results of the normalized output frequency as a function of the normalized current difference between the top and bottom leakage sources.

off between area and frequency, as indicated by the fitted curve (dotted line) in the figure. Meanwhile, our proposed sensor can resolve this trade-off. The successive dots along the same line are the same size as M1 and slightly-shifted sizes of M2. Since the output frequency of the proposed sensor is determined by the ratio of the amount of leakage currents from M1 and M2, independent of the total circuit area, low output frequency can be realized by minimizing the difference between the sizes of M1 and M2. Therefore, low output frequency can be obtained, even with a small footprint. Since the value of differential leakage current is determined by the valance between two leakage sources, steep-slope characteristics can be found. Figure 5 shows the simulated normalized output frequency as a function of the normalized current difference between the top and bottom leakage sources. As shown in Eq. (2), a linear relationship between frequency and current difference between the top and bottom leakage sources was confirmed. The results indicate the effectiveness of the proposed approach, in that, output frequency can be reduced by minimizing the differential current. Figure 5 also indicates that the proposed gate leakage timer also does not work is the current difference between top and bottom leakage sources is lower than certain level. Therefore, this value critically determines the limit of the frequency and circuit size. In addition, this minimum value is affected by the gate current mismatch.

3. Calibration Architecture

3.1 Concept and Theory

Accurate and steady operation is a necessary requirement for the timer because it is the most important component to synchronize the system. However, both the conventional and proposed gate leakage timers are susceptible to process variations. Thus, it is essential to design a calibration architecture that will ensure a robust timer for reliable applications. As a solution for this, we introduce the calibration method using an eFUSE. Figure 6 shows the proposed cali-

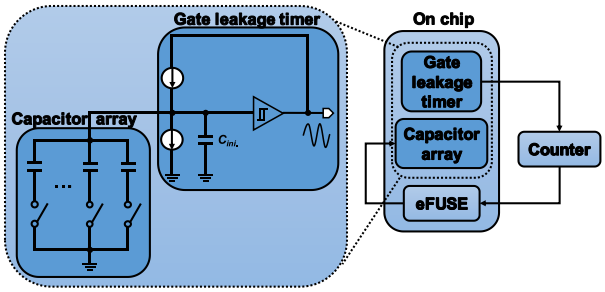

Fig. 6 Proposed calibration architecture.

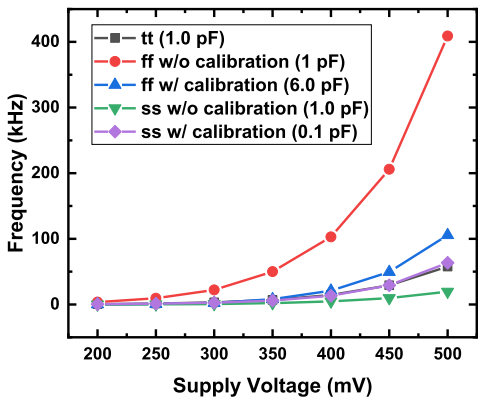

Fig. 7 Simulated results of the normalized output frequency as a function of the supply voltages.

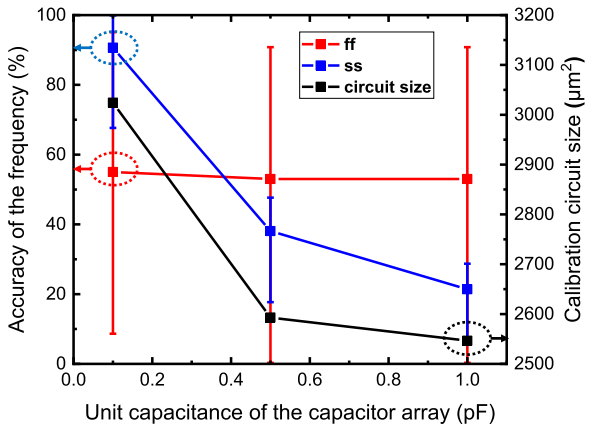

Fig. 8 Simulated results of the accuracy of the frequency as a function of the unit capacitance of the capacitor array.

bration architecture for the gate leakage timer. The calibration system is composed of the gate leakage timer described in Sect. 2, a capacitor array, a counter, and an eFUSE. The capacitor array, composed of the capacitors and switches, is used to tune the output frequency because it depends on capacitance, as shown in Eq. (2). We applied Metal-Insulator-Metal (MIM) capacitor for capacitor array to reduce the leakage current. The counter is used to diagnose and optimize the output frequency of the gate leakage timer and sends a control signal to the eFUSE. Then, the eFUSE switches the capacitor array as indicated by the counter. The gate leakage timer, capacitor array, and eFUSE are fabricated on the same chip, while the counter is off the chip. This calibration method can be used to conduct the test after manufacturing, which suppresses the process variations.

Since the additional components need to be integrated to realize this calibration method, the system size increases compared to the gate leakage timer without the calibration architecture. In this calibration method, the quantity of eFUSEs and capacitors is the same because each capacitor needs to be controlled by an eFUSE. As the quantity of capacitors connected with the small step in the capacitor array increases, the output frequency accuracy increases. However, connecting more capacitors results in a larger system size because it increases both the number of capacitors and eFUSEs. Therefore, there is a trade-off between the system size and achievable accuracy of the output frequency.

Although we conducted simulation based on the architecture in Fig. 6, it is also possible to connect a transistor array to adjust the differential current to optimize the output frequency. By substituting the transistor array for the capacitor array, it is possible to make a calibrated gate leakage timer with a smaller footprint. In the conventional gate leakage timer, only the capacitor array can be used as the calibration element because the output frequency is determined only by the capacitance, as shown in Eq. (1), while the proposed gate leakage timer can be tuned by both the capacitance and differential current. This is the advantage of the proposed gate leakage timer from the viewpoint of the circuit footprint. In general, however, controlling the differential current is more difficult than controlling the capacitance because it is more delicate. Therefore, if increasing the system size is permitted, the capacitor array is better.

3.2 Simulation

Figure 7 shows the simulated results of the output frequency as a function of the supply voltages. We conducted virtual calibration by changing the capacitance of the storage capacitor at the steady step,0.1 pF in this case, and adopted the optimized output frequency. The simulated results before calibration shown in Fig. 7 imply that the output frequency of the gate leakage timer greatly varies with the process variations. After conducting calibration, the steady output frequency can be realized, as shown in Fig. 7.

Figure 8 shows the simulation results that quantitatively explains the trade-off between accuracy and footprint of the proposed calibration scheme. Although there are variations with corners, as unit capacitance of the capacitor becomes smaller, the accuracy of the frequency increases, while the calibration circuit size also increases. However, considering the fact that the consumption power is mainly determined by the output frequency of the timer and the circuit size of the timer is relatively small compared with other components of the system, the advantages which the proposed calibration architecture provides outweigh the dis-

advantages of the additional footprint. Assuming that the size of the eFUSE is 9.3 μm^2/bit [10], the size of the simulated circuit exceeds the conventional gate leakage timer. However, considering that the conventional also needs to be calibrated, the advantages provided by the calibration are justified because a timer with a steady and accurate operation is essential for reliable IoT applications. Furthermore, the excess area is comparable to the size of the conventional gate leakage timer [4].

4. Test Chip Design and Measurement Setup

4.1 Test Chip Design

In order to verify the effectiveness of the proposed technique, a prototype test chip was designed and fabricated using 55-nm-DDC-CMOS technology. Since this chip was designed without a calibration architecture, a chip designed with calibration should be fabricated and measured in the future. Figure 9 shows a microphotograph and layout of the test chip. The footprint was 28 μm^2, which corresponds to 1/17 of the conventional timer [4]. The capacitor area is 0.072 μm^2, which corresponds to 1/3333 of the conventional timer [4]. The layout was performed based on the standard cell. By introducing a fully manual layout, further area reduction can be achieved.

4.2 Measurement Setup

The measurement was performed using a probe station by a manual probing method. The power supplies were generated and measured by a precision source/measure unit (B2901A, Keysight Technologies). The output frequency was measured with a sampling oscilloscope (TDS 7404, Tektronix Inc.).

5. Results and Discussion

5.1 Measurement Results

Figure 10 shows the measured waveform of the proposed gate leakage timer. Since the designed circuit had minimum components to optimize for low-frequency operation, the output waveform is not stable. However, by designing with more margin, the more stable output waveform can be obtained. Figure 11 shows the measured output frequency as a function of the supply voltage of the proposed timer. The proposed timer successfully achieved 0.11 Hz when the supply voltage was 0.290 V. Due to the imperfection of the measurement setup, the supply voltage that achieves an identical frequency is relatively higher than that from the simulation results. By introducing a low-power-DDC-CMOS process, a low-power operation of 4.5 pW was achieved. Since the output frequency of the proposed timer is determined by the balance between the two leakage currents from two leaky transistors, the output frequency depends on the supply voltage. As shown in Fig. 11 the measured results show a steep slope that is consistent with this assumption, which supports the effectiveness of the proposed approach.

Ten chips were measured and all successfully functioned with performance variations. Detailed analysis of the immunity to the process, voltage, and temperature (PVT) variation will be investigated in future work. However, since the proposed circuit topology is similar to the conventional one [4], PVT variation is expected to be identical. Furthermore, the same countermeasures can be applied. By intro-

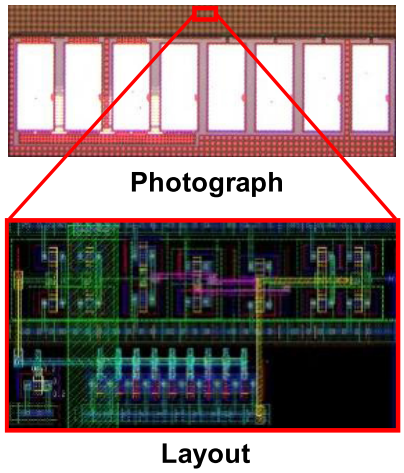

Fig. 9 Test chip microphotograph and layout.

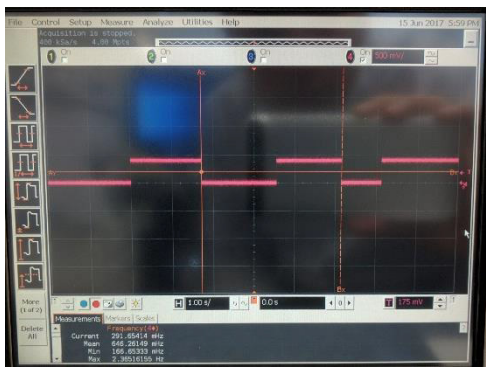

Fig. 10 Measured waveform of the proposed gate leakage timer.

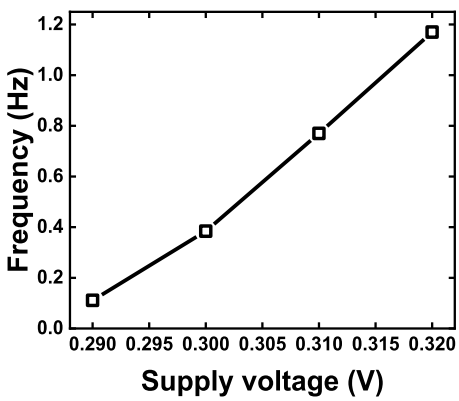

Fig. 11 Measured output frequency as a function of the supply voltage.

Table 1 Performance comparison.

	CICC'07[4]	VLSI'15 [11]	JSSC'16 [12]	This work
Frequency [Hz]	0.07	18	2.8	0.11
Process	130 nm CMOS	180 nm CMOS	65 nm CMOS	55 nm DDC CMOS
Supply voltage [V]	0.3	0.6	0.5	0.29
Power consumption [pW]	1	4.2	44.4	4.5
Total area [μm^2]	480	N/A	25550	28
Area of capacitance [μm^2]	240	N/A	N/A	0.072
FoM(Total)*1 [Hz•μm^2]	33.6	N/A	71540	3.08
FoM(Total_Proc.)*2 [Hz•μm^2/nm^2]	0.00199	N/A	16.93	0.00102
FoM(Cap.)*3 [Hz•μm^2]	16.8	N/A	N/A	0.0792

*1 FoM(Total) = Frequency [Hz] • Total area [μm^2]
*2 FoM(Total_Proc.) = Frequency [Hz]•Total area [μm^2]/Process[nm^2]
*3 FoM(Cap.) = Frequency [Hz] • Capacitor area [μm^2]

ducing the calibration method shown in Sect. 3, the PVT variations can be suppressed and optimized, and reliable frequency can be generated for the system under any conditions.

5.2 Performance Evaluation

Performance comparison to the conventional gate-leakage timers [4], [11], [12] is summarized in Table 1. The circuit footprint dramatically reduced and it worked at the same level of output frequency. Therefore, the proposed gate leakage timer successfully solved the trade-off between the circuit footprint, output frequency, and power consumption, achieving compatibility between them. Furthermore, our timer outperforms the conventional one from the viewpoint of the FoMs, i.e., the products of the total or capacitor area and output frequency. The proposed sensor achieved 10.9/2121-times improvement in the FoMs compared with conventional gate-leakage timer [4]. The proposed technique will be helpful for developing the next-generation low-power consumption, yet low-cost IoT edges. Furthermore, by integrating the calibration architecture, a more reliable timer for IoT applications can be realized.

6. Scaling Scenario

This section presents a scaling scenario of the proposed circuit architecture. The proposed differential leakage technique is conducive to process scaling. Figure 12 shows the scaling scenario of the conventional and proposed timers. In this scaling scenario, the following assumptions were utilized:

1. Non-capacitor area is ideally scaled.
2. Currents flowing into the capacitor are constant in each process node.
3. Output frequency is determined by only capacitance and current flowing into the capacitor.

As shown in Fig. 12, in the future scaled CMOS process node, the proposed technique becomes more advantageous over the conventional timer. As technology scaling advances, the performance gap between the conventional and proposed timer becomes greater. The reason is that the capacitor footprint becomes relatively larger as the transistor becomes smaller. Since the capacitor footprint of the proposed timer is less dominant than that of the conventional one, the proposed technique is much more conducive to process scaling.

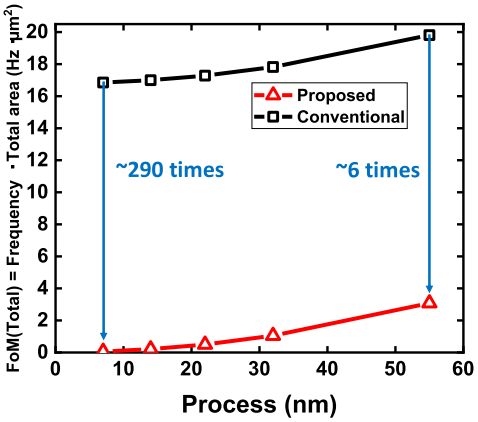

Fig. 12 Scaling scenario.

7. Conclusion

The goal of this work was to realize a small-footprint, low-frequency, and low-power gate leakage timer. The measured results using a 55 nm-DDC-CMOS prototype successfully demonstrated the highest FoM of the product of the capacitor area ($0.072\,\mu m^2$) and output frequency (0.11 Hz), that corresponds to an improvement by a factor of 2,121 over the conventional one. The measured power is 4.5 pW and the total footprint can be reduced to $28\,\mu m^2$, which enables low-cost and low-power IoT edges. The simulated results show that the proposed timer is conducive to technology scaling. Since the gate leakage timer is susceptible to the process variations, the calibration method to compensate for these variations was also proposed in this paper. The proposed calibration architecture is beneficial for realizing an accurate and steady timer for reliable IoT applications.

Acknowledgments

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