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Recent Progress in the Development of Large-Capacity Integrated Silicon Photonics Transceivers

Yu TANAKA[†,††,†††a)], ***Member***

SUMMARY We report our recent progress in silicon photonics integrated device technology targeting on-chip-level large-capacity optical interconnect applications. To realize high-capacity data transmission, we successfully developed on-package-type silicon photonics integrated transceivers and demonstrated simultaneous 400 Gbps operation. 56 Gbps pulse-amplitude-modulation (PAM) 4 and wavelength-division-multiplexing technologies were also introduced to enhance the transmission capacity.

key words: *silicon photonics, optical interconnection, wavelength division multiplexing*

1. Introduction

Recently, transmission bandwidths have rapidly increased inside and/or between data centers for realizing futuristic 5G internet of things (IoT) systems [1], [2]. The ability to lower power consumption and system costs while simultaneously facilitating higher bandwidth are inevitable requirements for these systems. In addition, the computing capability in high performance computing systems continues to increase [3]–[5]. In the above-mentioned scenario, the use of optical interconnects is a promising solution for handling ever-increasing data demand along greater than a few hundred-meter distances via single mode fiber (SMF) transmission [6].

Silicon photonics is a promising technology to enhance the bandwidth and reduce costs due to its advantages in providing optical devices with small foot-print based on mature complementary metal oxide semiconductor (CMOS) technologies.

Recently, Luxtera demonstrated high-performance silicon-photonics-based 100 Gbsp parallel single mode (PSM) transceivers targeting applications in data centers with transmission distances of 500 m to 2 km [7]. On the other hand, for interconnections between data centers with a target transmission distance of approximately 80 km, Acacia developed 200 Gbps (30 GBaud, 16 quadrature amplitude modulation (QAM)) silicon-photonics-based integrated transceivers for digital coherent device applications [8]. As mentioned above, the silicon photonics technologies have been intensively applied in the fields of telecommunication and data communication networks. In particular, high-density assembly techniques for high-capacity data transmission will be expected to establish with the merge of silicon photonics and high-density flip-chip bonding techniques with very narrow bump pitches.

In this paper, we discuss the recent progress in the research and development of high-density and high-capacity optical transceivers based on silicon photonics and novel assembly technologies. In Sect. 2, we will describe the evolution of optical interconnection configuration between boards and large scale integration (LSI) chips. The necessities of "on-package-type" interconnection will also be discussed. In Sect. 3, high-density and large-capacity silicon-photonics-based optical transceivers we have developed so far will be introduced. Particularly, attention will be focused on assembly techniques that form "bridge structure" which mitigates the influence of power and signal integrities. In Sect. 4, the pulse amplitude modulation (PAM) 4 technologies in short will be discussed to increase the aggregate bandwidth in a single lane. An effective method for producing PAM 4 signals on silicon photonics chips will be described, resulting in significantly reduced power consumption. Another way to increase the aggregate bandwidth is by using the wavelength division multiplexing (WDM), and this will be introduced in Sect. 5. Finally, we will conclude the paper.

2. Requirements for Higher Bandwidth Interconnection

Currently, available data rates of optical transceivers are as high as approximately 25 Gbps. In addition, transmission standards such as the IEEE Ethernet and Infiniband require higher speeds up to 50 Gbps or 100Gbps per lane [9], [10]. To increase the data rate to the standards mentioned above, the length of the electrical waveguide must be shortened due to the drastically increased electrical losses. In these situations, the entire interconnection configuration will also must be improved to accommodate the increased data speed. The existing so-called board-edge-type transceiver form factor, such as quad small form-factor pluggable (QSFP) form factor, will be replaced by an on-board-type transceiver form factor to increase the data rate. This is because it can be placed closer to the I/O terminals (SerDes) of the CPU chips as well as decrease the electrical losses and power con-

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[†]The author is with Photonics Electronics Technology Research Association (PETRA), Tsukuba-shi, 350–8569 Japan.
[††]The author is with Fujitsu Laboratories Limited, Atsugi-shi, 243–0197 Japan.
[†††]The author is with Fujitsu Limited, Kawasaki-shi, 211–8588 Japan.
a) E-mail: yu_tanaka@fujitsu.com

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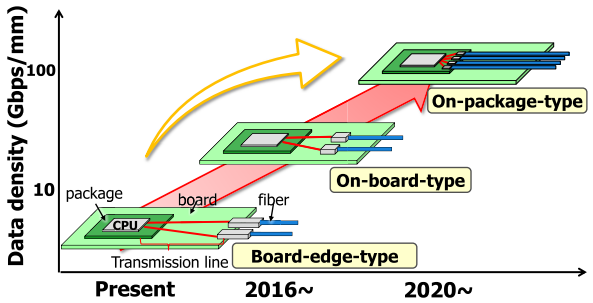


Fig. 1 Evolution of the high-bandwidth interconnection.

sumption. The specifications and requirements for applications using these on-board-type transceivers were argued at the relevant consortium [11]. Furthermore, to realize future high-performance computing with transmission data of more than 10 Tbps per node, the distance between CPUs and optical transceivers must be drastically decreased and the transceiver should be placed closer to the CPU chips on the same package substrate. This type of optical interconnection is a so-called on-package-type transceiver.

Figure 1 shows a schematic of the evolution of optical interconnection with respect to the transceiver form factor to accommodate the increased data rates. Regarding on-package-type transceivers, since the CPU and transceivers are mounted on the same package substrate (the thick green area in Fig. 1), it can mitigate the limited transmission bandwidth by the wide bump pitch between the package and board substrates (the thin green area). Using on-package-type transceivers, we can increase the transmission bandwidth and realize large-capacity interconnections.

3. High-Density and Large-Capacity Integrated Transceivers

3.1 On-Package-Type 400G (16 ch × 25 Gbps) Transceivers

To realize high-density integrated transceivers which can deal with higher transmission bandwidths, we proposed a chip-scale on-package-type optical transceiver structure [12]. The use of silicon photonics technologies is promising for realization of the above-mentioned high-density optical transceiver structure. Many optical functional elements such as modulators, photodetectors, and waveguides can be densely integrated using conventional CMOS technology. Using these advanced silicon photonics technologies and assembly techniques, we developed a novel transceiver configuration called a "bridge structure" [13]. This structure is composed of bonded chips on the surface of a package substrate. It realizes high-density chip-scale assembly and very short electrical signal line lengths between the CPUs and electric integrated circuit (EIC) to function as transceivers on a surface of package substrate. Here, the EIC consists of drivers (DRV) for high-speed optical modulators and transimpedance amplifiers (TIA) for high-speed photodetectors with high responsivity. Furthermore, this structure can reduce power consumption since the compensating circuits such as decision feedback equalizers (DFEs) to recover distorted electrical waveforms at higher data rates are not required.

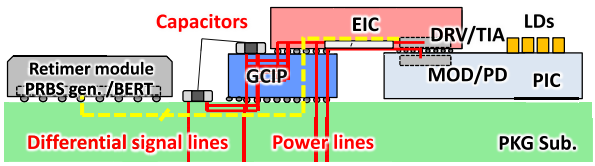


Fig. 2 Schematic structure of the 16 ch × 25 Gbps on-PKG-type silicon photonics TRx.

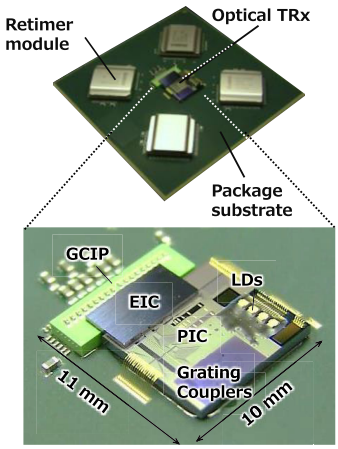


Fig. 3 Photographs of the fabricated on-package-type transceiver on a package substrate.

We developed a prototype of the on-package-type transceiver targeting 400 Gbps (16 channel × 25 Gbps) operation [14]. A schematic illustration of the structure of the device is shown in Fig. 2. The "bridge structure" composed of the EIC and photonic integration circuits (PIC) with a glass ceramic interposer (GCIP) enables the optical transceiver engine to be mounted on a conventional flat package surface without any voids on the package substrate. Our goal was to realize aggregate 400 Gbps using high speed data rates of 25 Gbps per lane.

Figure 3 shows a photographs of the assembled prototype optical transceiver engine on the package substrate. A highly integrated and assembled structure with a small footprint of 10 mm × 11 mm was realized. Here, four retimer modules surrounding the optical transceiver engine function as the 16 channel pseudo random bit sequence (PRBS) data generators and bit error rate testers (BERTs) for evaluating transmission characteristics. In each lane for the 16 channel transceiver, high-speed Mach–Zehnder-type modulators with push-pull p-n junctions and waveguide-type germanium photodetectors were densely formed on the PIC. Control lines to receive signal from the monitor photodetectors were wire-bonded at the PIC. Here, a total of four 4 channel laser diode (LD) arrays to generate optical signals were placed on the same PIC and precisely mounted

on the terraces formed on the PIC with accurate alignment marks. In addition, grating couplers (GCs) were used as optical input/output ports. A single-polarization-type GC for the transmitter and polarization-splitting-type GCs for the receiver were also used. By forming this "bridge structure", we successfully realized the high density transceiver. The bandwidth density at the edge of the PIC was estimated to be 40 Gbps/mm achieving the highest value reported to date. We think that the "bridge structure" may overcome the bandwidth limits that may be caused by the conventional wire-bonding assembly techniques. In the "bridge structure", the bump pitches could be the limit of the bandwidth density. Furthermore, the total bandwidth density may be made larger by increasing the aggregate data rate in a single lane to ~80–100 Gbps/mm.

To realize the simultaneous 16 channel operation in this high-density configuration, the signal and power integrities must be carefully designed. To suppress reflections and crosstalk noise from the channels, characteristic impedance for all signal lines between the DRV and TIA inside the EIC and retimer modules were set at 100 Ω differential signal lines even inside the transmission lines on EIC and the vias inside a GCIP. Moreover, to reduce the simultaneous switching noise arising from fluctuations of the EIC driving voltage at simultaneous operation, we optimized the target impedances for the transmitter and receiver power lines. In addition, the impedance was reduced by placing the chip capacitors on the GCIP. The power lines for the transmitter and receiver were also completely separated inside the package substrate to protect the receiver signals from noise generated by the transmitter signals with large peak-to-peak amplitude voltages.

3.2 Simultaneous 16 Channel Operation

Using the above-mentioned on-package-type transceiver, we measured the clear optical eye diagrams for the transmitter and electrical BER eyes for the receiver at 25 Gbps PRBS $2^7 - 1$ non-return-to-zero (NRZ) signals. The eye diagrams of all transmitter channels are shown in Fig. 4. Bit error rate measurements were also conducted, and the results are shown in Fig. 4. Error free operation (BER < 1×10^{-12}) at the simultaneous 16 channel for the transmitter measurements was successfully confirmed. The total crosstalk penalties during simultaneous 16 channel operation were estimated to be 1.4 dB, which is very small considering the high-density assembly configuration.

Receiver performance was also examined using the 25 Gbps NRZ input signal generated by the LiNbO3 modulators with a $2^{31} - 1$ PRBS pattern. We confirmed the BER eyes of the receiver during the simultaneous 16-ch operation as shown in Fig. 5. Here, the horizontal and vertical axes indicate the unit interval (40 ps) and amplitude (250 mV), respectively. The white area indicates regions with a BER < 10^{-6}. Moreover, we investigated the BER characteristics of ch_10 while changing the number of the other channels and the results are shown in Fig. 5 (b). The sensitivity marginally degraded and the crosstalk penalty was estimated to be 1.4 dB while operating all channels.

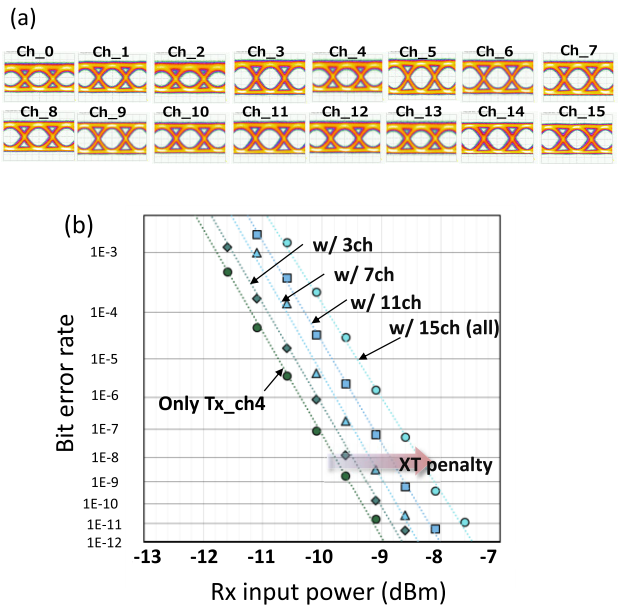


Fig. 4 (a) Optical eye diagrams of the transmitter channels and (b) the sensitivity changes of ch_4 during multichannel transmitter operation. The total crosstalk penalty between transmitters is estimated to be 1.4 dB.

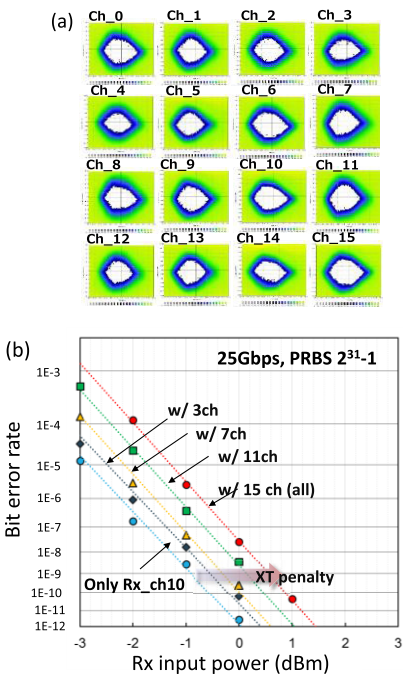


Fig. 5 (a) BER eyes of each channel during simultaneous 16-ch operations and (b) BER characteristics of Rx multichannel operations. The total Rx-to-Rx crosstalk penalty was 1.4 dB.

The measured total power for the transmitter circuit including the driver and modulator was measured to be 1995 mW. The total power for the receiver circuit including the TIA and PD was 367 mW. Here, the power for the driver and TIA was dominant in the above estimation. As a con-

sequence, the operation power efficiency was determined to be 4.99 and 0.92 mW/Gbps for the transmitter including the LD power and receiver, respectively. Finally the total power efficiency of the device was estimated to be 5.91 mW/Gbps.

4. The 56 Gbps PAM4 Transmitters

Furthermore, we recently developed other key technologies to enhance the aggregated bandwidth using the silicon photonics technologies. In terms of power efficiencies of the transmitter circuits, 4.99 mW/Gbps was high compared to other reported values which are listed in a previous paper [14]. To reduce the transmitter circuit power and realize higher data rates, we developed a novel low power silicon photonics four level pulse-amplitude modulation PAM 4 modulator [15].

The fabricated silicon photonics chip and 28 nm CMOS driver chip were flipchip bonded as shown in Fig. 6. On both chips, 100 μm pitch bump pads were fabricated. The area required for a single channel PAM4 transmitter was as small as 450 $\times$ 900 μm. The modulator consisted of a p-i-n junction phase shifter (carrier injection) with a RC passive equalizer. The lengths of the p-i-n phase shifters were 500 μm for most significant bit (MSB) and 250 μm for least significant bit (LSB).

In Fig. 7, the output waveforms for 40, 50, and 56 Gbps PAM4 operation are shown. The total bias current of the MSB and LSB segments was 1.1 mA at a single arm which was relatively large to avoid the insufficient eye-opening due to the nonlinear behavior in the low-bias condition. The transmitter exhibited clear eye-opening at every data rate tested. The four modulation levels of the PAM4 eye diagram are almost equally spaced. The outer extinction ratios were 5.3, 5.0, and 4.7 dB for the 40, 50, and 56-Gbps operations, respectively, with total power consumptions of 72.2, 73.5, and 88.9 mW, respectively, corresponding to record-high energy efficiencies of 1.59–1.81 mW/Gbps. This efficiency is the highest achieved to the best of our knowledge.

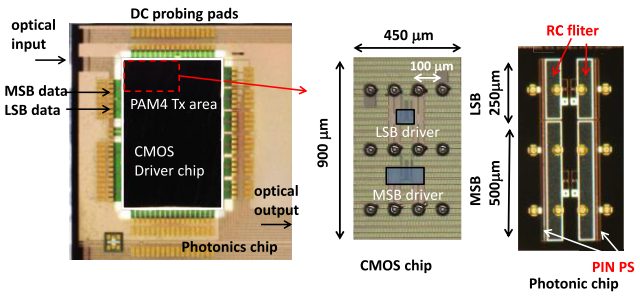


Fig. 6 Layout of the silicon photonics integrated PAM4 transmitter.

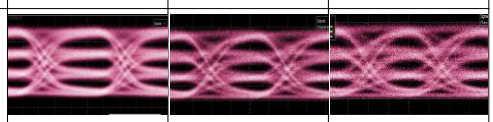
Data rate (Gbps)	40	50	56
Eye Diagram			
Outer ER (dB)	5.3	5.0	4.7
Power Efficiency (mW/Gbps)	1.81	1.67	1.59

Fig. 7 The 40, 50, and 56 Gbps PAM4 optical eye waveforms.

5. Silicon Photonics WDM Technologies and Integrated Transceivers

Toward a much higher bandwidth, advanced optical technology such as WDM is a promising candidate for enhancing aggregate bandwidth and reducing assembly costs associated with connecting optical fibers [16]. We have developed next-generation silicon photonics WDM transceivers consisting of several active devices, including optical sources, modulators and photodetectors. In addition, passive devices, such as optical multiplexers/demultiplexers (MUX/DeMUX) and grating couplers as the optical interface with SMFs in transmitters and receivers, have been reported [17]–[24].

Here, we introduce silicon photonics device technologies for WDM optical interconnection focusing on silicon-nanowire-waveguide-based optical MUX/DeMUX technologies based on multistage cascade-connected delayed Mach-Zehnder interferometers (DMZIs).

Optical (De)MUX performance, such as insertion loss (IL), spectral crosstalk (XT) and undesired operating window shift (OWS), usually deteriorate with fabrication imperfections and temperature changes on silicon substrates. Especially, to dynamically cope with the unwanted OWS, tunability is required in the WDM transceiver. In general, silicon-wire (De)MUX operates only for a single polarization due to the relatively large birefringence of the waveguide. However, in terms of launching into the DeMUX at the receiver side, inability to maintain the constant state of polarization (SOP) in SMFs complicates WDM signal operation. Here, we report novel Si-wire DMZI-type DeMUX schemes that can overcome the abovementioned challenges.

5.1 WINC-Based DMZI-DeMUX for Large Fab Tolerance

High-precision CMOS processes enabled the minimization of phase noise in DMZI-DeMUXs, allowing us to obtain low XT and IL. However, it is difficult to circumvent dimension errors, which lead to productivity deterioration. We successfully overcame this technical barrier by making the DeMUX response less sensitive to dimension fluctuations by using the structure shown in Fig. 8. The wavelength insensitive coupler (WINC) scheme has a much wider 3dB splitting spectral range than conventional directional couplers by inserting the additional phase shift of 048 π rad to the upper arm waveguide [25]. Therefore, we minimized the degradation of IL and XT over a broad wavelength range greater than 100 nm.

For the fabricated silicon-wire-based DMZI-DeMUX,

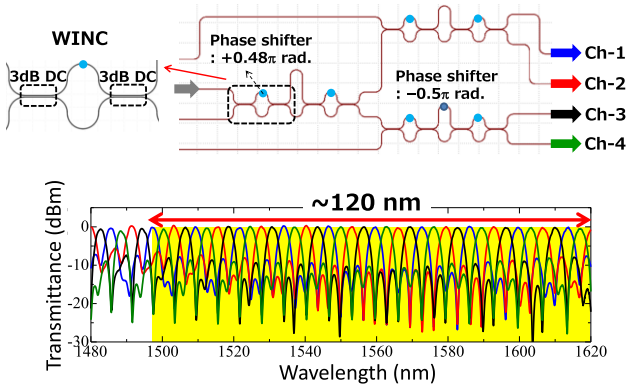


Fig. 8 Layout and measured spectra of the WINC-based DMZI-DeMUX for improved fabrication tolerance.

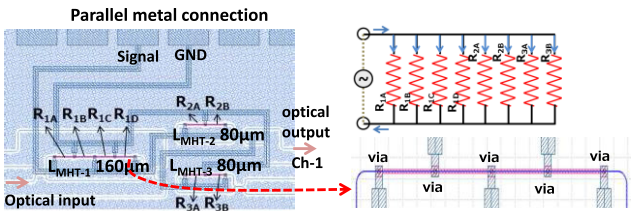


Fig. 9 Tunable DMZI-DeMUX for low-voltage driving.

we achieved a clear filter response of < −10dB over > 120-nm-wide spectral range [22], which is approximately two times wider than that of DC-based DeMUX.

5.2 Tunable DMZI-DeMUX with a Low Driving Voltage

The flatband DeMUX approach is a good method for coping with fabrication imperfections or external temperature changes that cause the OWS. An alternative way to overcome this problem involves tuning the operating window using micro-heaters (MHT) [22]. Figure 9 shows a schematic of the MHT-mounted DMZI-DeMUXs. By mounting TiN-based resistors on the upper side of each DMZI, the operating window can be tuned to the longer-wavelength side, depending on the voltage applied to the MHT. For both cases, heater lengths were set to 160 μm for $L_{MHT\text{-}1}$ and 80 μm for both $L_{MHT\text{-}2}$ and $L_{MHT\text{-}3}$ to maintain constant phase matching between the multiple DMZIs.

Usually, the resistance (R_{MHT}) of each MHT increases proportionally with increasing L_{MHT}. Thus, if we connect each MHT serially, the voltage required for driving tuning (V_{MHT}) inherently increases. In this case, considering heater driving by a CMOS-based circuit, a V_{MHT} of > 3 V would limit the available tuning range. To overcome this problem, we modified the heater metallization to form a parallel connection instead of a serial connection.

For the fabricated tunable DMZI-DeMUX, we achieved full free-spectral range (FSR) tuning of 24.2 nm span by applying a V_{MHT} of 2.5 V. It should be noted that the excess loss was negligible for the FSR tuning.

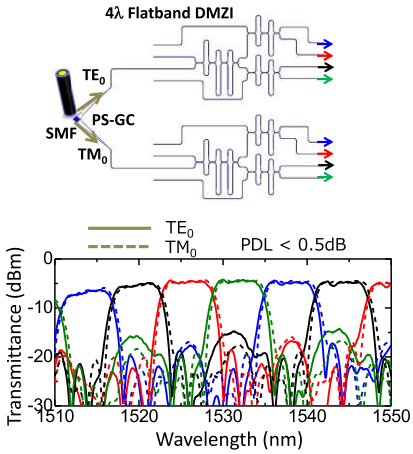


Fig. 10 Polarization diversified DMZI-DeMUX at the receiver side.

5.3 Polarization Diversified DMZI-DeMUX

As shown in Fig. 10, we also developed the polarization diversified scheme by combining a polarization splitting grating coupler (PS-GC) and a pair of silicon-wire 1 × 4 channel DMZI-DeMUXs. The PS-GC containing square-lattice circular-type scatterers works as a polarization splitter. Each 1 × 4 channel DMZI-DeMUX was identically designed for flattening the spectral response [22]. It should be noted that the DMZI-DeMUX designed for use in the polarization diversified scheme is not restricted to flatband type devices.

The spectra of the fabricated polarization diversified DMZI-DeMUX integrated with the PS-GC exhibited nearly identical spectral characteristics irrespective of the SOP of the input signal. The polarization dependent loss and operating window deviation for the device were estimated to be <1.0 dB and <0.4 nm, respectively. Monolithically integrating high-speed Ge-based photodetectors and TIA [14] with the DMZI-DeMUX arrays allowed for the detection of WDM optical signals with an arbitrary SOP through CMOS electronic circuitry.

5.4 WDM Integrated Transceivers and 25 Gbps × 4λ Operation

Recently, 100 Gbps error-free WDM signal transmission was experimentally demonstrated in the integrated transceiver assembly in which 25Gbps × 4λ modulators and photodetector arrays, tunable MUXs/DeMUXs and grating coupler arrays are monolithically integrated in a silicon photonics platform [24]. Figure 11 shows the top-view of this fabricated WDM transceiver assembly.

To operate the PIC chip, a CMOS-based EIC chip including driver and TIA was electrically assembled on the PIC by solder bumping technologies similarly to the aforementioned technique. The operating window of each WDM grid for the parallel-MHT-connection-based tunable MUXs/DeMUXs integrated with Ge monitor photodetectors were automatically adjusted by the external control circuits.

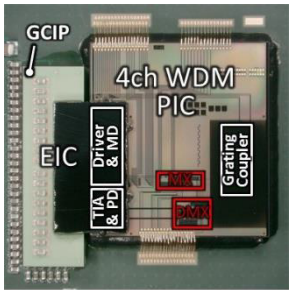


Fig. 11 Polarization diversified DMZI-DeMUX at the receiver side.

The signal quality of the WDM transceiver assembly was evaluated using co-mounted retimer modules acting as both pattern generators and error detectors for the 25 Gb/s electrical signals. Through signal transmission from Tx to Rx, we successfully observed error-free operation (BER $< 5 \times 10^{-13}$) for all output channels.

6. Conclusions

Recent progress in silicon photonics integrated device technologies targeting on-chip-level large-capacity optical interconnect applications was described in detail. To realize high-capacity data transmission, we successfully developed the on-package-type silicon photonics integrated transceivers and demonstrated simultaneous 400 Gbps operation. In addition, 56 Gbps PAM4 and WDM technologies were introduced to enhance transmission capacity. The on-package-type transceiver configuration is efficient way for achieving high-capacity transmission since it possibly reduces the influence of the limited bandwidth by the wide bump pitches and drastically increased electrical losses due to enhanced aggregate bandwidth in a single lane.

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Yu Tanaka is currently a senior researcher at PETRA. He received his PhD degree in material science from the Tokyo Institute of Technology, Tokyo, Japan in 2000. In 2002, He joined Fujitsu Laboratories, Atsugi, Japan. Since then, he has been involved in development of many optical devices which include quantum dot lasers and photonic-crystal-based optical switches. He joined the photonics electronics technology research association (PETRA) in 2012. He is currently engaged in the development and commercialization of integrated silicon-photonics-based optical transceivers.