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Toward Scalable Superconducting Quantum Computer Implementation

Yutaka TABUCHI[†a)], ***Nonmember***, **Shuhei TAMATE**[†], ***Member***, ***and*** **Yasunobu NAKAMURA**[†,††], ***Nonmember***

SUMMARY In this paper, we briefly review the concept of superconducting quantum computers and discuss their hardware architecture. We also describe the necessary technologies for the development of a medium-scale quantum computer with more than tens of thousands of quantum bits.

key words: *superconducting quantum computers, quantum information processing*

1. Introduction

In the recent years, the development of quantum computers has been accelerated. In parallel with the research in universities, the enormous efforts in industry such as in Google, IBM and Intel have dramatically increased the number of integrated quantum bits (qubits). It is anticipated to realize quantum computers exceeding a few hundred qubits in several years. As of June 2018, Google has realized quantum computers up to 22 qubits [1] and demonstrated its operation with the lowest error rate of 1% per gate in their 9-qubits device [2]. IBM has also realized quantum computers up to 20 qubits; those up to 16 qubits are open to the world through a free cloud service, and the 20-qubit one is for commercial use [3].

While those prototype quantum computers are highlighted in daily news articles, it may require some time to realize a fully fault-tolerant quantum computer. In this paper, we briefly review the basic operation principle of a qubit, and introduce a hardware architecture of superconducting quantum computers and its implementation. Furthermore, we discuss the technologies required for medium-scale quantum computers which provide several error-tolerant "logical" qubits with more than ten thousands of physical qubits and with the error rate below 0.1% [4].

2. Quantum Bits and Gates

Bits in conventional computers take binary values of 0 or 1. A bit is represented, in a DRAM device for example, with a level of voltage caused by the presence or absence of millions of electrons on a capacitor. Figure 1 (a) illustrates the representation of a bit. The voltage is conditioned above or below thresholds to express logical 0 or 1. Due to the presence of the thresholds, the logical bit values are inherently robust against noise.

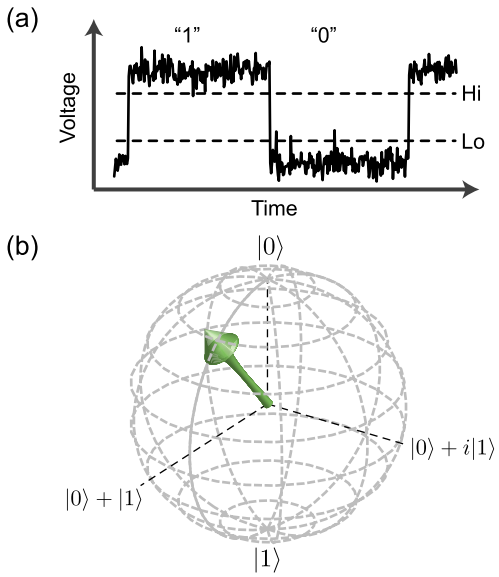

Fig. 1 Representations of a bit and a quantum bit. (a) When a conventional bit is represented by a voltage value, threshold values are used for binarization of the state, and the logical "0" or "1" is assigned. It is robust against noise in the voltage. (b) A quantum bit is binarized by observation. In the Bloch sphere representation, the binary values determined by the measurement are associated with the north and south poles of the sphere. The *xy*-coordinates of the sphere represent the coherence of the quantum states, i.e., a superposition state of logical "0" and "1". The quantum mechanical state before the measurement is expressed by a point on the sphere.

Quantum bits are the information units in quantum computers. Information of a qubit is carried by a physical system having two relevant and selectively accessible energy eigenstates as the qubit basis states. The examples include a spin 1/2, a tunnel-coupled double quantum dots with a single electron, a superconducting island (loop) capturing and releasing a Cooper pair (magnetic flux quantum) [5], and a vacuum and a single boson state of a collective excitation mode. Quantum mechanics allows not only the individual eigenstates but also the superposition of the two states. A useful representation of a qubit is shown in Fig. 1 (b). Similar to the conventional bits, qubits also take a definite binary values of 0 or 1, but only after a measurement operation for extracting the result. We assign the state after the measurement to the north or south pole of the

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[†]The authors are with Research Center for Advanced Science and Technology, The University of Tokyo, Tokyo, 153–8904 Japan.
[††]The author is with Center for Emergent Matter Science, RIKEN, Wako-shi, 351–0198 Japan.
a) E-mail: tabuchi@qc.rcast.u-tokyo.ac.jp

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sphere depending on the binarized outcome and express it as $|0\rangle$ or $|1\rangle$ using a ket vector. A pure state of the qubit is represented by a point on the surface. For example, a superposition state $(1/\sqrt{2})(|0\rangle + \exp(i\phi)|1\rangle)$ is represented by a point on the equator. States with different superposition phases ϕ are distinguished by the longitudinal difference. These states give binary values with the equal probabilities of 50% after a measurement. More generally, the state $\sqrt{p}|0\rangle + \sqrt{1-p}\exp(i\phi)|1\rangle$ gives a probability of p of finding logical 0 after a measurement. When the qubit is disturbed by the noise from the surrounding environment, the state becomes a mixed state. A mixed state is represented by a point inside the sphere in Fig. 1 (b). The latitude still corresponds to the probability of the logical outcomes after a measurement.

A conventional logic gate is a circuit that outputs the resultant logical value as a voltage (Fig. 2). The circuit is strongly nonlinear with respect to the input signals and is robust against the noise in the inputs. In quantum computation, in contrast, although the final outcomes are binarized by measurements, superposition states need to be maintained during the computation. The inputs and outputs of quantum logic gates are quantum states. As shown in Fig. 1 (b), a quantum state refers to one point on the sphere, which is parametrized by analog values that require infinite precision. In addition to added errors to the output due to the finite precision of quantum gates, input errors propagate to the output. Since quantum mechanics requires quantum gates to have linear input-output relations, it is not possible for quantum gates to possess error resilience as in conventional logic gates.

In quantum mechanics, observation gives strong nonlinearity to the input-output relation of quantum states because the measurement collapses the wavefunction and projects it either on the north or south pole on the sphere representing the quantum state. Quantum error correction is a scheme that extracts temporal and spatial information of the errors occurring in a group of qubits as a set of binary values obtained by measurements while maintaining the superposition states necessary for quantum computation [4]. Through the measurements, the analog errors are discretized into digital errors. Thus, the application of a finite number of quantum gates is sufficient for the error correction.

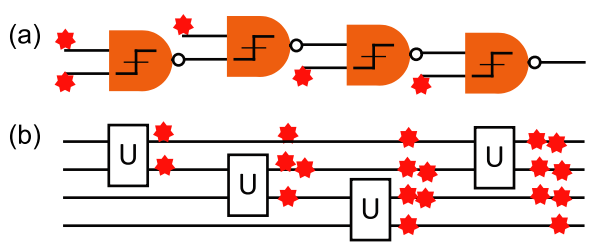

Fig. 2 Conventional and quantum logic gates. (a) Conventional gates have thresholds inside, i.e., output voltages are binarized with respect to the thresholds, so that the noise (marked with stars) does not affect the logical output. In other words, it is a circuit which has strong nonlinearity in input-output relation. (b) Quantum gates are analog circuits in which the input and output are linearly related in the unitary operations. The noise at the input directly influences the output.

3. Superconducting Qubits

Superconducting qubits were initially demonstrated using the degree of freedom of a single Cooper-pair charge confined in a superconducting electrode [6]. Thereafter, qubits using different degrees of freedom, such as the magnetic flux in a superconducting loop and the superconducting phase between a Josephson junction, have been developed [5]. Superconducting qubits called "transmons" [7], which evolved from charge qubits, are widely used today because of their relatively good coherence properties.

Figure 3 (a) depicts a typical single-qubit superconducting device as an example. The transmon qubit here consists of two concentric electrodes bridged by a Josephson junction. The state of the qubit is controlled through a coaxial microwave line from the backside of the substrate. The coplanar waveguide resonator coupled to the qubit is used to readout the state of the qubit.

Figure 3 (b) shows the corresponding equivalent circuit of the device. The capacitor C_q composed of the concentric circular electrodes and the Josephson junction form a nonlinear LC resonator since the junction can be approximated as a nonlinear inductance L_q. The resonance frequency of

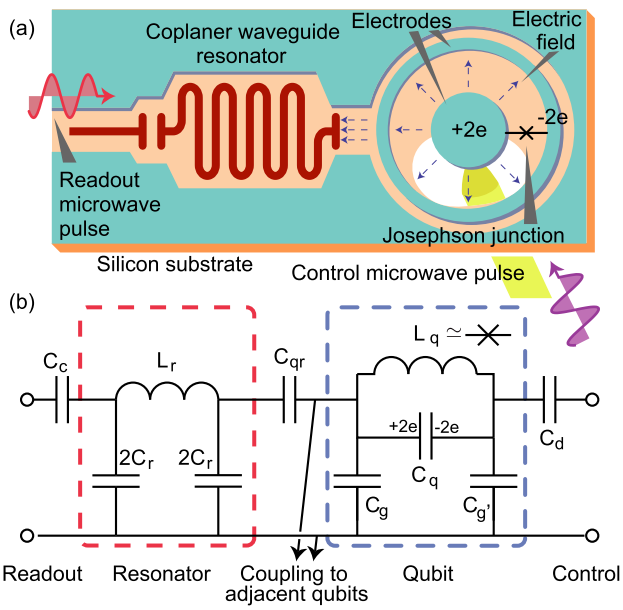

Fig. 3 (a) Schematic illustration of a qubit design. (b) Corresponding equivalent circuit. The device is fabricated on a silicon substrate and consists of a qubit and a readout resonator in a single unit. Here we employ a qubit with concentric electrodes and with a single Josephson junction (marked with a cross) and control it from the backside of the substrate through the capacitor C_d to allow the scalability. The outer electrode is used for coupling to a readout resonator and other qubits. Each qubit is coupled to the readout resonator via the capacitor C_{qr}, and the qubit state is mapped, as described in Sect. 4, to the carrier phase of a readout pulse which is introduced through the capacitor C_c. Two arrows in the equivalent circuit indicate electrodes for capacitive coupling to other qubits.

the LC resonator is designed to be around 4–8 GHz, and the capacitance C_q is about 50 fF. Whereas the nonlinear LC resonator has a nearly harmonic potential, a frequency difference arises, in the quantized energy states, between the transition frequency of the ground state and the first excited state and that of the first and second excited states. Such a frequency difference allows selective controls of only the ground state and the first excited state as an effective two-level system, i.e., a qubit.

There are a few different approaches for transmon-qubit implementation in planar circuits. Qubits are usually surrounded by the superconducting ground electrodes. In Google's design [2], one electrode of the transmon qubit is grounded ($C_{g'} \to \infty$). On the other hand, in the designs used by IBM [8] and Delft University of Technology [9], both of the electrodes are floated with respect to the ground, and the two capacitances are equal, i.e., $C_g = C_{g'}$. There is another approach using concentric circular electrodes without ground plane on chip, where their sample package serves as a ground [10], [11]. We employ asymmetric ground coupling capacitors $C_g \gg C_{g'}$ to the on-chip ground electrodes (Fig. 3 (a)) in order to suppress crosstalk between qubits. Crosstalk currents from neighboring electrodes when driving the adjacent qubit can flow into the ground electrode via the capacitor C_g, so that the crosstalk voltage between the qubit electrodes reduces. In other words, the outer ring shields the inside of the qubit.

4. Basic Operations in Superconducting Quantum Computers

Figure 4 shows a block diagram of a superconducting quantum computer. Similar diagrams have also been reported in refs [12], [13]. Basic operations of superconducting quantum computers are comprised of four parts, i.e., initialization, control, measurement and post signal processing in a conventional computer. Superconducting qubits are initialized in a refrigerator, controlled by the waveform generators and microwave modulators, which implement quantum gates and measurement operation, and readout by the microwave demodulators (Fig. 4). The readout signal is further post processed by the conventional computers to implement quantum error correction protocol, or user applications. Here, we detail former three parts of the operations.

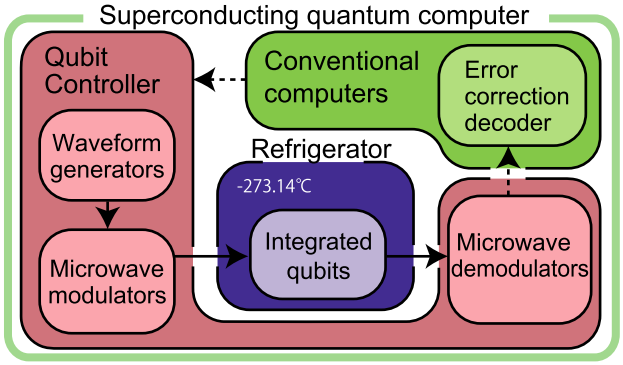

Fig. 4 Schematic diagram of a superconducting quantum computer. The integrated qubits are cooled down close to the absolute zero temperature using a dilution refrigerator and placed in a magnetic shield to eliminate the effect of magnetic-field fluctuations. Analog microwave modulators and demodulators from 4–12 GHz are used to implement quantum gates and measurements. Decoding of the quantum error correction code, that is, estimation and correction of the errors, is performed by conventional computers or dedicated circuits. Quantum algorithms and applications of interest are loaded into the conventional computers.

(1) Initialization

An integrated qubit unit is designed to be controllable with microwave pulses with the carrier frequencies of 5–10 GHz. It is cooled down close to the absolute zero temperature (~0.01 K) using a dilution refrigerator to minimize the electromagnetic noise due to blackbody radiation at the qubit frequency. The integrated qubit unit is a passive circuit that does not work autonomously, and all the control and measurement are performed with room temperature electronics.

(2) Control

Quantum gates are composed of a series of microwave pulses. For ideal quantum computation, only infinitesimal analog errors can be tolerated in the microwave pulses, whereas the condition is relaxed to the error rate of approximately 0.5% under error correction protocols[†]. The microwave pulses are generated by high-speed digital-to-analog converters, which modulate microwave carrier signals. The pulses are then introduced to the integrated qubit unit to implement quantum gates. In order to improve the latency between the room temperature electronics and the low temperature device and in order to reduce the number of wiring which increases with the number of qubits, a part of the room temperature electronics could be substituted by single flux quantum logic circuits operated at a low temperature stage [14].

(3) Measurement

Microwave pulses are also used for qubit measurement. The measurement pulse interacts with a qubit through a microwave resonator. The carrier phase of the reflected pulse depends on the state of the qubit; for example, the phase is unchanged when the state of the qubit is $|0\rangle$, and the phase is shifted by 180 degrees when the state of the qubit is $|1\rangle$. The pulse energy for a single measurement is c.a. 6 attowatts·μs (aW·μs), which is too weak to be detected in a single-event measurement with a state-of-the-art cryogenic semiconductor amplifier with the typical noise power density of 50 aW·μs. Instead, superconducting parametric amplifiers provide near quantum-limited amplification corresponding to the noise power density around 3 aW·μs at 10 GHz, and have been used to amplify tiny signals for qubit measurements [15]. Broadband parametric amplifiers have also been extensively studied for frequency-multiplexed simultaneous readout of several qubits [16]–[18].

[†]The value is the error threshold required for the quantum error correction [4]. An error rate that is sufficiently smaller than the threshold allows efficient computation.

5. Technological Requirements for Medium-Sized Quantum Computers

A layered architecture of quantum computers has been proposed by Jones *et al*. [12]. They defined layers of the architecture of an entire quantum computer. For the hardware part, from the lowest level, they introduced the physical layer, the virtualization layer, and the quantum error correction layer. In order to realize a scalable quantum computer, the following technologies are necessary in the hardware layers. The first is the technology to manufacture a large array of qubits, and the second is the technology to maintain the accuracy of gates in the integrated circuits. Finally, controllers and computing units at room temperature need to be scalable as well.

Technologies for making a two-dimensional (2D) array of qubits, which are required in most of the state-of-the-art quantum error correction protocols, include three-dimensional wiring, heat load control, miniaturization of peripheral circuits [14], [16], [17], [19], and so on. For quantum bits integrated in a 2D array, it is necessary to wire the control and readout lines perpendicularly to the substrate. As the quality of qubits is deteriorated by the materials with large dielectric loss, the conventional multilayered wiring technology cannot be easily adapted. Currently, many groups are employing superconducting flip-chip bonding with a vacuum gap [1], [20], [21]. In addition, superconducting through silicon vias (TSVs) to guide signals to the backside of the substrate and silicon multilayered interposers for their wiring have also been demonstrated [9], [20]. For the peripheral circuits, it is necessary to miniaturize and integrate the currently centimeter-sized components such as circulators used for qubit readout. In addition, it is desirable to develop "address decoders" (such as demultiplexers, matrix switches and so on) operating at cryogenic temperature in order to perform space, frequency and time multiplexing of control and readout signals. However, from the viewpoint of the accuracy discussed below, it requires analog microwave technologies much more advanced than those commonly used in digital applications.

Technologies for maintaining accuracy in the physical layer include improvement of the coherence, suppression of crosstalk and spurious electromagnetic modes, high precision of control microwave pulse waveforms, and stabilization of carrier phases. Error mitigation methods that make errors less likely to occur are included in the virtualization layer, and techniques for correcting errors are included in the quantum error correction layer. In order to run an error correction protocol on a quantum computer, it is necessary to reduce the error rate to a value far below the threshold, for example, 0.1% per gate or less at the stage of the virtualization layer. An issue in the physical layer is to improve the accuracy of the waveform; it is necessary to simultaneously reduce the impedance mismatch that can become noticeable as the complexity in the circuits and packaging such as the use of TSVs and multilayered substrates increases. Moreover, it is necessary to suppress the deterioration of the waveform due to nonlinearity of the active elements, the number of which may increase with the automation of control, by employing a digital predistorter [22], [23], for example. An example of control methods in the virtualization layer is known as quantum optimal control [24], [25]. By introducing such method that is robust to waveform deformation, errors in the quantum gates are reduced.

6. Conclusion

We have argued that quantum computers require an error correction mechanism during the computation by considering the difference between conventional and quantum bits. We have also illustrated an implementation of a superconducting quantum bit and enumerated the necessary technologies for scalling-up in the near future. By acquiring them one by one, a fault-tolerant quantum computer will be realized.

References

[1] K.D. Kissell, "An Update on Google's Quantum Computing Initiative Fine Kernel Tool Kit System." http://www.teratec.eu/library/pdf/forum/2018/Presentations/Forum_Teratec_2018_A3_06_Kevin_Kissel_Google.pdf.
[2] J. Kelly, R. Barends, A.G. Fowler, A. Megrant, E. Jeffrey, T.C. White, D. Sank, J.Y. Mutus, B. Campbell, Y. Chen, Z. Chen, B. Chiaro, A. Dunsworth, I.-C. Hoi, C. Neill, P.J.J. O'Malley, C. Quintana, P. Roushan, A. Vainsencher, J. Wenner, A.N. Cleland, and J.M. Martinis, "State preservation by repetitive error detection in a superconducting quantum circuit," Nature, vol.519, pp.66–69, 2015.
[3] IBM Q, Experience, https://quantumexperience.ng.bluemix.net/qx/devices.
[4] A.G. Fowler, M. Mariantoni, J.M. Martinis, and A.N. Cleland, "Surface codes: Towards practical large-scale quantum computation," Phys. Rev. A, vol.86, no.3, 032324, 2012.
[5] M.H. Devoret and J.M. Martinis, "Implementing qubits with superconducting integrated circuits," Quantum Inf. Process., vol.3, pp.163–203, 2004.
[6] Y. Nakamura, Y.A. Pashkin, and J.S. Tsai, "Coherent control of macroscopic quantum states in a single-Cooper-pair box," Nature, vol.398, pp.786–788, 1999.
[7] J. Koch, T.M. Yu, J. Gambetta, A.A. Houck, D.I. Schuster, J. Majer, A. Blais, M.H. Devoret, S.M. Girvin, and R.J. Schoelkopf, "Charge-insensitive qubit design derived from the Cooper pair box," Phys. Rev. A, vol.76, no.4, 042319, 2007.
[8] M. Takita, A.W. Cross, A.D. Córcoles, J.M. Chow, and J.M. Gambetta, "Experimental demonstration of fault-tolerant state preparation with superconducting qubits," Phys. Rev. Lett., vol.119, no.18, 180501, 2017.
[9] R. Versluis, S. Poletto, N. Khammassi, B. Tarasinski, N. Haider, D.J. Michalak, A. Bruno, K. Bertels, and L. DiCarlo, "Scalable quantum circuit and control for a superconducting surface code," Phys. Rev. Applied, vol.8, no.3, 034021, 2017.
[10] J. Braumüller, M. Sandberg, M.R. Vissers, A. Schneider, S. Schlör, L. Grünhaupt, H. Rotzinger, M. Marthaler, A. Lukashenko, A. Dieter, A.V. Ustinov, M. Weides, and D.P. Pappas, "Concentric transmon qubit featuring fast tunability and an anisotropic magnetic dipole moment," Appl. Phys. Lett., vol.108, no.9, 032601, 2016.
[11] J. Rahamim, T. Behrle, M.J. Peterer, A. Patterson, P.A. Spring, T. Tsunoda, R. Manenti, G. Tancredi, and P.J. Leek, "Double-sided coaxial circuit QED with out-of-plane wiring," Appl. Phys. Lett.,

vol.110, no.22, 222602, 2017.
[12] N.C. Jones, R. Van Meter, A.G. Fowler, P.L. McMahon, J. Kim, T.D. Ladd, and Y. Yamamoto, "Layered architecture for quantum computing," Phys. Rev. X, vol.2, no.3, 031007, 2012.
[13] J.M. Gambetta, J.M. Chow, and M. Steffen, "Building logical qubits in a superconducting quantum computing system," npj Quantum Inf., vol.3, p.2, 2017.
[14] R. McDermott, M.G. Vavilov, B.L.T. Plourde, F.K. Wilhelm, P.J. Liebermann, O.A. Mukhanov, and T.A. Ohki, "Quantum-classical interface based on single flux quantum digital logic," Quant. Sci. Tech., vol.3, no.2, 024004, 2018.
[15] R. Vijay, D.H. Slichter, and I. Siddiqi, "Observation of quantum jumps in a superconducting artificial atom," Phys. Rev. Lett., vol.106, 110502, 2011.
[16] J.Y. Mutus, T.C. White, R. Barends, Y. Chen, Z. Chen, B. Chiaro, A. Dunsworth, E. Jeffrey, J. Kelly, A. Megrant, C. Neill, P.J.J. O'Malley, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, K.M. Sundqvist, A.N. Cleland, and J.M. Martinis, "Strong environmental coupling in a Josephson parametric amplifier," Appl. Phys. Lett., vol.104, no.26, 263513, 2014.
[17] C. Macklin, K. O'Brien, D. Hover, M.E. Schwartz, V. Bolkhovsky, X. Zhang, W.D. Oliver, and I. Siddiqi, "A near–quantum-limited Josephson traveling-wave parametric amplifier," Science, vol.350, no.6258, pp.307–310, 2015.
[18] T. Roy, S. Kundu, M. Chand, A.M. Vadiraj, A. Ranadive, N. Nehra, M.P. Patankar, J. Aumentado, A.A. Clerk, and R. Vijay, "Broadband parametric amplification with impedance engineering: Beyond the gain-bandwidth product," Appl. Phys. Lett., vol.107, no.26, 262601, 2015.
[19] B. Abdo, K. Sliwa, L. Frunzio, and M. Devoret, "Directional amplification with a Josephson circuit," Phys. Rev. X, vol.3, no.3, 031001, 2013.
[20] D. Rosenberg, D. Kim, R. Das, D. Yost, S. Gustavsson, D. Hover, P. Krantz, A. Melville, L. Racz, G.O. Samach, S.J. Weber, F. Yan, J.L. Yoder, A.J. Kerman, and W.D. Oliver, "3D integrated superconducting qubits," npj Quantum Inf., vol.3, p.42, 2017.
[21] W. O'Brien, M. Vahidpour, J.T. Whyland, J. Angeles, J. Marshall, D. Scarabelli, G. Crossman, K. Yadav, Y. Mohan, C. Bui, V. Rawat, N. Renzas, Russ andVodrahalli, A. Bestwick, and C. Rigetti, "Superconducting caps for quantum integrated circuits," arXiv:1708.02219, 2017.
[22] H. Jaeger and H. Haas, "Harnessing nonlinearity: Predicting chaotic systems and saving energy in wireless communication," Science, vol.304, no.5667, pp.78–80, 2004.
[23] P. Varahman, Z. Atlasbaf, and N.V. Heydarian, "Adaptive digital predistortion for power amplifiers used in CDMA applications," 2005 Asia-Pacific Conference on Applied Electromagnetics, p.4, 2005.
[24] A.P. Peirce, M.A. Dahleh, and H. Rabitz, "Optimal control of quantum-mechanical systems: Existence, numerical approximation, and applications," Phys. Rev. A, vol.37, no.12, pp.4950–4964, 1988.
[25] N. Khaneja, T. Reiss, C. Kehlet, T. Schulte-Herbrüggen, and S.J. Glaser, "Optimal control of coupled spin dynamics: design of NMR pulse sequences by gradient ascent algorithms," J. Magn. Reson., vol.172, pp.296–305, 2005.

Yutaka Tabuchi received the B.S., M.S. and D. Eng. from Osaka University in 2008, 2009 and 2012, respectively. He is now a research associate at The University of Tokyo.

Shuhei Tamate received the B.S., M.S. and D. Eng. from Kyoto University in 2008, 2010 and 2013, respectively. During 2014–2017, he worked at National Institute of Informatics. He is now a project research associate at The University of Tokyo.

Yasunobu Nakamura received the B.S., M.S. and D. Eng. from The University of Tokyo in 1990, 1992 and 2011, respectively. During 1992–2012, he worked at NEC Corporation. He is now a professor at The University of Tokyo. He is also a team leader at Center for Emergent Matter Science in RIKEN.