PAPER

Transient Characteristics on Super-Steep Subthreshold Slope "PN-Body Tied SOI-FET" —Simulation and Pulse Measurement—

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SUMMARY In this study, the transient characteristics on the super-steep subthreshold slope (SS) of a PN-body tied (PNBT) silicon-on-insulator field-effect transistor (SOI-FET) were investigated using technology computer-aided design and pulse measurements. Carrier charging effects were observed on the super-steep SS PNBT SOI-FET. It was found that the turn-on delay time decreased to nearly zero when the gate overdrive-voltage was set to 0.1–0.15 V. Additionally, optimizing the gate width improved the turn-on delay. This has positive implications for the low speed problems of this device. However, long-term leakage current flows on turn-off. The carrier lifetime affects the leakage current, and the device parameters must be optimized to realize both a high on/off ratio and high-speed operation.

key words: *feedback, floating body effect, pulse measurement, SOI MOSFET, steep subthreshold slope, thyristor, transient*

1. Introduction

Technologies for the Internet of Things (IoT) and for artificial intelligence (AI) systems have been rapidly growing in importance, with the goal of a highly automated society, such as industry 4.0 [1] and society 5.0 [2]. IoT and AI systems require large quantities of computing devices, such as large-scale integrated circuits (LSIs) and sensors, and their power consumption has become an important issue. Therefore, it is preferable that these devices operate with ultra-low power.

To reduce the power consumption of LSIs, the subthreshold slope (SS) of the metal-oxide semiconductor field-effect transistor (MOSFET) is a key parameter. Recently, various types of steep SS devices have been proposed to overcome the fundamental SS limitation of a conventional MOSFET (60 mV/dec at room temperature). For example, tunnel field-effect transistors (FETs) [3], [4] and negative capacitance FETs [5], [6] have been extensively researched for the development of ultralow power LSIs. However, their experimentally obtained SSs have not been sufficiently low. As an alternative, the super-steep SS of the PN-body tied (PNBT) silicon-on-insulator field-effect transistor (SOI-FET), which has a symmetrical source/drain structure and shows the super-steep SS direct current (DC) characteristics of SS < 1 mV/dec over several orders of the drain current I_d, has been proposed [7], [8]. Additionally, we have researched the application of the PNBT SOI-FET to energy harvesting application devices [9]. The super-steep SS of our device is assumed to come from the floating-body effect, and from the conduction mechanism of the inherent thyristor structure. Both mechanisms are generally expected to have low-speed concerns because the carrier charging into the body (channel) region, which is a key mechanism of the floating-body effect, results in a delay, and the minority-carrier lifetime limits the operation speed of the thyristor. Therefore, it is very important to evaluate the transient effect on PNBT SOI-FET. In this study, the transient characteristics of the super-steep SS PNBT SOI-FET are investigated using technology computer-aided design (TCAD) and pulse measurements. We show the transient effect on the PNBT SOI-FET and the carrier dynamics in the simulated device. It was found that optimizing the gate width (W_g) and adjusting the gate overdrive voltage could reduce the turn-on delay time. However, the flow of long-term leakage current on turn-off is an issue in the PNBT SOI-FET. This paper is based on Ref. [10] and Ref. [11], and included the detailed explanation and the additional data.

2. Device Structure and Experimental Setups

Figure 1 shows the device structure of the PNBT SOI-FET. It consists of a conventional floating-body partially-

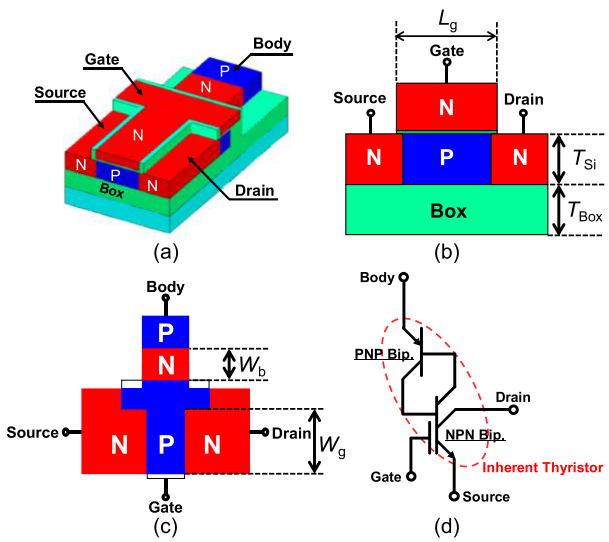


Fig. 1 Structure of PNBT SOI-FET: (a) bird's eye view, (b) front view, (c) top view, (d) schematic of PNBT SOI-FET, which has an inherent thyristor structure.

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Table 1 WGFMU key specifications [12].

Measurement Range	1 μA	1 mA
Minimum Measurement Window	1.64 μs	40 ns
Settling Time	37 μs	200 ns
Noise Level	425 pA	280 nA
Minimum Rise/Fall Time	70 ns	

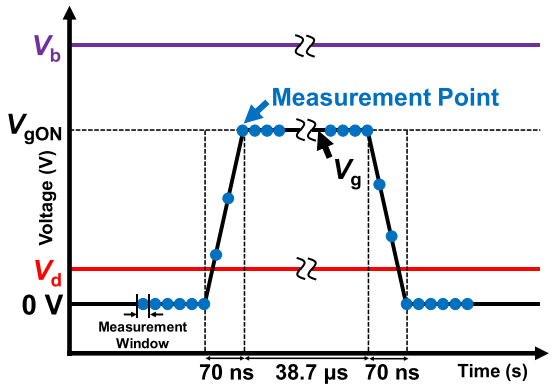


Fig. 2 Pulse waveform applied to the devices.

depleted SOI-FET in the source-to-drain direction, and a p-n-p bipolar junction transistor in the neutral-body (channel)-region-to-body-terminal direction, as shown in Figs. 1 (a)–1 (c). This means that the PNBT SOI-FET contains an n-p-n-p thyristor between the source/drain and the body terminal, as per the schematic shown in Fig. 1 (d). The actual devices were fabricated using a LAPIS semiconductor 0.2-μm silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) process with 50 nm-thick SOI (T_{Si}), a 200 nm buried oxide (Box) (T_{Box}), a 4.4 nm-thick gate oxide (T_{ox}), 0.2 or 1 μm gate length (L_g), and a 1.2 μm n-region (base) width (W_b). The gate has a T-shape to maintain the overlay accuracy according to the layout rules of the process that we used [8], [9]. We used a Keysight B1500A semiconductor device parameter analyzer with a waveform generator/fast measurement unit (WGFMU) for DC and pulse measurements. Table 1 shows the key specifications of the WGFMU [12]. We measured the I_d of the 40 ns or 1.64 μs time slot (measurement window as shown in Table 1) when introducing the pulse gate voltage (V_g) with a constant drain voltage (V_d) and body voltage (V_b) as shown in Fig. 2. A 3D TCAD "HyENEXSS" [13]–[15] was used to analyze the current below the measurement limitation, and to measure the carrier dynamics in the PNBT SOI-FET. The Shockley–Read–Hall (SRH) generation/recombination, Auger recombination, and band-to-band tunneling model were used, and the carrier lifetime parameters in the SRH model were set to the default lifetime × 0.02 to fit the measurement results [16]. The concrete values are shown in the appendix.

3. Results and Discussions

First, the DC and transient characteristics were compared between the conventional floating-body SOI-FET (L_g = 0.2 μm) and the PNBT SOI-FET. Figure 3 shows the measured I–V_g characteristics of the floating-body and PNBT SOI-FETs. The PNBT SOI-FET produces a super-steep SS (= 0.6 mV/dec) when V_b = 1.0 V. In our previous studies, the idea that the super-steep SS is induced by the positive feedback of the floating-body effect, and that the thyristor plays an important role in injecting carriers from the body terminal to the body (channel) region was proposed [7]–[9]. While a conventional floating-body SOI-FET can also induce a super-steep SS [17], [18], this would require the impact ionization phenomenon; thus, a super-steep SS does not occur in the floating-body SOI-FET at V_d = 0.1 V. In the n-channel PNBT SOI-FET, the electrons diffusing from the source to the base (n-region) decrease the base potential, and this induces the injection of holes from the body terminal to the body (channel) region, as shown in Fig. 4. The PNBT SOI-FET has hysteresis characteristics, as shown in Fig. 3 (a). This is also induced by the floating-body effect. In this study, the hysteresis width is smaller than the pulse swing (0–V_{gON}). Additionally, the PNBT SOI-FET needs the V_b, and the body current I_b flows from the body terminal to the source as shown in Fig. 3 (b). I_b is smaller than I_d; thus, the body power consumption may be lower than the drain power consumption. However, the body current in the CMOS with the PNBT SOI-FET is a leakage current [19]. Hence, we need to consider this issue further. The operation mechanism of the PNBT SOI-FET is similar to that of other metal-oxide semiconductor (MOS) gate-controlled n-p-n-p devices, such as feedback FETs [20]–[23] and Z^2-FETs [24]–[26]. However, the inherent thyristor plays only a subsidiary role in the PNBT SOI-FET. The main current flows along the source-to-drain direction.

We define the V_g at which I_d = 1 μA flows as the turn-on trigger V_g in pulse measurements, as shown in Figs. 3 (c) and 3 (d). Figure 5 shows the measured waveform of I_d, when the gate turns on (V_g = 0 V to trigger V_g) and off (V_g = trigger V_g to 0 V). The turn-on characteristics shown in Fig. 5 (a) were measured in the 1 mA range because it has the shortest minimum measurement window and settling time in the selectable WGFMU range. On turn-on, a near-zero delay was observed with the floating-body SOI-FET. This can be expected, because the gate delay of the 0.2 μm MOSFET technology is below 1 ns [27]. This suggests that the WGFMU data below the settling time, which are used in later measurement results, are also expected to be reliable. In contrast, a delay of approximately 500 ns was observed with the PNBT SOI-FET. These are clear data due to be over the settling time. The delay is considered due to the time taken by the carriers charging into the body (channel) region, and it poses a problem, limiting the operation speed of the PNBT SOI-FET.

The turn-off characteristics shown in Fig. 5 (b) were measured in the 1 μA range to measure the transient low leakage current level. It was noted that the time resolution of the 1 μA range was lower than that of the 1 mA range. The turn-off characteristics just after the off state could not

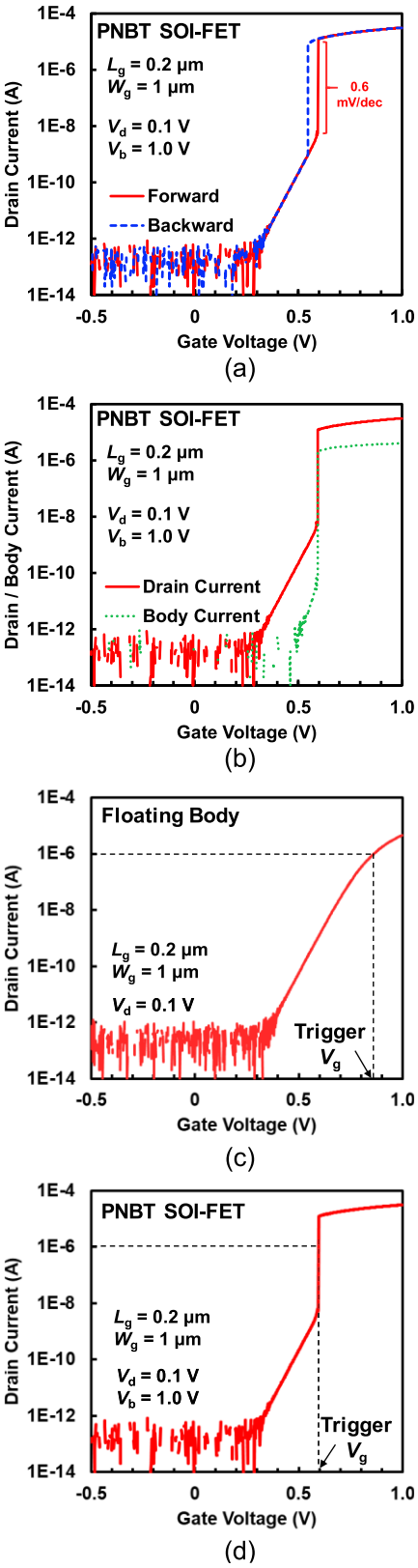


Fig. 3 Measured I–V_g characteristics. (a) Double sweep I_d–V_g characteristics of the PNBT SOI-FET, and (b) I_d and I_b–V_g characteristics of the PNBT SOI-FET. Definition of trigger V_g on (c) the floating-body SOI-FET, and (d) the PNBT SOI-FET.

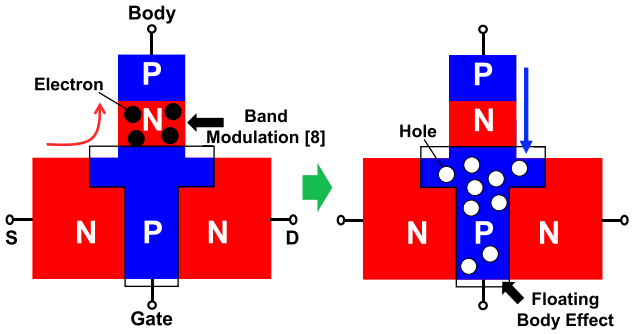


Fig. 4 Illustration of super-steep SS mechanism on PNBT SOI-FET.

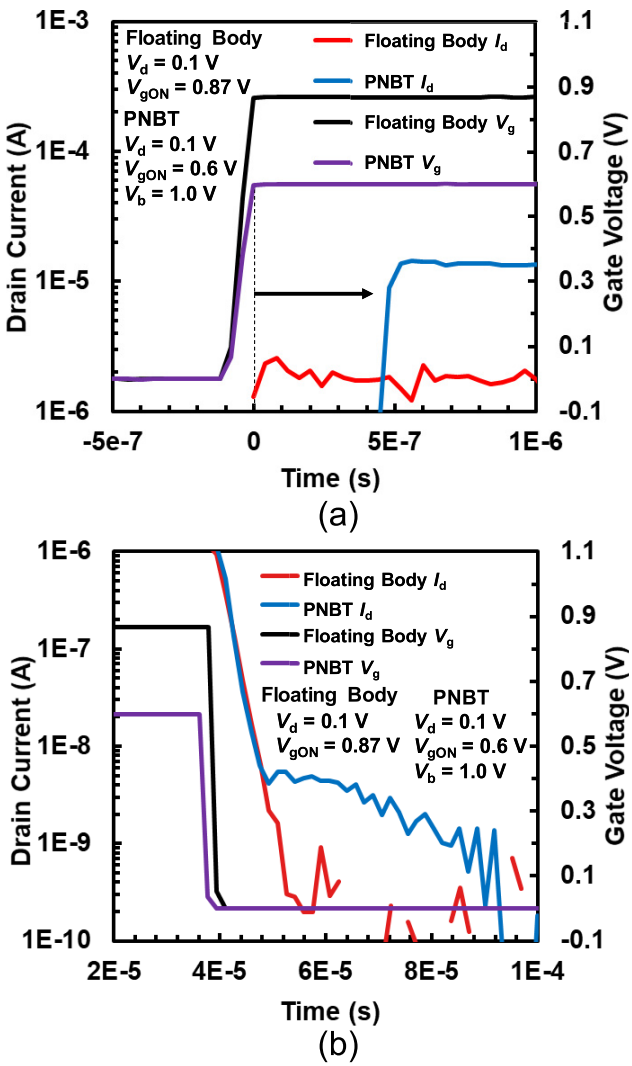


Fig. 5 Measured waveform of turn-on (a) and turn-off (b) leakage current of I_d with both floating-body SOI-FET and PNBT SOI-FET.

be ascertained because of measurement limitations. However, leakage current flow at 50–100 μs was observed with the PNBT SOI-FET, but was not observed in the floating-body SOI-FET. It is considered due to the carrier discharging from the body (channel) region. These data are also expected to be reliable because, as expected, the SOI-FET has

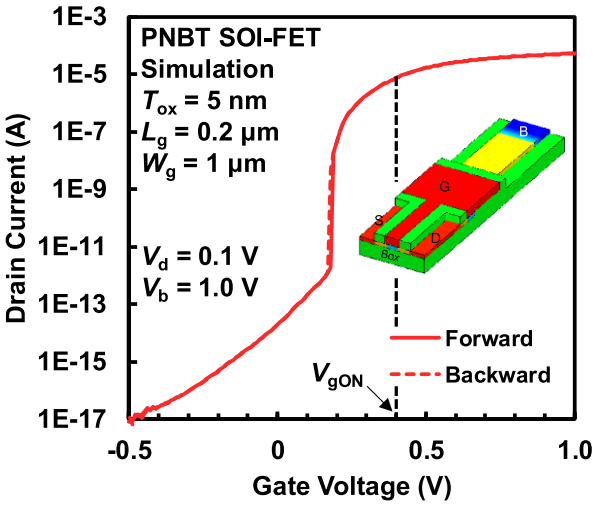


Fig. 6 Simulated I_d–V_g characteristics of the PNBT SOI-FET. Solid line: forward scan; dotted line: backward scan.

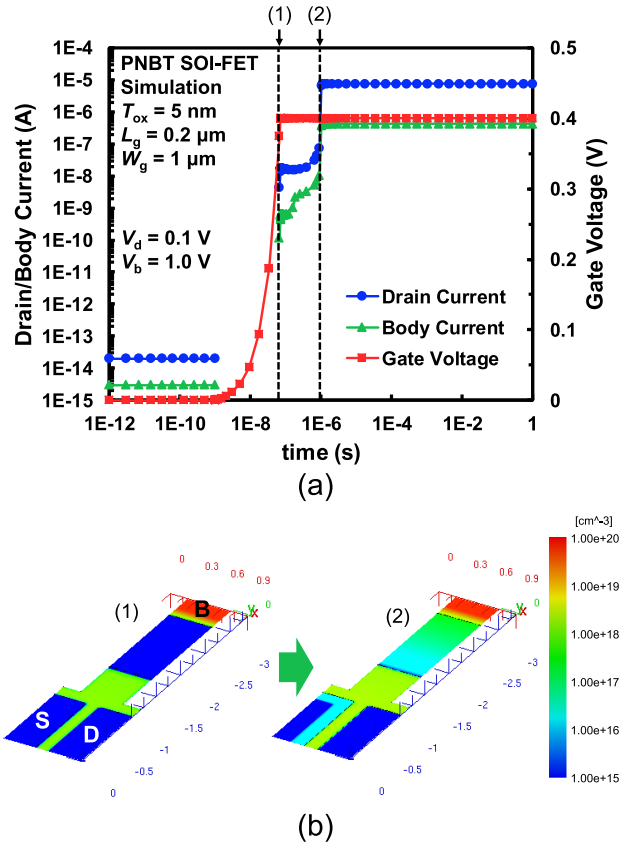


Fig. 7 Simulated transient (a) I_d and I_b characteristics, and (b) hole concentration at center of SOI when V_g = 0–0.4 V at turn-on.

no such leakage current, although the current level is below the WGFMU specifications.

Second, we simulate the transient characteristics of the PNBT SOI-FET for a more detailed analysis. The discussion of this simulation is based on a prior study conducted by us [11]. Figure 6 shows the simulated I_d–V_g characteristics of the PNBT SOI-FET. The simulated device structure is also shown in Fig. 6; it can be seen that the simulation can reproduce the super-steep SS DC characteristics. T_{ox} is set to 5 nm, which is a different value than in the actual structure. Figure 7 shows the transient I_d and I_b characteristics and the hole concentration at the center of the SOI when V_g = 0–0.4 V on turn-on. An I_d of less than 0.1 μA flows just after V_g = 0.4 V, after which the mode of the I_d flow shifts to 10 μA. Essentially, the device switches via a two-step change. There is an abrupt increase in the number of holes in the body (channel) region and the base (n-region) during the second step, as shown in Fig. 7 (b)-(2). The two-step change is explained as follows. First, a conventional subthreshold current flows between the source and the drain immediately after the on-state is reached. Next, the electrons diffuse from the source to the base (n-region), and this induces positive feedback (as in a thyristor), which results in the floating-body effect and a large current. The current in the second step of the simulation corresponds to the delay time in the measured data, as shown in Fig. 5 (b). The holes are provided from the body terminal, and they diffuse to the body (channel) region. However, because this is affected by the recombination at the base (n-region), time is taken for the arrival of the holes in the channel region, and the distance between the body terminal and the body (channel) region affects the delay time. We assume that the hole arrival time is the origin of the delay time.

Figure 8 shows the transient I_d and I_b characteristics, and the hole concentration when V_g = 0.4–0 V on turn-off. I_d and I_b decrease immediately after V_g = 0 V and exhibit a long-term leakage current, which was also observed in the measurements. It requires 1 s for the device to reach the off-state (I_d < 0.1 pA). The holes in the base (n-region) decrease at the point V_g = 0 V, as shown in Fig. 8 (b). However, some holes still accumulate in the body (channel) region. Figure 8 (c) shows the hole concentration at the front of the device. The remaining holes in the body (channel) region eject to the source; however, the ejection speed is slow. The potential of the body (channel) region decreases when some of the holes in the body (channel) region are discharged to the source as the forward current of the p-n junction. The lowering of the potential decreases the forward current of the p-n junction and slows the ejection of the remaining holes. It is known that the potential in the body (channel) region decreases logarithmically because of the above effect [28]. This effect also occurs in conventional partially depleted SOI-MOSFETs, and it induces the history effect and pass-gate leakage [29]. In Fig. 5 (b), we assume that the floating-body SOI-FET operating at V_d = 0.1 V does not show the floating-body effect because the hole injection quantity is not adequate to modulate the body (channel) region potential. This is considered to be the reason for the lack of long-term leakage current in our floating-body SOI-FET. However, the PNBT SOI-FET shows the floating-body effect because the body (channel) region potential is modulated by sufficient hole injection from the body terminal, and thus, it shows long-term leakage current.

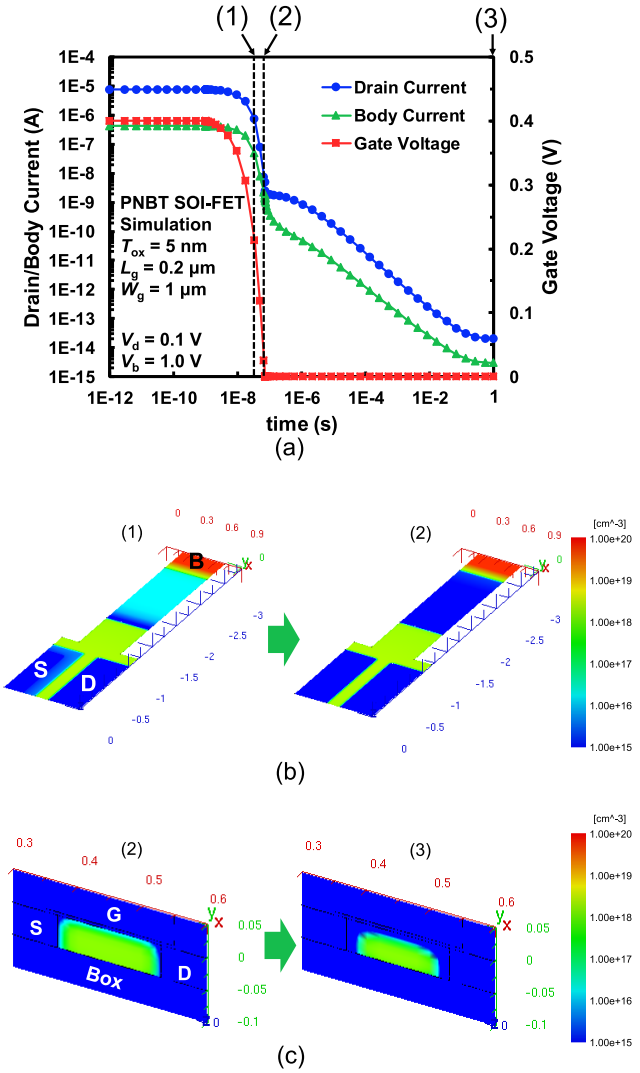


Fig. 8 Simulated transient (a) I_d and I_b characteristics, hole concentration at (b) center of SOI, and (c) front when V_g = 0.4–0 V on turn-off.

Third, we investigate the dependence on the applied voltages for fast operation of the PNBT SOI-FET. Figure 9 shows the measured turn-on waveform of the PNBT SOI-FET dependence on the turn-on V_g (V_{gON} shown in Fig. 2). The V_{gON} dependence, with three V_d and V_b conditions, is shown in Fig. 9 (a)–9 (c). In all conditions, the turn-on delay time decreases when V_{gON} increases. It is considered that fast band modulation occurs in the base (n-region) because many electrons are injected from the source, and this also induces rapid positive feedback. Figure 9 (d) summarizes the turn-on delay time vs. V_{gON} with three V_d and V_b conditions. It was found that a near-zero delay is obtained on the PNBT SOI-FET when the V_{gON} is set as the overdrive of 0.1–0.15 V from the trigger V_g producing the super-steep SS. This has positive implications for the low-speed concerns of the PNBT SOI-FET. Figures 10 and 11 show the I_d–V_g characteristics, and a summary of the turn-on delay time dependence on V_d and V_b of the PNBT SOI-FET. The results of two V_{gON} values are shown. The trigger V_g does not vary

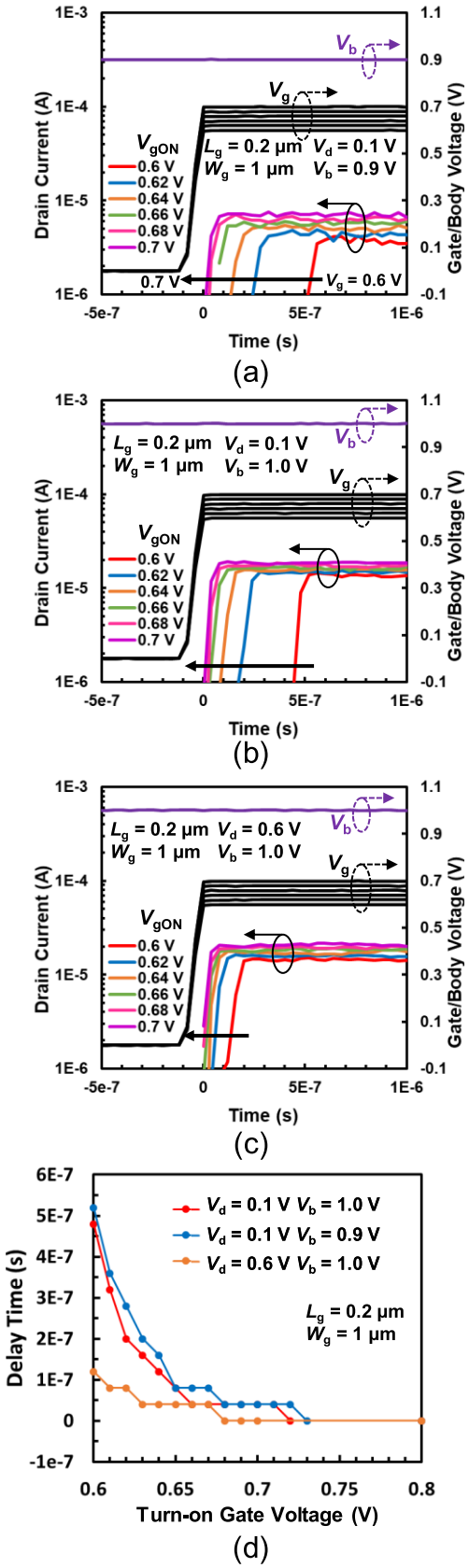


Fig. 9 Turn-on delay time dependence on V_{gON} with various V_d and V_b values. (a) V_d = 0.1 V, V_b = 0.9 V; (b) V_d = 0.1 V, V_b = 1.0 V; (c) V_d = 0.6 V, V_b = 1.0 V; (d) summary of (a)–(c).

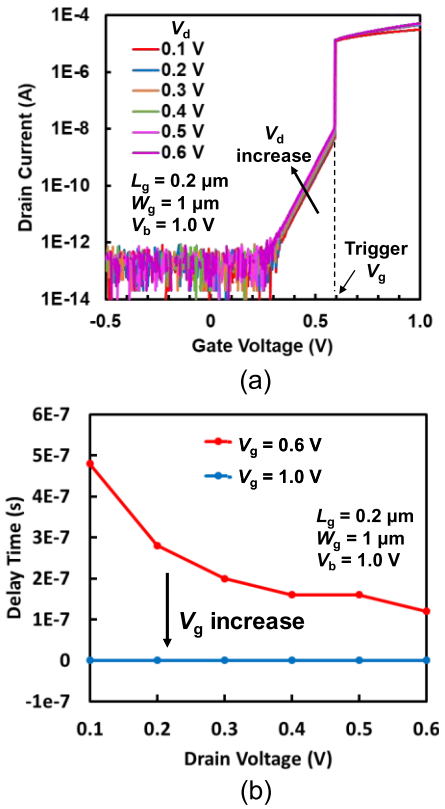


Fig. 10 (a) I_d–V_g characteristics, and (b) turn-on delay time dependence on V_d.

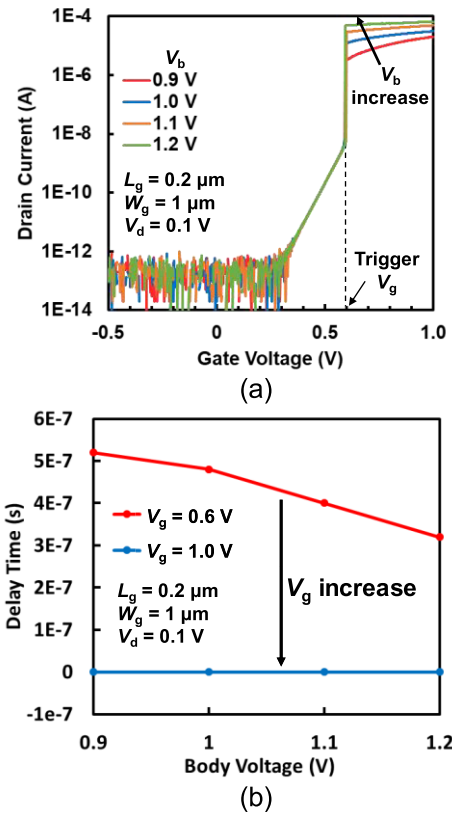


Fig. 11 (a) I_d–V_g characteristics, and (b) turn-on delay time dependence on V_b.

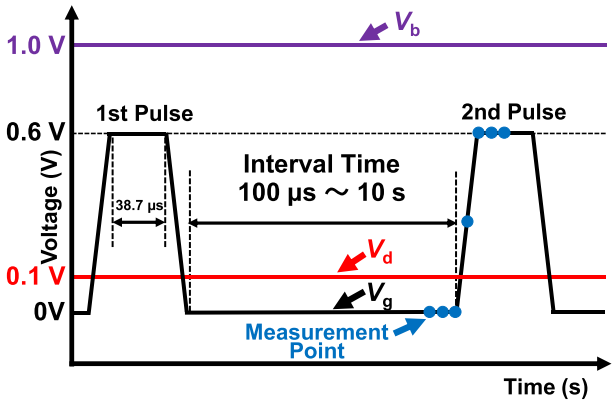


Fig. 12 Waveform of double pulse measurement.

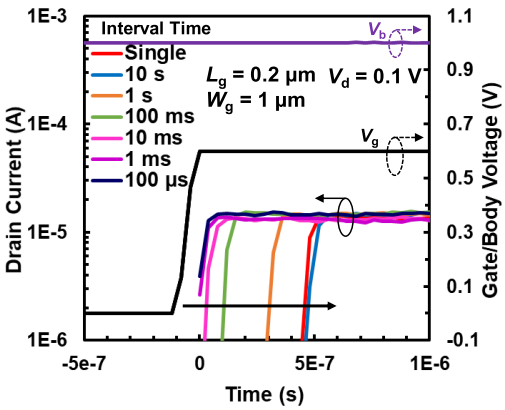


Fig. 13 Delay time on the second pulse. (a) Measured waveform of interval time dependence of second pulse turn-on delay, (b) summary of delay time on the second pulse vs. interval time.

according to V_d and V_b as shown in the DC characteristics, and the delay time decreases when V_d and V_b increase. It was also found that when V_g is set to approximately the trigger V_g value, the delay time does not decrease to nearly zero. V_d modulates the depletion width of the drain-side p-n junction. Therefore, the volume of the neutral-body (channel) region also modulates. Additionally, V_b affects the quantity of injection holes, and thus, the delay time decreases.

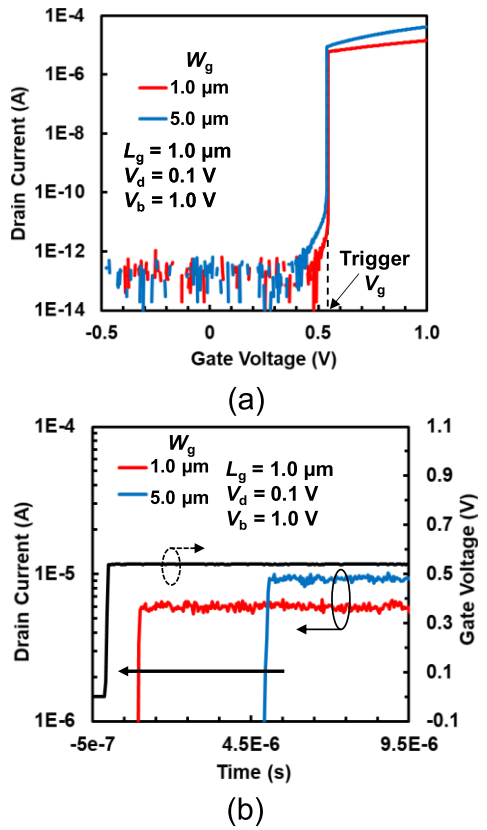


Fig. 14 Turn-on delay time dependence on W_g. (a) I_d–V_g characteristics, (b) turn-on characteristics.

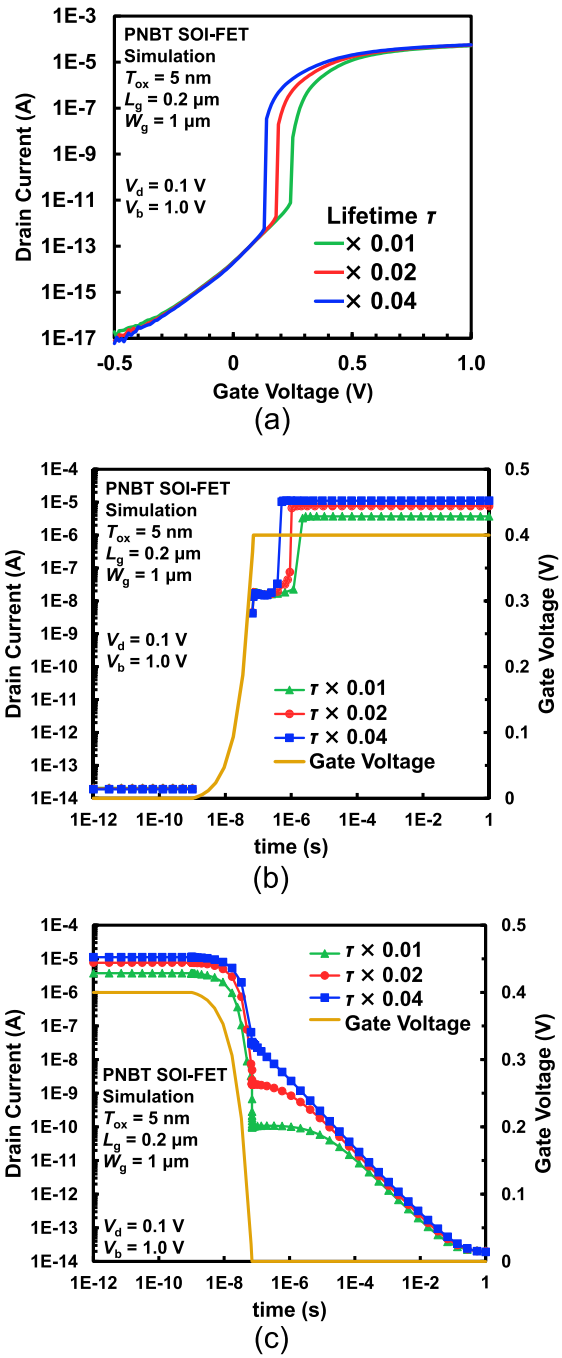


Fig. 15 SRH carrier lifetime dependence. (a) I_d–V_g characteristics, (b) turn-on, and (c) turn-off characteristics.

However, the delay time is nearly zero on all V_d and V_b when V_g = 1.0 V. Therefore, V_g has the most significant effect on the operating speed.

We measured the turn-on delay time of I_d on the second pulse, as shown in Fig. 12, to check the effect of the charged carrier at the first pulse. The V_g was set to be the trigger V_g of the super-steep SS, and the interval time between the first and second pulses was changed. Figure 13 shows the measured turn-on waveform of the PNBT SOI-FET dependence on the interval time, and a summary of the delay time on the second pulse vs. the interval time. It was found that, when the interval time increases to 10 s, the delay time on the second pulse increases to equal the single pulse delay time. These data clearly indicate that the charging carriers from the first pulse remain in the body (channel) region. The turn-on delay time of the second pulse decreases to nearly zero when the interval time between the pulses is below 10 ms, even if the gate voltage value is around the trigger V_g. This is because the remaining carriers assist the turn-on at the second pulse. This is a concern in circuit design; however, these characteristics may also be utilized for memory applications [23], [24], [26].

Finally, we investigate the impact of device size and carrier lifetime on high-speed operation. Figure 14 shows the measured W_g dependence of the PNBT SOI-FET characteristics. When V_g > trigger V_g, I_d is not proportional to W_g. Additionally, the increase rate of I_d is different between W_g = 1 μm and W_g = 5 μm, as shown in Fig. 14 (a). We consider that these are induced by the difference in the strength of the feedback. W_g affects the strength of the feedback because the PNBT structure is asymmetry in the body terminal direction. In this case, the elongated W_g weakens the feedback. Furthermore, the strong feedback induces the parasitic bipolar effect (PBE), similar to a conventional floating-body SOI-FET, and then the I_d flows within the entire SOI. In our previous study, we have reported the PBE and confirmed the I_d enhancement effect [30]. V_g controls

the surface potential only and therefore, the I_d controllability decreases when the I_d flows through the entire SOI. This leads to the following results. (1) In terms of the W_g ratio, the I_d at $W_g = 5\ \mu$m is smaller than I_d at $W_g = 1\ \mu$m owing to the weak feedback. (2) The operation mode at $W_g = 5\ \mu$m does not change to the flowing entire SOI mode. Therefore, the increase rate of I_d is different due to the difference in the gate controllability. The delay time of the PNBT SOI-FET is reduced with a narrow W_g as shown in Fig. 14 (b). The charged carrier is expected to be small when the $L_g \times W_g$ dimensions are small; this result suggests that carrier charging in the body (channel) region also plays a key role. Figure 15 shows the simulated carrier lifetime dependence of the PNBT SOI-FET characteristics. The carrier lifetime affects the carrier injection efficiency from the body terminal to the body (channel) region. The trigger voltage shifts in the negative direction in the long carrier lifetime condition, because it is prone to strong positive feedback for high carrier injection efficiency [16]. It improves the turn-on delay, as shown in Fig. 15 (b); however, as shown in Fig. 15 (c), it also deteriorates the turn-off leakage current. These characteristics show a trade-off relationship. This method needs improvement; however, the turn-off leakage current problem has the possibility of being mitigated in the short carrier lifetime condition. We can control the carrier lifetime using ion implantations, such as with Ar [31] or Ge [32].

4. Conclusion

We investigated the transient characteristics on the super-steep SS PNBT SOI-FET using TCAD simulation and pulse measurements. The turn-on delay, the turn-off leakage current, and the carrier charging effect were observed. Those characteristics come from the turn-on speed of the inherent thyristor and the floating-body effect. It was found that the turn-on delay time decreased to near zero when the gate overdrive was set to 0.1–0.15 V and/or the interval between pulses was set to below 10 ms. This is good news for the low speed concern of the PNBT SOI-FET. Additionally, W_g scaling also reduced the turn-on delay time. However, the leakage current on turn-off is still a critical issue for ultralow power operation. We consider that a greater number of optimized device parameters are needed to realize both a high on/off ratio and high-speed operation.

Acknowledgments

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References

[1] Acatech. (2013, April) Recommendations for implementing the strategic initiative INDUSTRIE 4.0. [Online]. Available: https://www.acatech.de/wp-content/uploads/2018/03/Final_report_Industrie_4.0_accessible.pdf

[2] Society 5.0. [Online]. Available: https://www.gov-online.go.jp/cam/s5/eng/

[3] A.M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," Nature, vol.479, pp.329–337, Nov. 2011. doi: 10.1038/nature10679.

[4] T. Mori, H. Asai, J. Hattori, K. Fukuda, S. Otsuka, Y. Morita, S. O'uchi, H. Fuketa, S. Migita, W. Mizubayashi, H. Ota, and T. Matsukawa, "Demonstrating performance improvement of complementary TFET circuits by Ion enhancement based on isoelectronic trap technology," 2016 IEEE Int. Electron Devices Meet., San Francisco, CA, pp.19.4.1–19.4.4, 2016. doi: 10.1109/IEDM.2016.7838453.

[5] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low-power nanoscale devices," Nano Lett., vol.8, no.2, pp.405–410, Dec. 2007. doi: 10.1021/nl071804g.

[6] K.-S. Li, Y.-J. Wei, Y.-J. Chen, W.-C. Chiu, H.-C. Chen, M.-H. Lee, Y.-F. Chiu, F.-K. Hsueh, B.-W. Wu, P.-G. Chen, T.-Y. Lai, C.-C. Chen, J.-M. Shieh, W.-K. Yeh, S. Salahuddin, and C. Hu, "Negative-capacitance FinFET inverter, ring oscillator, SRAM cell, and ft," IEEE Int. Electron Devices Meet., San Francisco, CA, pp.31.7.1–31.7.4, 2018. doi: 10.1109/IEDM.2018.8614521.

[7] J. Ida, T. Mori, Y. Kuramoto, T. Horii, T. Yoshida, K. Takeda, H. Kasai, M. Okihara, and Y. Arai, "Super steep subthreshold slope PN-body tied SOI FET with ultra low drain voltage down to 0.1V," 2015 IEEE Int. Electron Devices Meet., Washington, DC, pp.22.7.1–22.7.4, 2015. doi: 10.1109/IEDM.2015.7409761.

[8] T. Mori and J. Ida, "P-Channel and N-Channel Super-Steep Subthreshold Slope PN-Body Tied SOI-FET for Ultralow Power CMOS," IEEE J. Electron Devices Soc., vol.6, pp.1213–1219, Oct. 2018. doi: 10.1109/JEDS.2018.2876432.

[9] T. Mori, J. Ida, S. Momose, K. Itoh, K. Ishibashi, and Y. Arai, "Diode characteristics of a super-steep subthreshold slope PN-body tied SOI-FET for energy harvesting applications," IEEE J. Electron Devices Soc., vol.6, pp.565–570, April 2018. doi: 10.1109/JEDS.2018.2824344.

[10] H. Endo, J. Ida, T. Mori, K. Ishibashi, and Y. Arai, "First Experimental Confirmation of Transient Effect on Super Steep SS "PN-Body Tied SOI FET" with Pulse Measurements," 2019 Electron Devices Technology and Manufacturing Conference (EDTM), Singapore, Singapore, pp.91–93, 2019. doi: 10.1109/EDTM.2019.8731082

[11] T. Mori, J. Ida, and H. Endo, "Analysis of transient effect on super-steep SS PN-body tied SOI-FET," 2019 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, pp.1–2, 2019. doi: 10.1109/VLSI-TSA.2019.8804639.

[12] Keysight B1500A Semiconductor Device Analyzer data sheet. [Online]. Available: http://literature.cdn.keysight.com/litweb/pdf/5989-2785EN.pdf

[13] N. Kotani, "TCAD in Selete," Proc. Int. Conf. SISPAD, pp.3–7, 1998. doi: 10.1007/978-3-7091-6827-1_2

[14] T. Wada, M. Fujinaga, Y. Okura, H. Ishikawa, S. Ito, T. Uchida, T. Enda, S. Otsuka, H. Komatsubara, and T. Shinzawa, "ENEXSS a 3-dimensional TCAD system," Ext. Abstr. (LIII Spring Meet. 2006), Japan Society of Applied Physics, 22p-ZA-2, 2006 (in Japanese).

[15] M. Nakamura, "Current status and subjects on practical 3D TCAD for next generation," Jpn. Soc. Appl. Phys., vol.77, no.7, pp.818–822, 2008 (in Japanese).

[16] T. Mori and J. Ida, "Analysis and optimization of device parameters on super-steep subthreshold slope PN-body tied SOI-FET," Proc. International Conference on Solid State Devices and Materials (SSDM), pp.839–840, Sept. 2018.

[17] C.-E.D. Chen, M. Matloubian, R. Sundaresan, B.-Y. Mao, C.C. Wei, and G.P. Pollack, "Single-transistor latch in SOI MOSFETs," IEEE Electron Device Lett., vol.9, no.12, pp.636–638, Dec. 1988. doi: 10.1109/55.20420.
[18] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, J.G. Fossum, L. Altimime, and M. Jurczak, "Realizing super-steep subthreshold slope with conventional FDSOI CMOS at low-bias voltages," IEDM Tech. Dig., pp.16.6.1–16.6.3, Dec. 2010. doi: 10.1109/IEDM.2010.5703377.
[19] D. Ueda, K. Takeuchi, M. Kobayashi, and T. Hiramoto, "Optimizing MOS-gated thyristor using voltage-based equivalent circuit model for designing steep-subthreshold-slope PN-body-tied silicon-on-insulator FET," Jpn. J. Appl. Phys., vol.57, no.4S, pp.04FD06-1–04FD06-6, March 2018. doi: 10.7567/JJAP.57.04FD06.
[20] A. Padilla, C.W. Yeung, C. Shin, C. Hu, and T.-J.K. Liu, "Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages," IEDM Tech. Dig., pp.171–174, Dec. 2008. doi: 10.1109/IEDM.2008.4796643.
[21] M. Kim, Y. Kim, D. Lim, S. Woo, K. Cho, and S. Kim, "Steep switching characteristics of single-gated feedback field-effect transistors," Nanotechnology, vol.28, no.5, pp.1–8, Dec. 2016. doi:10.1088/1361-6528/28/5/055205.
[22] C. Lee, E. Ko, and C. Shin, "Steep slope silicon-on-insulator feedback field-effect transistor: design and performance analysis," IEEE Trans. Electron Devices, vol.66, no.1, pp.286–291, Jan. 2019. doi: 10.1109/TED.2018.2879653.
[23] J. Cho, D. Lim, S. Woo, K. Cho, and S. Kim, "Static random access memory characteristics of single-gated feedback field-effect transistors," IEEE Trans. Electron Devices, vol.66, no.1, pp.413–419, Jan. 2019. doi: 10.1109/TED.2018.2881965.
[24] J. Wan, C.L. Royer, A. Zaslavsky, and S. Cristoloveanu, "A systematic study of the sharp-switching Z^2-FET device: from mechanism to modeling and compact memory applications," Solid State Electron., vol.90, pp.2–11, Dec. 2013. doi: 10.1016/j.sse.2013.02.060.
[25] Y. Taur, J. Lacord, M.S. Parihar, J. Wan, S. Martinie, K. Lee, M. Bawedin, J.-C. Barbe, and S. Cristoloveanu, "A comprehensive model on field-effect pnpn devices (Z^2-FET)," Solid State Electron., vol.134, pp.1–8, Aug. 2017. doi: 10.1016/j.sse.2017.05.004.
[26] C. Navarro, J. Lacord, M.S. Parihar, F. A.-Lema, M. Duan, N. Rodriguez, B. Cheng, H.E. Dirani, J.-C. Barbe, P. Fonteneau, M. Bawedin, C. Millar, P. Galy, C.L. Royer, S. Karg, P. Wells, Y.-T. Kim, A. Asenov, S. Cristoloveanu, and F. Gamiz, "Extended Analysis of the Z^2-FET: Operation as Capacitorless eDRAM," IEEE Trans. Electron Devices, vol.64, no.11, pp.4486–4491, Nov. 2017. doi: 10.1109/TED.2017.2751141.
[27] K. Deguchi, K. Miyoshi, H. Ban, T. Matsuda, T. Ohno, and Y. Kado, "Fabrication of 0.2 μm large scale integrated circuits using synchrotron radiation x-ray lithography," J. Vac. Sci. Technol. B, vol.13, no.6, pp.3040–3045, Nov./Dec. 1995. doi: 10.1116/1.588318.
[28] M. Terauchi and M. Yoshimi, "Analysis of floating-body-induced leakage current in 0.15 μm SOI DRAM," 1996 IEEE Int. SOI Conf. Proc., Sanibel Island, FL, pp.138–139, 1996. doi: 10.1109/SOI.1996.552532.
[29] G.G. Shahidi, A. Ajmera, F. Assaderaghi, R.J. Bolam, E. Leobandung, W. Rausch, D. Sankus, D. Schepis, L.F. Wagner, K. Wu, and B. Davari, "Partially-depleted SOI technology for digital logic," 1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition (Cat. No.99CH36278), San Francisco, CA, pp.426–427, 1999. doi: 10.1109/ISSCC.1999.759337.
[30] T. Mori, J. Ida, W. Yabuki, S. Nakano, H. Endo, and Y. Arai, "Drain current enhancement effect on super-steep subthreshold slope "PN-Body Tied SOI-FET"," 2018 IEEE Silicon Nanoelectronics Workshop (SNW), Honolulu, HI, pp.71–72, 2018.
[31] T. Ohno, M. Takahashi, Y. Kado, and T. Tsuchiya, "Suppression of parasitic bipolar action in ultra-thin-film fully-depleted CMOS/SIMOX devices by Ar-ion implantation into source/drain regions," IEEE Trans. Electron Devices, vol.45, no.5, pp.1071–1076, May 1998. doi: 10.1109/16.669534.
[32] K.R. Mistry, J.W. Sleight, G. Grula, R. Flatley, B. Miner, L.A. Bair, and D.A. Antoniadis, "Parasitic bipolar gain reduction and the optimization of 0.25-/spl mu/m partially depleted SOI MOSFETs," IEEE Trans. Electron Devices, vol.46, no.11, pp.2201–2209, Nov. 1999. doi: 10.1109/16.796297.

Appendix:

In this appendix, we show the details of the parameter in the HyENEXSS's SRH model.

The generation/recombination rate U_{SRH} is calculated using the following Eq. (A· 1):

$$U_{\mathrm{SRH}} = \frac{n_i^2 - pn}{\tau_{\mathrm{p}}(n + n_i) + \tau_{\mathrm{n}}(p + n_i)} \tag{A· 1}$$

where τ is the carrier lifetime, n_i is the intrinsic carrier density, n is the electron concentration, and p is the hole concentration. τ is also calculated using the following Eq. (A· 2).

$$\tau_{\mathrm{n,p}} = A_{\mathrm{n,p}}\left(\tau_{\mathrm{min}}^{\mathrm{n,p}} + \frac{\tau_{\mathrm{max}}^{\mathrm{n,p}} - \tau_{\mathrm{min}}^{\mathrm{n,p}}}{1 + (N/N_{\mathrm{t}}^{\mathrm{n,p}})^{B_{\mathrm{n,p}}}}\right) \tag{A· 2}$$

The model parameters are shown in Table A· 1. In this study, we controlled the carrier lifetime by changing the values of A.

Table A· 1 Model parameters in HyENEXSS's SRH model.

parameter	Electron (n)	Hole (p)
τ_{max}	1.137×10^{-6} s	3.707×10^{-7} s
τ_{min}	3.0×10^{-7} s	1.0×10^{-7} s
N_{t}	2.5×10^{15} cm^{-3}	
A	0.01, 0.02, 0.04	
B	0.5	



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