A Sub-1-µs Start-Up Time, Fully-Integrated 32-MHz Relaxation Oscillator for Low-Power Intermittent Systems

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PAPER

A Sub-1-μs Start-Up Time, Fully-Integrated 32-MHz Relaxation Oscillator for Low-Power Intermittent Systems

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SUMMARY This paper presents a fully integrated 32-MHz relaxation oscillator (ROSC) capable of sub-1-μs start-up time operation for low-power intermittent VLSI systems. The proposed ROSC employs current mode architecture that is different from conventional voltage mode architecture. This enables compact and fast switching speed to be achieved. By designing transistor sizes equally between one in a bias circuit and another in a voltage to current converter, the effect of process variation can be minimized. A prototype chip in a 0.18-μm CMOS demonstrated that the ROSC generates a stable clock frequency of 32.6 MHz within 1-μs start-up time. Measured line regulation and temperature coefficient were ±0.69% and ±0.38%, respectively.

key words: *relaxation oscillator, fast start-up, digital signal processing, high accuracy, intermittent operation, PVT variations*

1. Introduction

Intermittent operation mode of VLSI systems is a promising method to achieve low-power dissipation of next-generation IoT (Internet of Things) devices [1]–[4]. To realize the intermittent operation, there are two general ways: 1) cut off bias signals (bias voltages or currents) and 2) cut off the supply voltage. Although the former can stop the circuit operation easily, the leakage current of the circuit cannot be cut off and the bias generator dissipates considerable power. The latter can reduce the power dissipation significantly. However, when the circuit is activated again, it needs a certain time before it operates correctly. For example, a clock source is an indispensable building block for analog and digital signal processing. However, conventional clock sources, or crystal oscillators (XOs) [5], dissipate a significant wasting power because they need a long start-up time (e.g., longer than several hundreds of μs). This leads to a longer active time and it dissipates large unnecessary power, or energy overhead (Eoh).

Several studies aiming to replace an external-XO with an on-chip oscillator have been investigated [6]–[14]. Relaxation oscillators (ROSC) have attracted considerable attention because they can be developed with fully on-chip configuration and achieve a fast start-up operation compared with conventional XOs. The conventional ROSCs employ additional circuits to compensate for non-ideal delays, which are caused by comparators and control logic circuits, and achieve high clock frequency with fully on-chip configuration [13], [14]. However, they still need a long start-up time (e.g., several tens of μs), because the compensation circuits need a long settling time, even though they do not include the start-up time of the bias current or bias voltage for the circuit. Thus, we have to develop an ROSC capable of fast start-up operation for intermittent systems with fully on-chip configuration.

In light of this background, we here present a fully on-chip ROSC capable of fast start-up operation with high accuracy for intermittent systems. We develop a current mode ROSC architecture that is different from a conventional voltage mode architecture. By using the current mode ROSC, we can develop the ROSC without an additional compensation circuit. This enables compact and fast switching speed to be achieved. In our proposed ROSC, the start-up time is determined by that of a reference circuit, which is usually less than 1 μs. In contrast to our previous works [15], [16], we discuss the circuit operation and effectiveness in more detail in this paper.

This paper is organized as follows: Sect. 2 briefly summarizes the operation of the conventional ROSC and describes the operation principle of our proposed ROSC. Sect. 3 shows simulated and measured results with a prototype chip we made using a 0.18-μm standard CMOS process technology. Sect. 4 concludes the paper.

2. ROSC

2.1 Conventional ROSC Architecture

Figure 1 (a) shows a conventional voltage mode ROSC. The circuit consists of a reference voltage V_{REF}, bias currents I_{B}s, voltage mode comparators (VMC) Comp.1,2, capacitors $C_{\mathrm{RAMP1,2}}$, reset switches $\mathrm{MN}_{\mathrm{RST1,2}}$, and a control logic circuit. When Q and Q_{B} are high and low, $\mathrm{MN}_{\mathrm{RST1}}$ and $\mathrm{MN}_{\mathrm{RST2}}$ are off and on, respectively. The C_{RAMP1} accepts I_{B} and generates a ramp voltage of V_{INT1}. The Comp.1 compares V_{INT1} with V_{REF}. When the V_{INT1} reaches V_{REF}, the Comp.1 detects it and Q and Q_{B} toggle low and high, respectively. By repeating above operation alternately for C_{RAMP1} and C_{RAMP2}, the circuit generates a clock pulse. The clock frequency f_{CLK} can be expressed as

$$f_{\mathrm{CLK}} = \frac{I_{\mathrm{B}}}{2C_{\mathrm{RAMP1,2}}V_{\mathrm{REF}}}. \quad (1)$$

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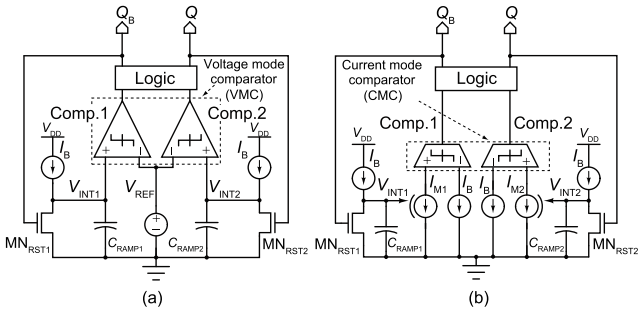

Fig. 1 Schematics of (a) conventional voltage mode and (b) our proposed current mode ROSC.

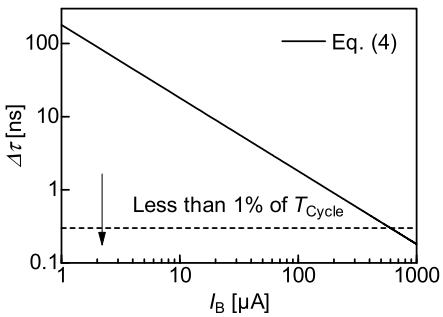

Fig. 2 Calculated delay as function of the bias current.

Therefore we can obtain the clock frequency f_{CLK} by setting parameters such as the V_{REF}, I_B, and $C_{RAMP1,2}$.

However, the clock frequency, or the clock period, changes due to the comparator's non-idealities such as offset voltage ΔV_{offset} and finite delay time $\Delta\tau$ of the comparator and digital circuits. Therefore, it is difficult to obtain a stable clock frequency when we consider the effect of PVT (process, voltage, and temperature) variations. Thus, Eq. (1) is rewritten as

$$f_{CLK} = \frac{I_B}{2\left\{C_{RAMP1,2}(V_{REF} + \Delta V_{offset}) + I_B \cdot \Delta\tau\right\}}. \quad (2)$$

The ΔV_{offset} is proportional to a threshold voltage mismatch between transistors. The voltage can be expressed as

$$\sigma(\Delta V_{TH}) = \frac{A_{V_{TH}}}{\sqrt{WL}}, \quad (3)$$

where $A_{V_{TH}}$ is the process dependence parameter, W is the channel width, and L is the channel length [17]. Therefore, the ΔV_{offset} can be reduced by using large W and L. On the other hand, simplified $\Delta\tau$ can be given by

$$\Delta\tau = \frac{C_L \Delta V}{I_B}, \quad (4)$$

where C_L is the load capacitor and ΔV is the output voltage swing of the comparator. Figure 2 shows the calculated results of $\Delta\tau$ (Eq. (4)) as a function of I_B. C_L and ΔV were set to 100 fF and 1.8 V, respectively. The delay is inversely proportional to the bias current I_B. When we consider to generate a 32-MHz clock frequency and suppress the effect of the delay within 1%, $\Delta\tau$ must be less than 0.3 ns. However, I_B needs more than 600 μA as shown in Fig. 2. Therefore, the conventional ROSC dissipates high power to achieve high accuracy of the frequency.

To solve this problem, several studies employing compensation circuits have been reported to obtain a robust and stable clock frequency [6]–[9]. However, they require additional circuits to compensate for the variation and need a long settling time to use, and increase power dissipation. Therefore, it is difficult to achieve a fast start-up time without increasing power.

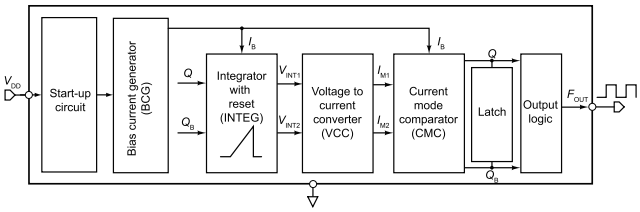

Fig. 3 Block diagram of our proposed ROSC.

2.2 Proposed ROSC Architecture

To achieve a fast start-up time of an ROSC, we consider modifying the architecture. Figure 1 (b) shows a schematic of our proposed ROSC. The circuit is similar to the conventional ROSC, but is different in employing current mode comparator (CMC) instead of the VMC. Because the CMC is able to operate faster than the VMC [18], the effect of the comparator's non-idealities can be minimized. By employing the CMC, we can eliminate the compensation circuit, and thus we can achieve a fast start-up operation. The start-up time of the proposed ROSC is determined by that of the bias circuit, which is usually less than 1 μs.

Figure 3 shows a simplified block diagram of our proposed ROSC. The circuit consists of a start-up circuit, bias current generator (BCG), integrators with reset (INTEG), voltage to current converter (VCC), current mode comparator (CMC), and output logic circuit. The BCG generates a bias current of I_B and the current is applied to the INTEG and CMC. The INTEG generates ramp voltages of V_{INT1} and V_{INT2} and the voltages are converted to currents of I_{M1} and I_{M2} by the VCC. The CMC accepts the generated currents and compares them with I_B. When the I_{M1} (or I_{M2}) reaches I_B, the latch toggles the internal logic and generates a clock pulse.

2.3 Circuit Design

Figure 4 shows the entire circuit configuration of our ROSC. We use the threshold voltage (V_{TH}) referenced current reference circuit as the BCG [19]. Resistors used in the BCG are made of a diffused resistor R_P and a high-resistive polysilicon resistor R_N that has opposite temperature coefficient with R_P. The bias current I_B is expressed as

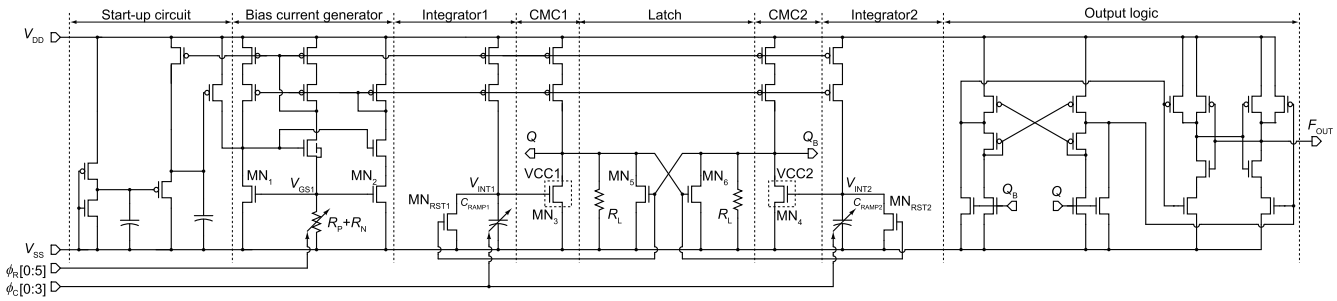

Fig. 4 Entire circuit configuration of our proposed ROSC.

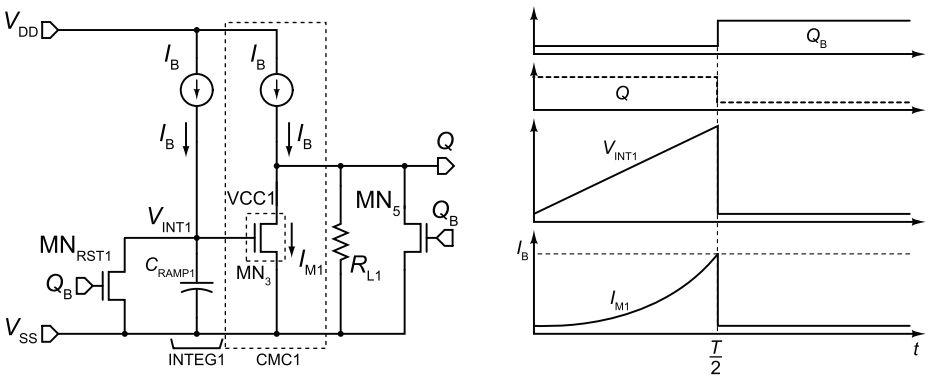

Fig. 5 Schematic and timing diagram of the INTEG1, VCC1, and CMC1.

$$I_B = \frac{V_{GS,MN1}}{R_P + R_N}. \tag{5}$$

Figure 5 shows an extracted schematic of the INTEG1, VCC1, and CMC1 and its timing diagram. When Q and Q_B are high and low, MN_{RST1} is off. The C_{RAMP1} accepts I_B and generates a ramp voltage of $V_{INT1} = (I_B \cdot t)/C_{RAMP1}$, where t is time. The V_{INT1} increases gradually and is monitored by a transistor MN_3 in the VCC1. The MN_3 generates a current of I_{M1} from V_{INT1}. The CMC1 compares I_{M1} with I_B. When the I_{M1} reaches I_B, the subsequent latch detects it and Q and Q_B toggle to low and high, respectively (see Fig. 4). The output logic accepts the voltages of Q and Q_B and converts them into full-swing output voltages. By repeating the operation, the ROSC generates a clock pulse.

The operation discussed above is performed in half of the clock period T_{cycle}. Thus, the V_{INT1} can be expressed as $(I_B \cdot T_{cycle}/2)/C_{RAMP1}$ when Q and Q_B toggle. Because V_{INT1} is equal to $V_{GS,MN3}$, we obtain the following equation;

$$V_{GS,MN3} = \frac{I_B \cdot T_{cycle}}{2C_{RAMP1}}. \tag{6}$$

Therefore, from Eqs. (5) and (6), the clock period T_{cycle} is given by

$$T_{cycle} = 2(R_P + R_N)C_{RAMP1}\frac{V_{GS,MN3}}{V_{GS,MN1}}. \tag{7}$$

Note that, using the same transistor sizes between MN_1 in the BCG and MN_3 (and MN_4) in the VCC, the gate-source voltages are canceled and the effect of process variation can be minimized (i.e., $T_{cycle} = 2(R_P + R_N)C_{RAMP}$). The oscillation frequency can be expressed as

$$f_{CLK} = \frac{1}{T_{cycle}} = \frac{1}{\{2(R_P + R_N)C_{RAMP}\}}. \tag{8}$$

2.4 Transition Delay of the CMC

As discussed above, our proposed ROSC achieves a fast start-up operation by eliminating compensation circuits. However, we have to also take into account the delay of the CMC itself. In order to fasten the transition delay of the CMC, we use clamping pull-down resistors R_{L1} and R_{L2} at nodes of Q and Q_B, respectively, as shown in Figs. 4 and 5. Without these resistors, Q or Q_B increases to V_{DD} when reset, due to the loss of the current path. This will cause a long transition delay and the oscillation frequency will be degraded.

From Eq. (8), the clock period T_{cycle} of the ROSC can be expressed as

$$T_{cycle} = 2\left((R_P + R_N)C_{RAMP} + \Delta\tau_{CMC} + \Delta\tau_{Latch}\right), \tag{9}$$

where $\Delta\tau_{CMC}$ and $\Delta\tau_{Latch}$ are the delays of the CMC and latch circuit, respectively. Because the $\Delta\tau_{Latch}$ is determined by the cross-coupled positive feedback circuit, the $\Delta\tau_{Latch}$ is shorter than the $\Delta\tau_{CMC}$ [19]. On the other hand, the $\Delta\tau_{CMC}$ depends on the clamping resistors because they determine the voltage levels of the Q and Q_B when reset. Thus, the larger R_L increases $\Delta\tau_{CMC}$. Therefore, we have to choose proper resistance of R_{L1} and R_{L2} to shorten $\Delta\tau_{CMC}$.

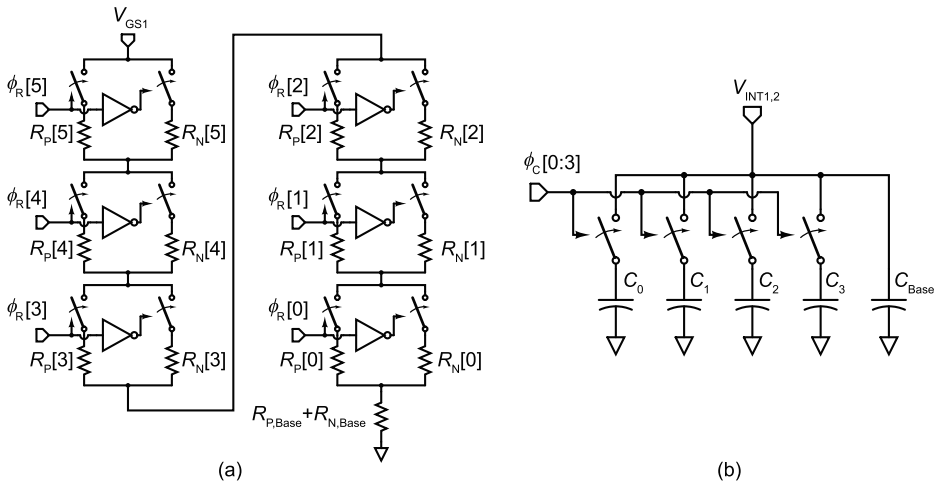

Fig. 6 Schematics of (a) RTC and (b) CTC.

2.5 Temperature Dependence

As shown in Eq. (8), because temperature dependence of C_{RAMP} is sufficiently small, temperature dependence of the clock frequency f_{CLK} is determined by the total resistance of $(R_{\mathrm{P}} + R_{\mathrm{N}})$. The temperature dependence of the resistors R_{P} and R_{N} are given by

$$\begin{aligned} R_{\mathrm{P}} &= R_{\mathrm{P}}(T_0) \cdot (1 + \alpha_{\mathrm{P}}(T - T_0)), \\ R_{\mathrm{N}} &= R_{\mathrm{N}}(T_0) \cdot (1 - \alpha_{\mathrm{N}}(T - T_0)), \end{aligned} \tag{10}$$

where $R_{\mathrm{P}}(T_0)$ and $R_{\mathrm{N}}(T_0)$ are resistances at a temperature T_0, α_{P} and α_{N} are temperature coefficients of resistors, T is the absolute temperature [21]. Using Eqs. (8) and (10), we can expressed the temperature coefficient of the oscillation frequency as

$$\frac{1}{f_{\mathrm{CLK}}} \frac{df_{\mathrm{CLK}}}{dT} = -\frac{R_{\mathrm{P}}(T_0) \cdot \alpha_P - R_{\mathrm{N}}(T_0) \cdot \alpha_N}{R_{\mathrm{P}} + R_{\mathrm{N}}}. \tag{11}$$

Thus, the temperature dependence of the clock frequency f_{CLK} can be compensated by choosing proper combination of R_{P} and R_{N} (i.e., $R_{\mathrm{P}}(T_0) \cdot \alpha_P - R_{\mathrm{N}}(T_0) \cdot \alpha_N = 0$).

2.6 Trimming Circuits

As discussed in the previous section, the oscillation frequency f_{CLK} is determined by RC product (see Eq. (8)). Therefore, the f_{CLK} will change with process and temperature variations. The process dependence of the oscillation frequency f_{CLK} can be given by

$$\frac{\Delta f_{\mathrm{CLK}}}{f_{\mathrm{CLK}}} = -\frac{\Delta(R_{\mathrm{P}} + R_{\mathrm{N}})}{R_{\mathrm{P}} + R_{\mathrm{N}}} - \frac{\Delta C_{\mathrm{RAMP}}}{C_{\mathrm{RAMP}}}. \tag{12}$$

To compensate for the variations, we develop resistor and capacitor trimming circuits (RTC and CTC).

Figure 6 (a) shows a schematic of the RTC. The RTC consists of a base resistor of $R_{\mathrm{P,Base}}$+$R_{\mathrm{N,Base}}$, switches, inverters, and trimming resistors ($R_{\mathrm{P}}[i]$ and $R_{\mathrm{N}}[i]$ $(i = 0-5)$). Using the same resistance and different temperature dependent resistors $R_{\mathrm{P}}[i]$ and $R_{\mathrm{N}}[i]$, we can control the temperature dependence of the frequency without changing the value of RC product.

Figure 6 (b) shows a schematic of the CTC. The CTC consists of a base capacitor C_{Base}, switches, and trimming capacitors $(C_0 - C_3)$. Because the temperature dependence of the capacitor is sufficiently small, the oscillation frequency can be adjusted by the CTC. Note that, we use transmission gate switches in RTC and CTC.

3. Results

3.1 Simulation

To investigate the CMC performance, we evaluated the CMC by changing $R_{\mathrm{L1,2}}$ in a 0.18-μm standard CMOS process technology. Figure 7 shows the simulated delay as a function of $R_{\mathrm{L1,2}}$. As discussed in Sect. 2.4, the error of the clock period was almost linearly dependent on the $R_{\mathrm{L1,2}}$. From the results, we found that the error can be minimized when $R_{\mathrm{L1,2}}$ is set to 40.7 kΩ.

The proposed ROSC was designed and simulated in the same CMOS technology. Target oscillation frequency was set to 32 MHz. We evaluated the circuit performance by extracting parasitics from post-layout data. After the extraction, because the parasitic capacitance and resistance were added, we adjusted design parameters such as capacitance and resistance to obtain a 32-MHz clock frequency. The total resistance of R_{P}+R_{N} and $C_{\mathrm{RAMP1,2}}$ were set to 20.5 kΩ, and 546.1 fF, respectively, and $R_{\mathrm{L1,2}}$ was set to 43.7 kΩ in this design.

Figure 8 shows the simulated start-up waveform. V_{DD} was changed from 0 to 1.8 V with 1-ns rising speed. The ROSC starts to oscillate at 0.4 μs. Figure 9 shows the oscillation frequency as a function of time. The oscillation frequency settles to the steady state frequency of 32.1 MHz within 1 μs. The power dissipation was 325.8 μW. We confirmed a stable operation with fast start-up time. Figure 10 shows the simulated star-up energy overhead (Eoh), which

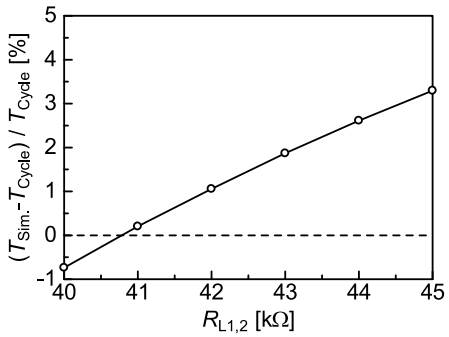

Fig. 7 Simulated delay of the CMC.

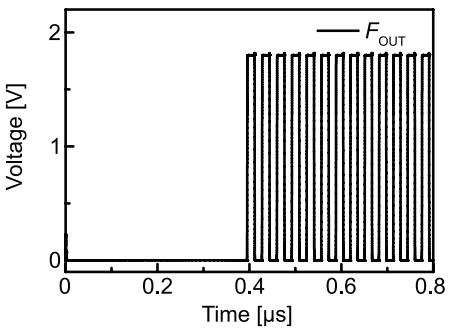

Fig. 8 Simulated start-up waveform.

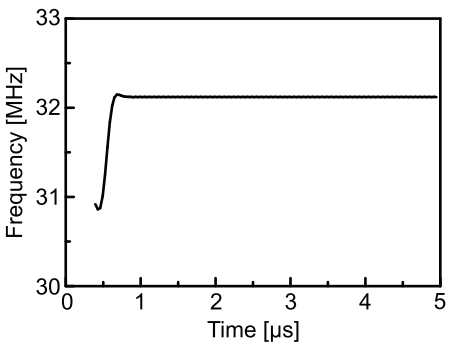

Fig. 9 Simulated output frequency.

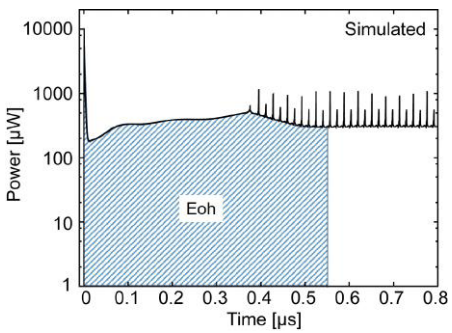

Fig. 10 Start-up energy.

was 261.9 pJ.

To investigate the circuit operation against process variation, we performed 1,000-run Monte Carlo statistical circuit simulations assuming die-to-die (D2D) global variations and within-die (WID) random mismatch variations in all MOSFETs using the parameters provided by the manufacturer. Figure 11 shows the simulated histogram of the output frequency at room temperature. The mean and standard deviation of the frequency were 32.2 and 0.25 MHz, respectively. The coefficient of variation was 0.79%. We confirmed that the variation of the frequency can be suppressed significantly.

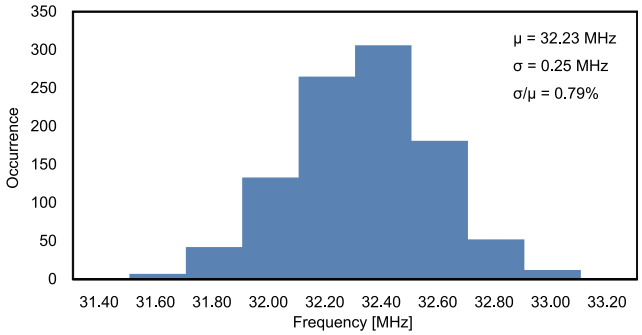

Fig. 11 Simulated histogram of frequency.

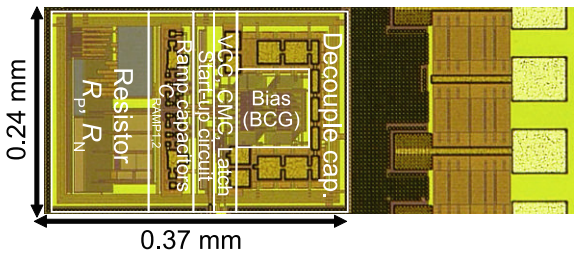

Fig. 12 Micrograph of prototype chip.

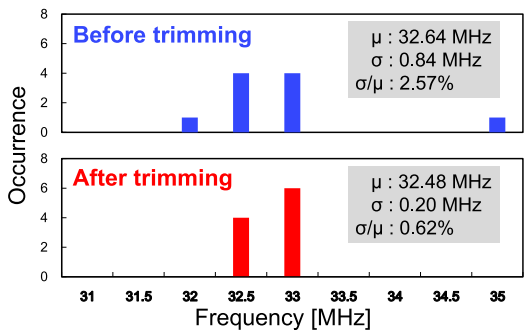

Fig. 13 Measured histogram before and after trimming.

3.2 Measurement

A prototype chip was fabricated with the same technology. Figure 12 shows a micrograph of our prototype chip. The chip area was 0.09 mm^2. With the digital codes, the R_P, R_N, and C_{RAMP} can be changed in the range of $5.7 < R_P < 12.7$ kΩ, $7.8 < R_N < 14.8$ kΩ, and $476.1 < C_{RAMP} < 618.1$ fF, respectively.

To investigate the stability against process variation, we measured the characteristics of 10 chips. Figure 13 shows the measured histograms of the output frequency before and

Fig. 14 Measured start-up waveform.

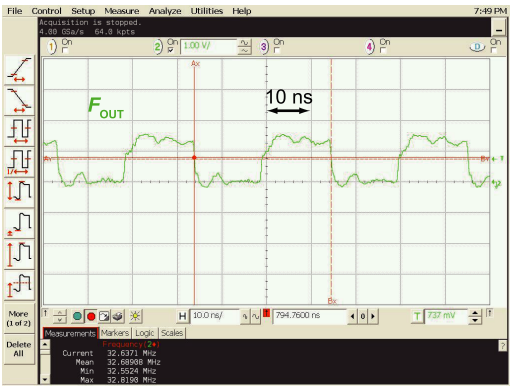

Fig. 15 Measured output waveform.

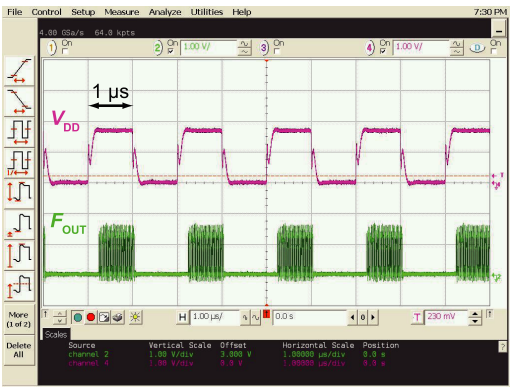

Fig. 16 Measured intermittent waveform.

after trimming at room temperature with a 1.8-V power supply. After trimming, the mean and standard deviation of the frequency were 32.5 and 0.20 MHz, respectively. The coefficient of variation was 0.62%. Thus, we achieved small frequency variation for 10 chips.

Figures 14 and 15 show the measured start-up and steady state waveform of our ROSC, respectively, at room temperature with a 1.8-V power supply. The start-up time was within 1 μs. The oscillation frequency and the power dissipation were 32.6 MHz and 300.6 μW, respectively.

Figure 16 shows the measured intermittent waveform.

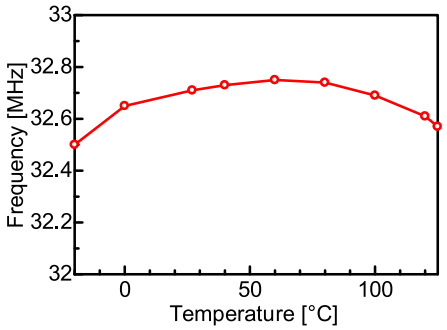

Fig. 17 Measured output frequency as a function of temperature.

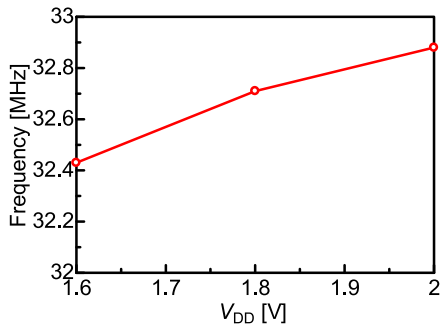

Fig. 18 Measured output frequency as a function of voltage.

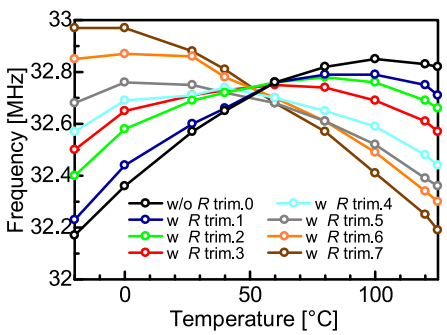

Fig. 19 Measured frequency with resistor trimming.

It could be confirmed that the proposed circuit repeats start-up and stand-by at intervals of 1 μs.

Figure 17 shows the measured output frequency as a function of temperature from −20 to 125 ℃ at 1.8-V power supply. The frequency variation with temperature was ±0.38%. Figure 18 shows the measured output frequency as a function of power supply. The frequency variation with supply voltage was ±0.69%. The proposed circuit achieved small temperature coefficient and low supply voltage dependence.

To evaluate the performance of the trimming circuits, we measured the output frequency by changing trimming codes. Figure 19 shows the measured output frequency as a function of temperature with different resistor trimming codes. The RTC can control the temperature coefficient of the frequency. The temperature coefficients were in the range of −5.34 to 4.48 kHz/℃ by changing trimming code.

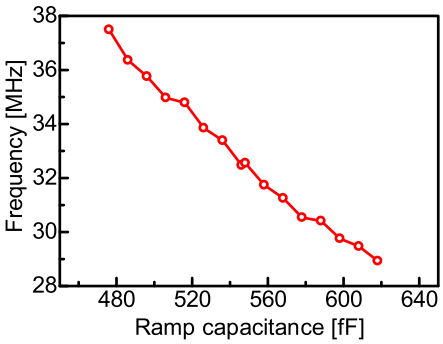

Fig. 20 Measured frequency with capacitor trimming.

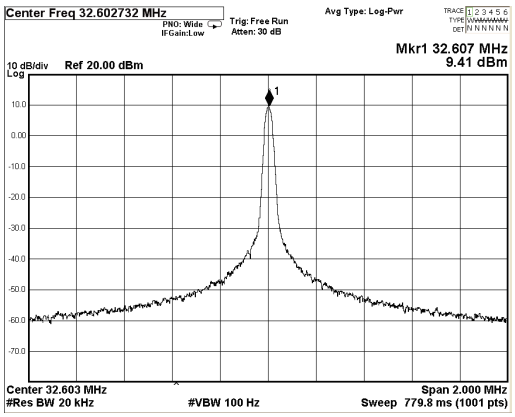

Fig. 21 Measured spectrum.

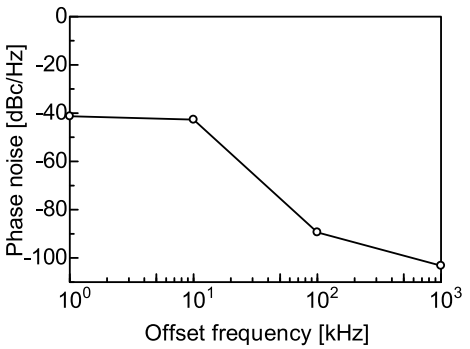

Fig. 22 Measured phase noise.

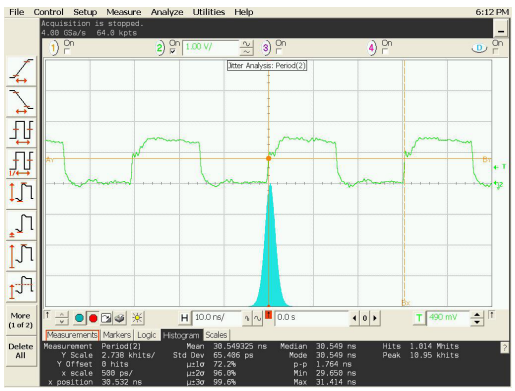

Fig. 23 Measured Jitter.

Figure 20 shows the measured output frequency with different capacitor trimming codes at room temperature. The frequency can be controlled in the range of 28.9 to 37.5 MHz.

Figures 21 and 22 show the frequency spectrum and phase noise as a function of the offset frequencies. The phase noises were −41.3, −42.7, −89.4, and −103.2dBc/Hz at 1, 10, 100 kHz, and 1 MHz, respectively. Figure 23 shows the measured jitter. The rms jitter was 66 ps_{rms} at 1Msamples.

It is well known that the clock jitter degrades the analog-to-digital converter (ADC) performance significantly [22]. Suppose that an ADC has an intrinsic signal-to-noise ratio SNR_{ADC}, that is determined by quantization and thermal noise and dependent on the ADC architecture. The overall SNR_{Total}, that includes the intrinsic performance of the ADC and the effect of the clock jitter, can be expressed as

$$SNR_{Total} = -20\log\sqrt{10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{Jitter}}{10}\right)}}, \quad (13)$$

where SNR_{Jitter} is the SNR with jitter [22]. The SNR_{Jitter} is defined as

$$SNR_{Jitter} = -20\log\left(\Delta t_{rms} 2\pi f_{in}\right), \quad (14)$$

where Δt_{rms} is the rms jitter and f_{in} is the input signal frequency [22]. From Eqs. (13) and (14), we can estimate the effect of the jitter. Figure 24 shows the calculated SNR_{Total} as a function of the input signal frequency with different SNR_{ADC}s. As shown in Fig. 24, the SNR_{Total} rolled of at 0.45, 1.35, 7.5 MHz when SNR_{ADC} were set to 75, 65, and 50dB, respectively. Therefore, our proposed ROSC can be used correctly below the frequencies.

The performance is summarized in Table 1 and compared with the-state-of-the-art clock generators. Our proposed fully-integrated ROSC achieved a small frequency variation, wide temperature range, and the fastest start-up time ever reported. Power dissipation of our proposed circuit was large compared with others. This is because our proposed circuit consists of almost analog circuits. Therefore, power dissipation strongly depends on the bias current flowing in each current path. The analog circuits in our proposed ROSC dissipated 288 μW. We can reduce the power

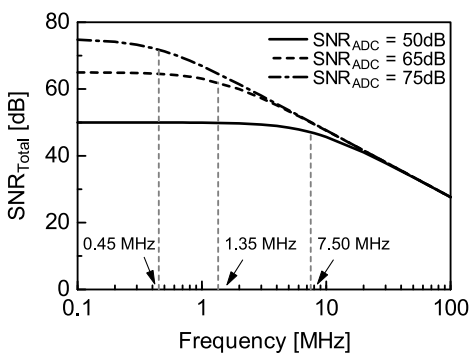

Fig. 24 Calculated SNR_{Total} as a function of input signal frequency. Clock jitter was set to 66 ps. SNR_{ADC} were set to 75, 65, and 50dB.

Table 1 Performance summary and comparison.

Ref.	[5]	[8]	[9]	[10]	[11]	[12]	[13]	[14]	This work
Type	X-tal	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation
Tech. (nm)	65	180	180	180	180	180	180	350	180
Area (mm^2)	0.08	0.14	0.14	0.015	0.032	0.012	0.013	0.08	0.09
V_{DD} (V)	1.68	1.9 - 3.0	1.4 - 1.9	1.4 - 2.0	1.7 - 1.9	0.6 - 1.1	1.5 - 3.6	1.8 - 3.0	1.6 - 2.0
T (℃)	−40 - 90	NA	−40 - 125	−40 - 125	−40 - 125	−30 - 120	−40 - 85	−20 - 100	−20 - 125
f_{CLK} (MHz)	24	2.02	25	10.5	14	12.77	32.8	30	32.6
Start-up time (μs)	64	NA	15*	NA	NA	NA	5*	2.5*	<1
Power (μW)	393	12	39.6*	219.8	43.2	56.2	16.6	180	300.6
FoM (μW/MHz)°	9.74	5.94	1.58*	14.95	1.7	4.88	0.01	3.33	9.22
$\Delta f_V^{\dagger}/f_{CLK}$ (%)	NA	±0.06	±0.2*	±0.13	±0.16	±0.01	±0.27★	±2.4	±0.69★
$\Delta f_T^{\ddagger}/f_{CLK}$ (%)	NA	NA	±0.18*	±1.13	±0.19★	±0.4	±0.84★	±0.6	±0.38★
$\sigma_{f_{CLK}}/\mu_{f_{CLK}}$	NA	5.62	NA	NA	NA	<0.8	NA	2.7	0.62★
Ext. signal	X-tal	No	No	No	I_{BIAS}	No	I_{BIAS}	No	No

*: Simulated results, ★: After trimming, °: FoM = Power/f_{CLK}, †: Frequency variation with supply voltage, ‡: Frequency variation with temperature.

dissipation by lowering bias current, considering the trade-off between the bias current and frequency accuracy. We are now developing such a modified ROSC. Our circuit achieves a fast start-up operation and is useful for the intermittent systems.

4. Conclusion

We presented a fully integrated current mode ROSC capable of fast start-up time operation. The proposed ROSC employs the current mode architecture that is different from the conventional voltage mode architecture. The current comparator can operate high speed and generate a 32-MHz oscillation frequency. The measurement results demonstrated that the oscillation frequency was 32.6 MHz at room temperature with 1.8-V supply voltage. The start-up time was extremely fast, within 1 μs. The distribution of the output frequency achieved 0.62% after calibration.

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