

High Speed and High Responsivity Avalanche Photodiode Fabricated by Standard CMOS Process in Blue Wavelength Region*

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SUMMARY Quadrant silicon avalanche photodiodes (APDs) were fabricated by standard 0.18 μm CMOS process, and were characterized at 405 nm wavelength for Blu-ray applications. The size of each APD element is $50 \times 50 \mu\text{m}^2$. The dark current was 10 pA at low bias voltage, and low crosstalk of about -80 dB between adjacent APD elements was achieved. Although the responsivity is less than 0.1 A/W at low bias voltage, the responsivity is enhanced to more than 1 A/W at less than 10 V bias voltage due to avalanche amplification. The wide bandwidth of 1.5 GHz was achieved with the responsivity of more than 1 A/W, which is limited by the capacitance of the APD. We believe that the fabricated quadrant APD is a promising photodiode for multi-layer Blu-ray system.

key words: silicon, photodiode, avalanche photodiode, CMOS, blu-ray

1. Introduction

Optical communication has been realized in long-haul communication, and recently board-to-board and chip-to-chip optical interconnection have been actively studied. In order to realize optical interconnection, it is necessary to integrate optical devices such as light sources, optical waveguides, photodetectors with electronic circuits. Ge photodiodes on Si substrate have been actively studied by utilizing CMOS compatible process for a long wavelength region [1]–[4], while Si photodetectors and Si photoreceivers have also been realized by standard CMOS process for short wavelength region [5]–[10]. Si photodiodes fabricated by standard CMOS process are very attractive devices for cost effective systems such as short optical interconnection and optical sensing applications because of easy monolithic integration with electronic circuits on Si substrate. In [5]–[10], the Si photodiodes and photoreceivers were characterized only in 830 ~ 850 nm wavelength region, and the maximum bandwidth of a few GHz and the maximum avalanche gain of more than 100 were achieved. We have also designed and realized avalanche photodiodes by standard CMOS process (CMOS-APD) and have characterized at 830 nm wavelength [11]–[14]. The avalanche gain of more than 100 was achieved at less than 10 V bias voltage, and the maximum bandwidth was 8.4 GHz at the avalanche gain of about 10 and the responsivity of about 0.02 A/W. The gain-bandwidth

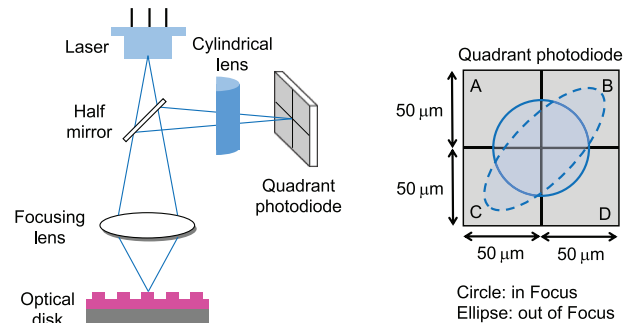


Fig. 1 Optical disk system.

product of 280 GHz was achieved [13].

The other possible application of the CMOS-APD is Blu-ray systems [15]–[17]. In Blu-ray systems, a laser diode emitting at 400 nm wavelength range is used as a light source, and a quadrant Si PIN photodiode (PIN-PD) is used for photodetection as shown in Fig. 1. The reflected light from the optical disk is detected by the quadrant PIN-PD through a cylindrical lens. The cylindrical lens is used so that the reflected light is circular shape for in focus and is ellipse shape for out of focus as shown in the right figure in Fig. 1. Then automatic focusing is realized by adjusting the height of the focusing lens so that the detected optical powers of four PIN-PD elements A, B, C and D satisfy the relation of $P_A \cdot P_D = P_B \cdot P_C$, where P_A , P_B , P_C and P_D are the detected optical power of PIN-PD elements A, B, C and D, respectively.

In current Blu-ray systems, a Si PIN-PD with the responsivity of about 0.3 A/W at 405 nm wavelength is used for photodetection. Since the data rate for 1× readout speed is 36 Mbps, 12× readout speed, for example, is 432 Mbps, which requires at least 200 MHz bandwidth for photodiodes. In [15], avalanche photodiodes were fabricated and were characterized in 300 ~ 1000 nm wavelength range. At 430 nm wavelength, the responsivity is 0.18 A/W at zero bias voltage and is increased to 4.6 A/W at 19.1 V bias voltage due to avalanche amplification, which corresponds to the avalanche gain of about 25. However, no frequency response and bandwidth were reported. In [16], CMOS photodiodes were fabricated and were characterized at 400 nm and 638 nm wavelength. At 400 nm wavelength, the high responsivity of 0.23 A/W was achieved by antireflection coating on the photodetection area, and the rise time of 1.0 ns and the fall time of 1.1 ns were achieved for 1 k Ω load resis-

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tance and 3 V bias voltage. However, no avalanche amplification was reported in this device.

In future Blu-ray systems, multi-layer optical disks will be used to increase the disk capacity. In this case, the reflected optical power from each layer is very low because the layers are semi-transparent, and then highly sensitive photodiodes at 400 nm wavelength range are required for photodetection. Although APDs are promising devices, conventional APDs require high voltage (about 150 V) to achieve large avalanche gain, and then integration with electronic circuits is difficult. The CMOS-APD has a feature of high-speed and high avalanche gain at low bias voltage, and therefore, is very attractive in multi-layer Blu-ray systems. We reported tentative responsivity and bandwidth of CMOS-APDs at 405 nm in [17]. The responsivity was 0.071 A/W at zero bias voltage and was enhanced to 2.61 A/W (avalanche gain of 36.8) at 9.1 V bias voltage due to avalanche amplification, and the bandwidth was 300 MHz, which was limited by uncalibrated frequency response of a blue laser.

In this paper, we characterize quadrant CMOS-APDs fabricated by standard CMOS process in blue wavelength region. Quadrant structure is widely used in optical disk system for automatic focusing of the laser beam as described above. The fabricated quadrant CMOS-APDs are low dark current of 10 pA for low bias voltage, and the crosstalk between CMOS-APDs is very low. The bandwidth of 1.5 GHz is achieved with the responsivity of more than 1 A/W.

2. Structure

Figure 2 is a photograph of the CMOS-APD fabricated by standard 0.18 μm CMOS process. The CMOS-APD is quadrant structure and four APD (APD-A, APD-B, APD-C, and APD-D) are formed. Nine electrodes in the bottom of the photograph are PADS for biasing and RF probing, where the PADS labeled “G” are the GND PADS and the PADS labeled “S” are the signal PADS for biasing and RF probing. The PAD size is $72 \times 72 \mu\text{m}^2$.

Figure 3 shows sample photographs of the photodetection area of the fabricated quadrant CMOS-APDs. Each APD has interdigital electrode structure, and the electrode spacing L_s is $24.64 \mu\text{m}$ and $7.52 \mu\text{m}$ for (a) and (b), respectively. The direction of the electrodes are decided to shorten wiring length to the PADS shown in Fig. 2. Figure 3(a) and (b) are the pMOS-type and the nMOS-type structure, respectively, and the detailed structure is explained below. The size of each APD element is $50 \times 50 \mu\text{m}^2$, which is the same size with the Si PIN-PD used in current Blu-ray systems. The separation between adjacent APD elements is $4 \mu\text{m}$ and $10 \mu\text{m}$ for (a) and (b), respectively.

Figure 4 shows the structure of the fabricated pMOS-type CMOS-APDs; (a) and (b) are the structure with the electrode spacing $L_s = 7.52 \mu\text{m}$ and $L_s = 24.64 \mu\text{m}$, respectively, and (c) is the schematic band diagram, where closed circles and open circles are electrons and holes, respectively. The interdigital anode and cathode electrodes are formed on the p^+ -layer and the n^+ -layer on the Nwell, respectively.

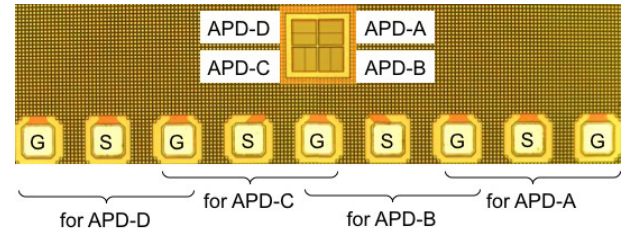
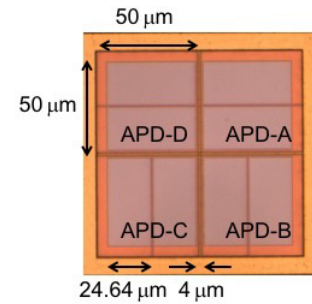
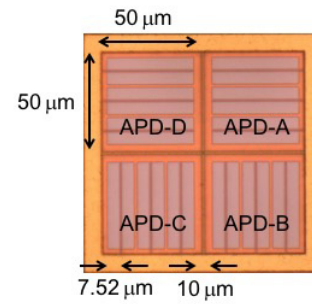


Fig. 2 Photograph of fabricated quadrant CMOS-APD.



(a) pMOS-type CMOS-APD with $L_s = 24.64 \mu\text{m}$.



(b) nMOS-type CMOS-APD with $L_s = 7.52 \mu\text{m}$.

Fig. 3 Photograph of photodetection area of fabricated CMOS-APD.

The cathode electrodes are connected to GND and the anode electrodes are negative biased. The p^+ -layers on the P-substrate are electrically connected to GND to form guard ring. The light with 405 nm wavelength is illuminated from the top of the APD and is absorbed through the silicide-free p^+ -layer on the Nwell. From optical property of intrinsic Si [18], the absorption length of Si at 405 nm wavelength is about 100 nm. Although the thickness and the doping concentration of the Nwell, the n^+ -layer and the p^+ -layer are not disclosed from manufacturer, the thickness of the n^+ -layer and the p^+ -layer is deduced to be $100 \sim 200 \text{ nm}$. Then most of the illuminated light is absorbed in the p^+ -layer and the Nwell. The holes photo-generated in the p^+ -layer immediately contribute to the photocurrent via anode electrode on the p^+ -layer, and the electrons photo-generated in the p^+ -layer are diffused toward the interface between the p^+ -layer and the Nwell and then drifted toward the n^+ -layer, and contribute to the photocurrent. The holes and the electrons photo-generated in the Nwell are drifted toward the p^+ -layer and the n^+ -layer on the Nwell, respectively, and contribute to the photocurrent. The electrons photo-generated in the P-substrate travel toward the n^+ -layer on the Nwell,

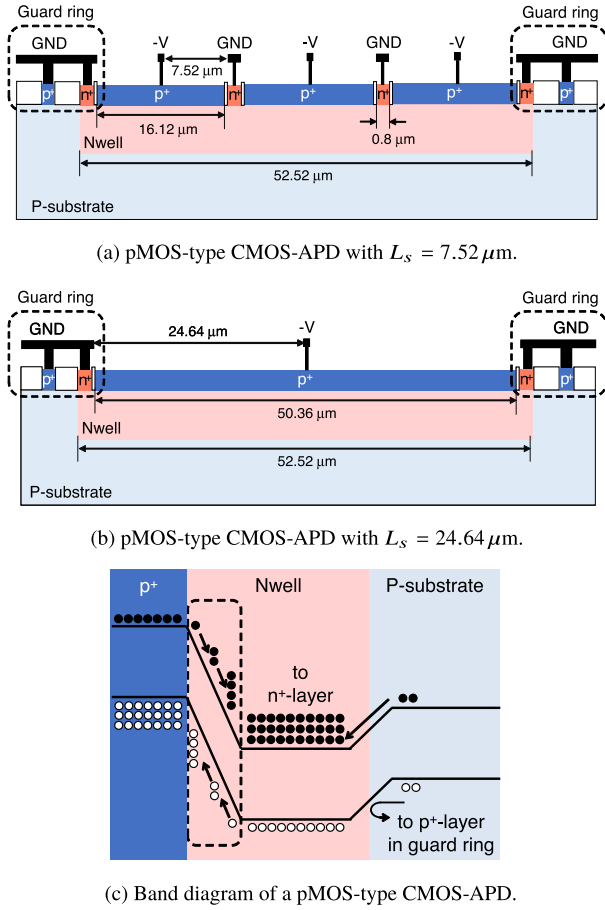


Fig. 4 Structure and band diagram of pMOS-type CMOS-APDs.

and the holes photo-generated in the P-substrate travel toward the p^+ -layer in the guard ring because of the built-in potential barrier between the P-substrate and the Nwell as shown in Fig. 4 (c), and the electrons and the holes are recombined by the guard ring structure and do not contribute to the photocurrent. In this structure, high electric field is applied around the interface between the p^+ -layer and the Nwell as shown in dashed region in Fig. 4 (c), and then the electrons photo-generated in the p^+ -layer and the holes photo-generated in the Nwell are multiplied due to avalanche mechanism during drifting toward the n^+ -layer and the p^+ -layer, respectively.

Figure 5 shows the structure of the fabricated nMOS-type CMOS-APDs; (a) and (b) are the structure with the electrode spacing $L_s = 7.52 \mu\text{m}$ and $L_s = 24.64 \mu\text{m}$, respectively, and (c) is the schematic band diagram, where closed circles and open circles are electrons and holes, respectively. The interdigital anode and the cathode electrodes are formed on the p^+ -layer and the n^+ -layer on the Pwell, respectively. The anode electrodes are connected to GND and the cathode electrodes are positive biased. The p^+ -layer on the Pwell, the p^+ -layer on the P-substrate, and the n^+ -layers on the deep Nwell (DNW) are electrically connected to GND to form guard ring. The light with 405 nm wavelength is illuminated from the top of the APD and is ab-

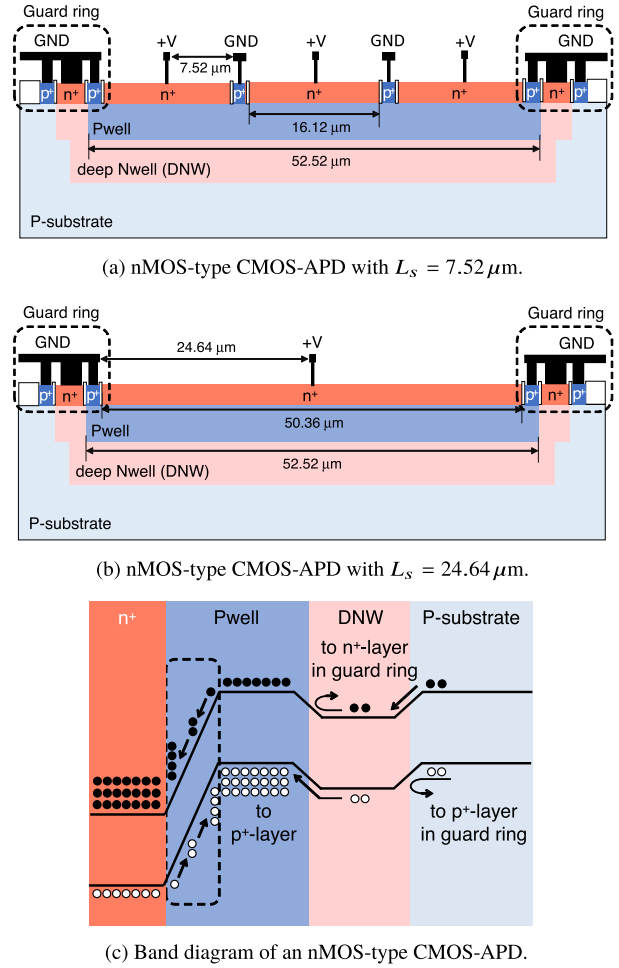


Fig. 5 Structure and band diagram of nMOS-type CMOS-APDs.

sorbed through the silicide-free n^+ -layer on the Pwell. Although the thickness and the doping concentration of the DNW, the Pwell, the n^+ -layer and the p^+ -layer are not disclosed from manufacturer, the thickness of the n^+ -layer and the p^+ -layer is deduced to be $100 \sim 200 \text{ nm}$, and is comparable to the absorption length of Si at 405 nm as described above. Then most of the illuminated light is absorbed in the n^+ -layer and the Pwell. The electrons photo-generated in the n^+ -layer immediately contribute to the photocurrent via cathode electrodes on the n^+ -layer, and the holes photo-generated in the n^+ -layer are diffused toward the interface between the n^+ -layer and the Pwell and then drifted toward the p^+ -layer on the Pwell, and contribute to the photocurrent. The electrons and the holes photo-generated in the Pwell are drifted toward the n^+ -layer and the p^+ -layer on the Pwell, respectively, and contribute to the photocurrent. The holes photo-generated in the DNW travel toward the p^+ -layer on the Pwell, and the electrons photo-generated in the DNW travel toward the n^+ -layer in the guard ring because of the built-in potential barrier between the Pwell and the DNW, and the holes and the electrons are recombined and do not contribute to the photocurrent. The electrons photo-generated in the P-substrate travel toward the n^+ -layer in the

guard ring because of the built-in potential barrier between the Pwell and the DNW, and the holes photo-generated in the P-substrate travel toward the p⁺-layer in the guard ring because of the built-in potential barrier between the DNW and the P-substrate, and the electrons and the holes are recombined and do not contribute to the photocurrent. In this structure, high electric field is applied around the interface between the n⁺-layer and the Pwell as shown in dashed region in Fig. 5 (c), and then the holes photo-generated in the n⁺-layer and the electrons photo-generated in the Pwell are multiplied due to avalanche mechanism during drifting toward the p⁺-layer and the n⁺-layer, respectively.

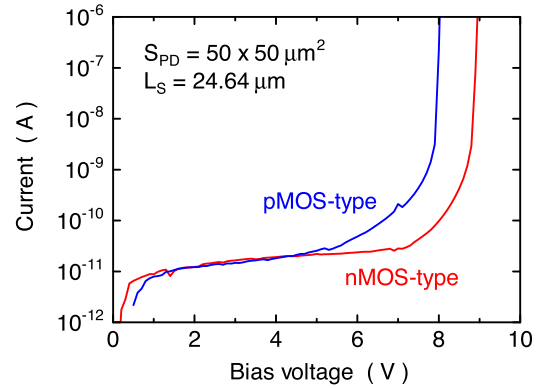
In the CMOS-APDs, the bandwidth is enhanced by decreasing the electrode spacing because the carrier transit time to the electrodes is decreased at the sacrifice of the responsivity due to increased illumination blocking area by electrodes. To confirm the influence of the electrode spacing on the bandwidth and the responsivity, we fabricated CMOS-APDs with different electrode spacing as shown in Figs. 3, 4 and 5. No antireflection coating is formed on the photodetection area because antireflection coating is not provided in standard CMOS process.

3. Characterization

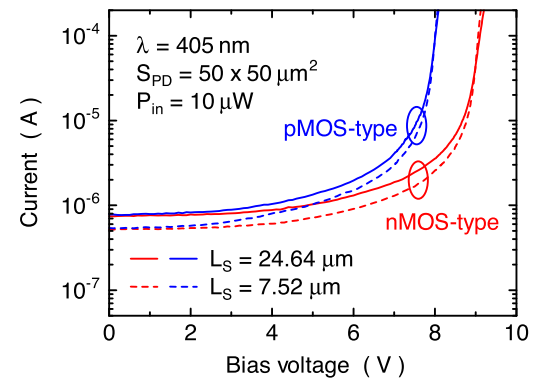
In characterizing the CMOS-APDs, a laser light with 405 nm wavelength was illuminated from the top of the CMOS-APDs via SI-9 optical fiber, which is multimoded for 405 nm wavelength. The output facet of the SI-9 fiber was aligned about 100 μm upper from the surface of the CMOS-APDs, and the beam size on the photodetection area was about 20 μm as a result.

Figure 6(a) shows the dark current of the pMOS-type and the nMOS-type CMOS-APDs with the electrode spacing $L_s = 24.64 \mu\text{m}$. The dark current is about 10 pA at low bias voltage for both the pMOS-type and the nMOS-type CMOS-APDs, which is comparable to the dark current of commercial Si PIN-PDs, and is drastically increased when the bias voltage exceeds 6 V and 8 V for the pMOS-type and the nMOS-type CMOS-APDs, respectively. The breakdown voltage is about 8 V and 9 V for the pMOS-type and the nMOS-type CMOS-APDs, respectively. The dark current characteristics is the same irrespective of the electrode spacing L_s . Figure 6(b) shows the I - V characteristics under light illumination. The wavelength of the light is 405 nm and the incident optical power is 10 μW . The current is almost constant when the bias voltage is below 4 V and 6 V for the pMOS-type and the nMOS-type CMOS-APDs, respectively, and is gradually increased; especially when the bias voltage is above 7 V and 8 V for the pMOS-type and the nMOS-type CMOS-APDs, respectively, the current is significantly increased due to avalanche amplification, which occurs around the interface between the p⁺-layers and Nwell for the pMOS-type CMOS-APD and between the n⁺-layers and the Pwell for the nMOS-type CMOS-APD.

Figure 7 shows the responsivity against the bias voltage obtained from Fig. 6(b). The responsivity at low bias



(a) Dark current



(b) Photocurrent for $P_{in} = 10 \mu\text{W}$

Fig. 6 I - V characteristics of pMOS-type and nMOS-type CMOS-APDs.

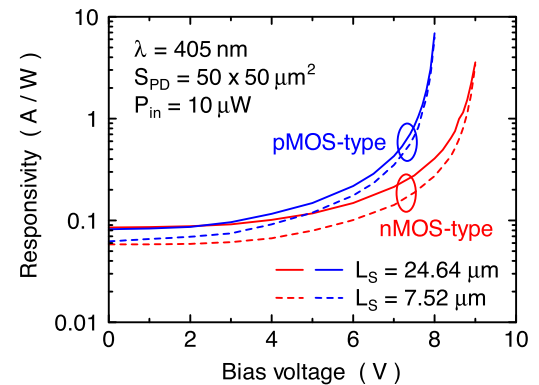
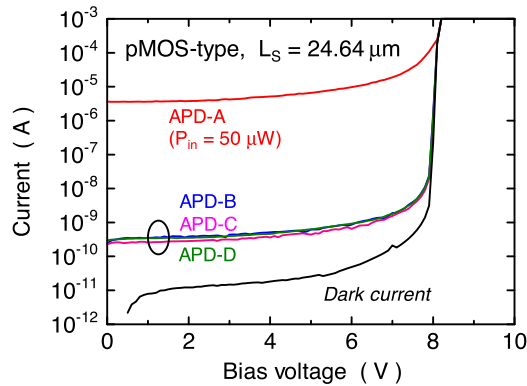
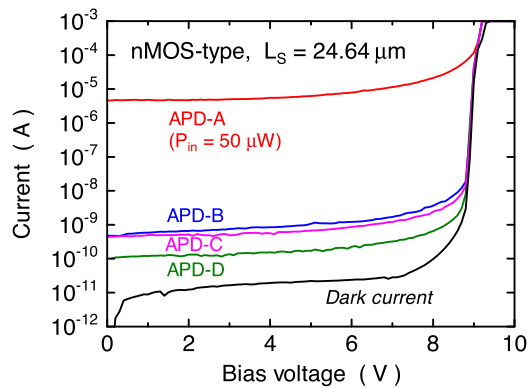


Fig. 7 Responsivity against bias voltage for pMOS-type and nMOS-type CMOS-APDs.

voltage is less than 0.1 A/W and is about half of commercial Si PIN-PD at 405 nm. The low responsivity at low bias voltage is attributed to surface reflection due to no antireflection coating. However the responsivity is significantly increased due to avalanche amplification, and the responsivity of more than 1 A/W is achieved, which is about 10 times larger than the responsivity of commercial Si PIN-PD. The avalanche gain of more than 10 is easily achieved and the maximum avalanche gain of 100 is achieved by carefully adjusting the bias voltage. The responsivity is enhanced by increasing the



(a) pMOS-type CMOS-APD



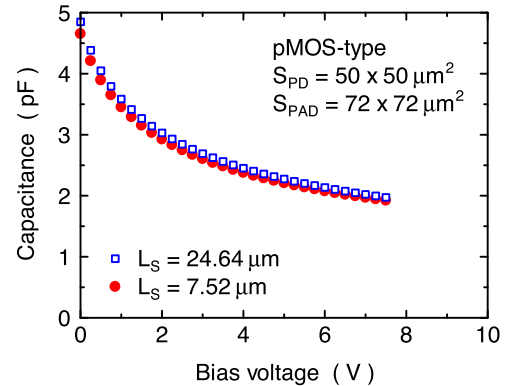
(b) nMOS-type CMOS-APD

Fig. 8 I - V characteristics of quadrant pMOS-type and nMOS-type CMOS-APDs when a laser light is illuminating onto one of the CMOS-APD.

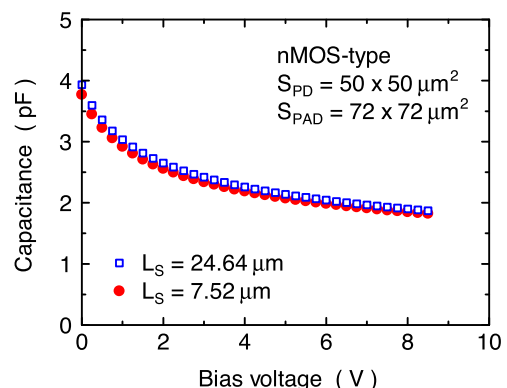
electrode spacing L_s because of decreased number of the interdigital electrodes which blocks light absorption.

Figure 8 shows the I - V characteristics of all the APD elements of the quadrant CMOS-APD when a light is illuminated to only the APD-A. Figure 8 (a) and (b) are the results for the pMOS-type and the nMOS-type CMOS-APDs, respectively. Large current is measured for the APD-A due to efficient light absorption. The current of the APD-B, APD-C and APD-D are slightly increased. The reason of the slight current increase is not clear yet, and may be misalignment of the light illumination or insufficient isolation between the APD elements due to common GND PAD structure as shown in Fig. 2. However the current of the APD-B, APD-C and APD-D is four orders of magnitude smaller than the current of the APD-A, which indicates that the crosstalk is -80 dB.

Figure 9 shows the C - V characteristics for (a) the pMOS-type and (b) the nMOS-type CMOS-APDs. The capacitance of the CMOS-APD with the electrode spacing $L_s = 24.64 \mu\text{m}$ is slightly larger than that with $L_s = 7.52 \mu\text{m}$ because of larger pn-junction area due to small number of the interdigital electrodes. The capacitance of the pMOS-type CMOS-APD is slightly larger than that of the nMOS-type CMOS-APD at low bias voltage. The difference in the



(a) pMOS-type CMOS-APD.



(b) nMOS-type CMOS-APD.

Fig. 9 C - V characteristics for pMOS-type and nMOS-type CMOS-APDs.

capacitance may be due to different doping concentration of the Nwell and the Pwell. However the capacitance of the pMOS-type and the nMOS-type CMOS-APDs are almost the same for the bias voltage above 5 V, and finally the capacitance of about 2 pF is achieved near the breakdown voltage. The CR-limited bandwidth of the CMOS-APD is then estimated to be 1.6 GHz for 50 Ω load resistance.

Figure 10 shows the frequency response at 8 V bias voltage for (a) the pMOS-type and (b) the nMOS-type CMOS-APDs. A laser diode with 405 nm wavelength is used as a light source and the laser is directly intensity modulated by the RF signal of a network analyzer (Agilent technology, E8363B). The frequency response of the laser is calibrated with a high-speed GaAs PIN-PD with nominal bandwidth of 30 GHz (Albis Optoelectronics AG, PQW-30A-S). The vertical axis is normalized to the signal magnitude at low frequency range. The bandwidth is enhanced with decreasing the electrode spacing L_s due to decreased carrier transit time, and the bandwidth of about 1.5 GHz is achieved for the pMOS-type and the nMOS-type CMOS-APDs with the electrode spacing $L_s = 7.52 \mu\text{m}$, which is limited by the capacitance as shown in Fig. 9.

Finally we summarize the relation between the responsivity and the bandwidth at 405 nm wavelength, and the re-

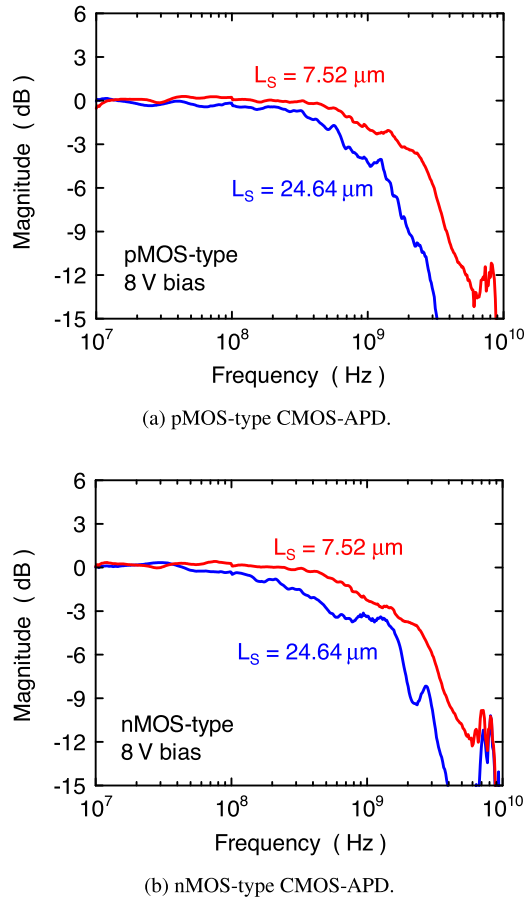


Fig. 10 Frequency response at 8 V bias voltage for pMOS-type and nMOS-type CMOS-APDs.

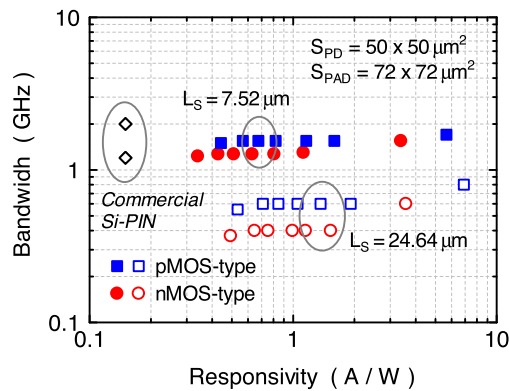


Fig. 11 Relation between responsivity and bandwidth.

sult is shown in Fig. 11. Closed and open squares are the results for the pMOS-type CMOS-APD, and closed and open circles are the results for the nMOS-type CMOS-APD. The CMOS-APD with the electrode spacing $L_s = 7.52 \mu\text{m}$ has wider bandwidth than that with $L_s = 24.64 \mu\text{m}$ due to decreased carrier transit time, and the pMOS-type CMOS-APD is slightly faster than the nMOS-type CMOS-APD. As described in Sect. 2, the holes photo-generated in the p^+ -layer immediately contribute to the photocurrent via electrodes on the p^+ -layer, and the electrons photo-generated in

the p^+ -layer travel toward the n^+ -layer via Nwell and then contribute to the photocurrent in the pMOS-type CMOS-APD. In the nMOS-type CMOS-APD, the electrons photo-generated in the n^+ -layer immediately contribute to the photocurrent via electrodes on the n^+ -layer, and the holes photo-generated in the n^+ -layer travel toward the p^+ -layer via Pwell and then contribute to the photocurrent. Since the drift velocity of electrons is faster than that of holes, the pMOS-type CMOS-APD is faster than the nMOS-type CMOS-APD.

The horizontal axis of Fig. 11 is scaled with the responsivity, and the responsivity is related to the avalanche gain. Hence Fig. 11 is basically the same with the gain-bandwidth characteristics. In usual APDs, the bandwidth is increased with the gain in low gain region due to increased drift velocity by increased bias voltage, and is then decreased with the gain in high gain region by increased avalanche build-up time. However the relation shown in Fig. 11 is flat with the responsivity. This is because the bandwidth is limited by the CR-limited bandwidth for $L_s = 7.52 \mu\text{m}$, and is limited by the carrier transit time-limited bandwidth for $L_s = 24.64 \mu\text{m}$, and the CR-limited bandwidth and the carrier transit time-limited bandwidth are narrower than the avalanche build-up time-limited bandwidth.

4. Conclusion

In conclusion, quadrant Si CMOS-APDs were fabricated by standard $0.18 \mu\text{m}$ CMOS process and were characterized at 405 nm wavelength for Blu-ray application. The photodetection size of each CMOS-APD is $50 \times 50 \mu\text{m}^2$, and interdigital anode and cathode electrodes are formed on the surface of the CMOS-APD. The dark current is 10 pA at low bias voltage and the breakdown voltage is about 8 V and 9 V for the pMOS-type and the nMOS-type CMOS-APDs, respectively. The responsivity is less than 0.1 A/W at low bias voltage, and is increased to more than 1 A/W near the breakdown voltage due to avalanche amplification. The crosstalk between APD elements is as low as -80 dB . The capacitance near the breakdown voltage is 2 pF for both the pMOS-type and the nMOS-type CMOS-APDs. The bandwidth is enhanced with decreasing the electrode spacing, and the maximum bandwidth was 1.5 GHz for the pMOS-type CMOS-APD, which is limited by the CR-limited bandwidth. The bandwidth is independent of the responsivity because the bandwidth is limited by the CR-limited bandwidth for narrower electrode spacing and by the carrier transit-time bandwidth for wider electrode spacing, and the 1.5 GHz bandwidth is obtained with the responsivity of more than 1 A/W. The results show that the quadrant CMOS-APD is very attractive device for Blu-ray application.

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References

- [1] M. Jutzi, M. Berroth, G. Wöhl, M. Oehme, and E. Kasper, "Ge-on-Si vertical incidence photodiodes with 39-GHz bandwidth," *IEEE Photon. Technol. Lett.*, vol.17, no.7, pp.1510–1512, 2005.
- [2] Z. Huang, N. Kong, X. Guo, M. Liu, N. Duan, A.L. Beck, S.K. Banerjee, and J.C. Campbell, "21-GHz-bandwidth Germanium-on-Silicon photodiode using thin SiGe buffer layers," *IEEE J. Sel. Top. Quantum Electron.*, vol.12, no.6, pp.1450–1454, 2006.
- [3] S. Klinger, M. Berroth, M. Kaschel, M. Oehme, and E. Kasper, "Ge-on-Si p-i-n photodiodes with a 3-dB bandwidth of 49 GHz," *IEEE Photon. Technol. Lett.*, vol.21, no.13, pp.920–922, 2009.
- [4] J. Michel, J. Liu, and L.C. Kimmerling, "High-performance Ge-on-Si photodetectors," *Nature Photonics*, vol.4, pp.527–534, DOI: 10.1038/NPHOTON.2010.157, 2010.
- [5] T.K. Woodward and A.V. Krishnamoorthy, "1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies," *IEEE J. Sel. Top. Quantum Electron.* vol.5, no.2, pp.146–156, 1999.
- [6] B. Yang, J.D. Schaub, S.M. Csutak, D.L. Rogers, and J.C. Campbell, "10-Gb/s all-silicon optical receiver," *IEEE Photonics Technol. Lett.*, vol.15, no.5, pp.745–747, 2003.
- [7] S. Radovanović, A.-J. Annema, and B. Nauta, "A 3-Gb/s optical detector in standard CMOS for 850-nm optical communication," *IEEE J. Solid-State Circuits*, vol.40, no.8, pp.1706–1717, 2005.
- [8] W.-K. Huang, Y.-C. Liu, and Y.-M. Hsin, "A high-speed and high-responsivity photodiode in standard CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 19, no.4, pp.197–199, 2007.
- [9] H.-S. Kang, M.-J. Lee, and W.-Y. Choi, "Si avalanche photodetectors fabricated in standard complementary metal-oxide-semiconductor process," *Appl. Phys. Lett.*, vol.90, no.15, 151118, 2007.
- [10] M.-J. Lee and W.-Y. Choi, "A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product," *Opt. Express*, vol.18, no.23, pp.24189–24194, 2010.
- [11] K. Iiyama, N. Sannou, and H. Takamatsu, "Avalanche amplification in silicon lateral photodiode fabricated by standard 0.18 μm CMOS process," *IEICE Trans. Electron.*, vol.E91-C, no.11, pp.1820–1823, 2008.
- [12] K. Iiyama, H. Takamatsu, and T. Maruyama, "Holeinjection-type and electron-injection-type silicon avalanche photodiodes fabricated by standard 0.18 μm CMOS process," *IEEE Photon. Technol. Lett.*, vol.22 no.12, pp.932–934, 2010.
- [13] Z.A.F.M. Naipiah, R. Gyobu, T. Hishiki, T. Maruyama, and K. Iiyama, "Characterizing silicon avalanche photodiode fabricated by standard 0.18 μm CMOS process for high-speed operation," *IEICE Trans. Electron.*, vol.E99-C, no.12, pp.1304–1311, 2016.
- [14] Z.A.F.M. Naipiah, T. Hishiki, and K. Iiyama, "Wavelength dependence of silicon avalanche photodiode fabricated by CMOS process," *Optics & Laser Technology*, vol.92, pp.193–197, 2017.
- [15] A. Pauchard, A. Rochas, Z. Randjelovic, P.A. Besse, and R.S. Porpovic, "Ultraviolet avalanche photodiode in CMOS technology," in *Proc. International Electron Devices Meeting 2000 (IEDM 2000)*, 30.6., San Francisco, CA, 2000.
- [16] A. Ghazi, H. Zimmermann, and P. Seegebrecht, "CMOS photodiode with enhanced responsivity for the UV/blue spectral range," *IEEE Trans. Electron. Dev.*, vol.49, no.7, pp.1124–1128, 2002.
- [17] T. Shimotori, K. Maekita, T. Maruyama, and K. Iiyama, "Characterization of APDs fabricated by 0.18 μm CMOS process in blue wavelength region," 17th Opto-Electronics and Communications Conference (OECC 2012), 5D1-3, Busan, Korea, 2012.
- [18] M.A. Green, "Self-consistent optical parameters of intrinsic silicon at 300 K including temperature coefficient," *Solar Energy Materials & Solar Cells*, vol.92, no.11, pp.1305–1310, 2008.



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