FOREWORD

Special Section on Solid-State Circuit Design —Architecture, Circuit, Device and Design Methodology

Now a mobile phone almost manages our daily life such as communication, education, health care, business, and entertainment. Major portion of the smart functions have been realized by solid-state circuits. In the future, automobile will be more connected and be more autonomous. Major portion of the smart functions will be realized by solid-states circuits. Such contributions of solid-states circuits have been and will be driven by the endless efforts of the innovators including not only the authors but also the readers of this special section.

It is my great honor to announce the publication of this special section on solid-state circuits design. The section is devoted to a distinctive exploration of new techniques on integrated circuits. It contains 6 regular papers. Two papers discuss the FPGA architecture for 3D and the 3D low skew clock distribution both using through chip interface. In the high-speed wireless applications, 60 GHz CMOS transmitter with on-chip antenna is discussed. From the reliability perspective, neutron induced cell upset is discussed. As a basic circuit research, the method of enhancing gain of operational amplifier is discussed. Final paper discusses low latency DMR architecture.

On behalf of the editorial committee, I would like to express my sincere appreciation to all the authors for their contributions and to all the reviewers for their critical readings. Lastly, I would like to thank the editorial committee for their work on this special section.

Takeshi Yamamura, Guest Editor-in-Chief

Takeshi Yamamura *(Member)* is a principal researcher of Fujitsu Laboratories LTD., received B.S. and M.S. degrees from the University of Tokyo, Tokyo, Japan, in 1978 and 1981, respectively. He joined Fujitsu Ltd., Kawasaki, Japan, in 1981, where he worked on the development of mixed signal LSIs. He joined Fujitsu Laboratories Ltd., in 2004, where he has been working on the research and development of mixed signal LSIs.