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LETTER

CMOS Image Sensor with Pixel-Parallel ADC and HDR Reconstruction from Intermediate Exposure Images

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SUMMARY We propose a HDR (high dynamic range) reconstruction method in an image sensor with a pixel-parallel ADC (analog-to-digital converter) for non-destructively reading out the intermediate exposure image. We report the circuit design for such an image sensor and the evaluation of the basic HDR reconstruction method.

key words: *pixel-parallel ADC, high dynamic range reconstruction, intermediate exposure image, image sensor, non-destructively reading out*

1. Introduction

CMOS image sensors are widely used in various fields such as monitoring and mobile devices. Furthermore, in the coming years, applications of an image sensor for the purpose of recognition and machine control functions such as automatic driving, drones, and robot vision are expected to increase. In such applications, it is necessary to control and recognize the machines with high accuracy and speed under various illuminance environments, such as outdoors. Thus, it is desirable to acquire a high-definition image at high speed regardless of the illuminance available. However, as a shortened exposure time is necessary in high-speed imaging, the low illuminance area tends to remain underexposed. Therefore, we are studying an image sensor and an imaging method for acquiring a high-speed captured image and an image with sufficient exposure time.

Current CMOS image sensors often use a column-parallel A/D conversion architecture in which one A/D converter (ADC) is arranged for each column of a pixel array and the A/D conversion is performed by scanning one line at a time [1]. In this method, to perform high-speed image acquisition while maintaining the number of pixels, it is necessary to shorten the A/D conversion time arranged in one pixel. Thus, achieving a high frame rate is limited, which is a problem. In contrast, a pixel-parallel A/D conversion architecture arranges one ADC for each pixel [2]–[5]. This method is suitable for high-speed image acquisition because the A/D conversion is performed on all pixels simultaneously. In the study [2], the pixel-parallel ADC is composed of a comparator and digital memory. However, the drawback of this method is that the pixel size is large and the number of digital data lines increases. Therefore, the study [3] reported the reduction of the number of memories by writing to the memory in two steps, and the study [4] reported the reduction of data lines by switching the memory to a counter. In addition, the study [5] has been reported to effectively avoid the implementation area limitation by stacking photodiode on pixel-parallel ADC using a wafer-to-wafer bonding technique.

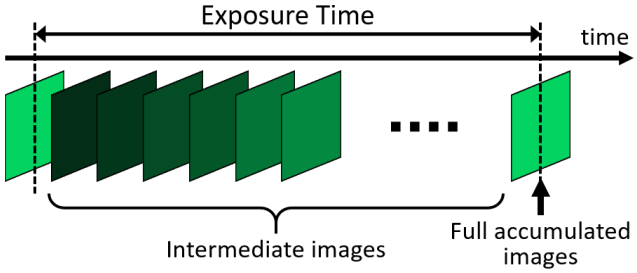

Fig. 1 Intermediate exposure images. An image sensor with a pixel-parallel ADC can read not only the full accumulated image, which is the output of popular image sensors, but also intermediate images during exposure.

Some parallel studies [6]–[9] have proposed an imaging method for acquiring images during the exposure. In this imaging method, intermediate images are acquired during the exposure period as shown in Fig. 1. Because each intermediate image has a different exposure time, we can acquire an image with a suitable exposure time even in different illuminance environments. Furthermore, various applications, such as image enhancement [7], optical flow estimation [8], and dynamic range expansion [9] can be achieved by using intermediate images. Therefore, by acquiring an intermediate image at a higher frame rate, we can gain more advantages and perform more applications for image sensing. In this paper, we propose an image sensor with a pixel-parallel ADC to readout intermediate images and also propose a method for reconstructing the high-gradation images from the intermediate images [10]. The proposed image sensor acquires the intermediate images at high speed, but uses low-resolution ADCs to avoid increasing the pixel size. In the studies [2], [3], the pixel layout in the 0.18um process shows that the memory area of the ADC occupies more than 40%

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of the total pixel area. In addition, the higher the resolution of ADC, the more the digital memory tends to control the pixel size, even if the microfabrication process with stacked structure is used. Therefore, the increase in pixel size can be suppressed in principle by AD conversion within a pixel to a lower resolution. Thus, we can reconstruct a high-gradation image by using low-gradation intermediate images.

2. Proposed Image Sensor

Figure 2(a) shows the configuration of the proposed image sensor. The image sensor includes a pixel array, a vertical shift register, a write control unit, sense amplifiers and a horizontal shift register. The pixel circuit (Fig. 2(b)) includes a photodiode (PD), a transfer transistor M1, a reset transistor M2, a source follower transistor M3, a current source transistor M4, a floating diffusion capacitance (C_{FD}), a comparator, and a dynamic random access memory (DRAM). By using a 4 transistor pixel structure with M1, a higher conversion gain can be achieved compared to a 3 transistor pixel structure, which increases sensitivity and reduces the input referred noise of the readout circuit in the later stage. The comparator and DRAM constitute the pixel-parallel ADC. The DRAM is connected to a sense amplifier and a write control circuit with a data bus for writing and reading.

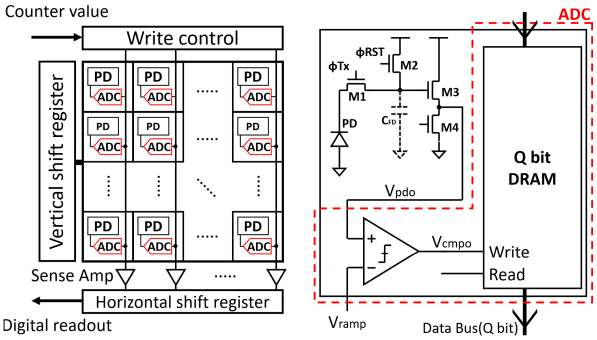
Figure 3 shows the timing chart of the pixel circuit. In normal imaging, the A/D conversion and readout are performed only once during the exposure period after reset and an image is acquired. On the other hand, in the acquisition of intermediate images, the A/D conversion and readout are repeatedly performed during the exposure period.

The acquisition process is as follows: First, M2 is turned off by setting ϕRST low, M1 is turned on by setting ϕTx high, and the potential of the FD node is reset. Thereafter, M2 is turned off, and just before each A/D conversion, M1 is turned on to transfer the charge output from the PD to the C_{FD}. The signal voltage V_{pdo} is the output from M3. In A/D conversion, V_{ramp} changes from V_{max} to V_{min} and is compared with V_{pdo}. The start of falling V_{ramp} is delayed from the start of counter code by half an interval of counter code. On the other hand, the end of the counter code is delayed by half an interval of the counter code from the end of falling V_{ramp}. The output V_{cmpo} of the comparator is connected to the DRAM write. Therefore, by inputting a counter code synchronized with V_{ramp} to the data bus, the DRAM holds the counter code when V_{cmpo} changes, thereby completing an A/D conversion operation.

In the readout period, as the columns share the data bus, scanning is performed to read data from the DRAMs, and an intermediate image is obtained.

3. HDR Reconstruction from Intermediate Images

In the proposed image sensor, a low-gradation intermediate image is acquired with high temporal resolution. The aim is to reconstruct a high-quality image using the characteristics of the intermediate image. In this section, we describe the



(a) Overview of image sensor. Each pixel circuit has own photodiode (PD) and ADC.

(b) Pixel circuit

Fig. 2 The proposed image sensor with pixel-parallel ADC.

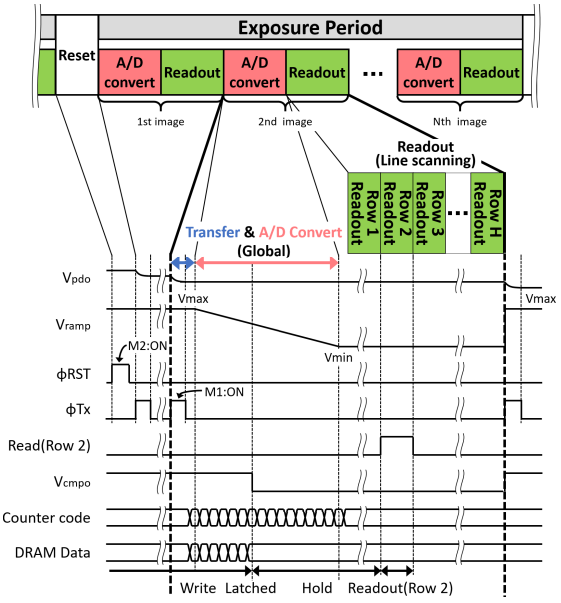


Fig. 3 Timing chart.

reconstruction of high-gradation images and HDR images using intermediate images.

When the light incident on the PD is constant, as in the static region, the charge is accumulated at a constant rate, and V_{pdo} changes with a constant slope. Therefore, the pixel value before the A/D conversion increases linearly as shown in Fig. 4. The pixel value of the intermediate image is obtained by quantizing V_{pdo} with A/D conversion. Therefore, the quantized pixel value changes stepwise, and the quantization error changes periodically between ±0.5 LSB. Using this quantization error feature, we cumulatively add the pixel values of the intermediate image to reduce the quantization error. We calculate the pixel value I_{recon} of the high-gradation reconstructed image:

$$I_{\text{recon}} = \frac{2}{N} \sum_{n=1}^{N} I_n, \tag{1}$$

where N is the total number of intermediate images and I_n is

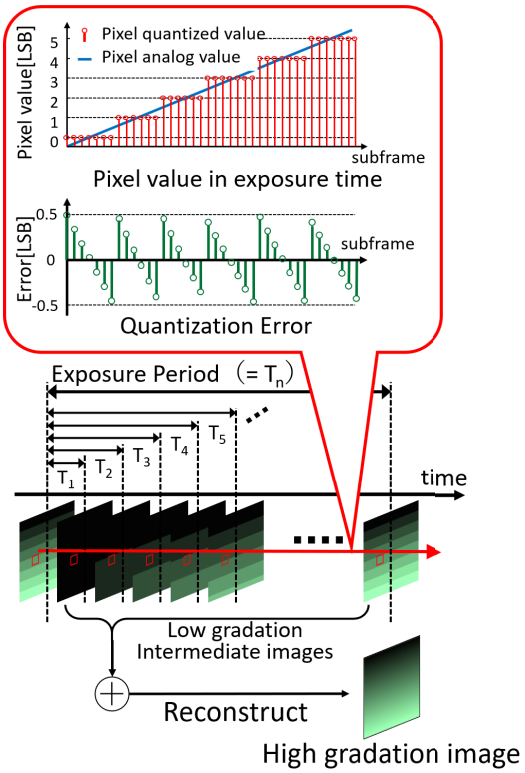


Fig. 4 Pixel value, quantized error, and reconstruction.

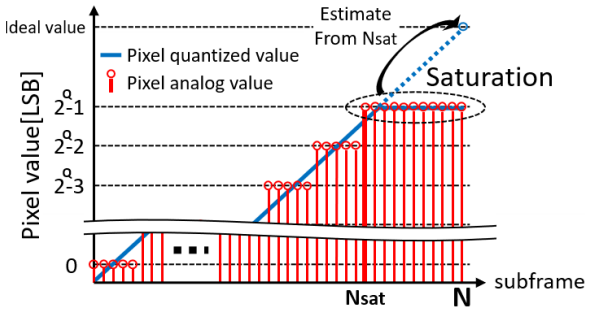


Fig. 5 Saturation detection and pixel value estimation.

(a) 32th (b) 64th (c) 128th

Fig. 6 Intermediate images (4 bits).

the pixel value of the n-th intermediate image. In an imaging scene with a strong contrast between light and dark, it is necessary to capture the low-illuminance area with a long exposure time, but the high-illuminance area gets saturated. In our proposed reconstruction method, as an intermediate image is repeatedly acquired during the exposure, we can acquire both the short exposure image before the saturation of the high-illuminance area and the long exposure image. Thus, we can reconstruct an HDR image using intermediate images. The reconstruction is accomplished by detecting the saturation time from the intermediate images. First, we detect the subframe number N_{sat} of the intermediate image that is saturated for the first time. If we acquire the intermediate images at a high frame rate, we can consider N_{sat} as the elapsed time from the start of exposure until saturation. Therefore, we calculate the HDR pixel value as shown in Fig. 5:

$$\left(2^Q - 1\right) \times \frac{N}{N_{\text{sat}}} \tag{2}$$

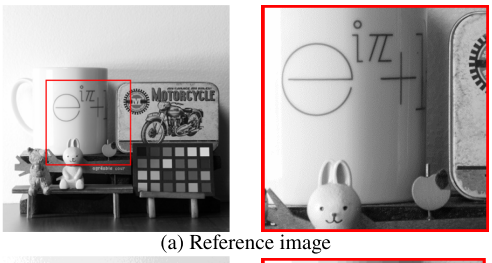
where N is the total number of intermediate image, and Q is the A/D conversion resolution. We assume that the pixel value at N_{sat} is $(2^Q - 1)$, which is the maximum value of A/D conversion. However, as the A/D conversion has a low resolution, the error is actually large. To minimize the effect of this error, high-gradation reconstruction is performed using Eq. (1) by using the first to N_{sat}-th intermediate images. Therefore, we reconstruct the pixel value I_{HDR} of the HDR image by using Eq. (3) that was obtained from Eq. (2):

$$I_{\text{HDR}} = \left(\frac{2}{N}\sum_{n=1}^{N_{\text{sat}}} I_n\right) \times \frac{N}{N_{\text{sat}}} \tag{3}$$

4. Evaluation of Simulation

In this section, we present the simulation results of the high-gradation and HDR image reconstruction methods using a low-gradation intermediate image, and evaluate its effectiveness. In the simulation, the resolution Q of A/D conversion is 4 bits, and the total number N of intermediate images acquired during the exposure period is 128 frames. Figure 6 shows the 32nd, 64th and 128th intermediate images used in the simulation. Figure 7 shows the result of the high-gradation reconstruction simulation using Eq. (1) in the scene where the saturation does not occur during the exposure period. As shown in Fig. 7(b), the low-gradation image has a false contour. On the other hand, in the reconstructed image shown in Fig. 7(c), because the gradation is reproduced, the image has no false contour, which confirms the effectiveness of the reconstruction method.

Figure 8 shows the intermediate images in a scene with a strong contrast and a saturated area during the exposure period. Figure 9 shows the result of the HDR image reconstruction simulation from these intermediate images by using Eq. (3). Now, the reconstructed image is subjected to gamma correction to facilitate the confirmation of the result. As shown in Fig. 8(c), the high-illuminance part is saturated in the long-exposure-time image in the scene with a sharp contrast. On the other hand, as shown in Fig. 8(a), in the short-exposure-time image, there is underexposure in the low-illumination area. However, in the reconstructed image, saturation and underexposure are reduced by using the characteristics of both the short-exposure-time and long-exposure-time images. The effectiveness of HDR image



(a) Reference image

(b) Low gradation image
(4 bits, 128th intermediate image)

(c) Reconstruction image

Fig. 7 Simulation result (non-saturation).

(a) 16th (b) 64th (c) 128th

Fig. 8 Intermediate images (4bit).

Fig. 9 Simulation result (HDR reconstruction, Gamma = 0.2).

reconstruction is thus confirmed.

In Fig. 9, the black squares of the checkerboard pattern, which are particularly low-illuminance areas, appear to be suffering from "white defects". In order to make the results of HDR reconstruction easier to understand, we applied gamma correction. As a result, insufficient gray scale in the low-illuminance region appears in the reconstructed image as a pseudo-contour. On the other hand, because each intermediate image as shown in Fig. 8(c) is quantized to 4bit gradation, it looks like there are no defects in the image. Because the gradation of the accumulated intermediate image of the proposed method is 4 bits, it is difficult to reproduce the gradation in the low-luminance region that causes blackout in the intermediate images by the simple method reported in this paper. Conventional HDR method using several high-gradation images with different exposure times is less likely to have this problem because the low-illuminance areas are reconstructed from the long-exposure images.

5. Conclusion and Future Work

In this paper, we proposed an image sensor with a pixel-parallel ADC to readout intermediate images. In addition, the resolution of the pixel-parallel ADC was lowered to reduce the pixel size, but we proposed to acquire a high-gradation image with a reconstruction method using multiple low-gradation intermediate images. Furthermore, we confirmed the effectiveness of the reconstruction method through simulation. In future studies, we plan to examine a reconstruction method that takes into account the movement of the subject, fixed pattern noise due to the variation in pixel, dark current noise in floating diffusion and ADC characteristics, an image sensor circuit configuration that is optimal for intermediate image acquisition, and an A/D conversion method. In addition, image sensor prototypes and actual machine evaluations will be discussed.

Acknowledgments

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References

[1] Y. Nitta, Y. Muramatsu, K. Amano, T. Toyama, J. Yamamoto, K. Mishina, A. Suzuki, T. Taura, A. Kato, M. Kikuchi, Y. Yasui, H. Nomura, and N. Fukushima, "High-speed digital double sampling with analog CDS on column parallel ADC architecture for low-noise active pixel sensor," 2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers, San Francisco, pp.2024–2031, IEEE, 2006.

[2] S. Kleinfelder, S. Lim, X. Liu, and A. El Gamal, "A 10000 frames/s CMOS digital pixel sensor," IEEE J. Solid-State Circuits, vol.36, no.12, pp.2049–2059, 2001.

[3] Y. Chen, F. Yuan, and G. Khan, "A 2a-stage memory write scheme for CMOS pulse-width-modulation digital pixel sensors," 2008 51st Midwest Symposium on Circuits and Systems, pp.125–128, IEEE, Aug. 2008.

[4] Y.-F. Yung and A. Bermak, "A digital CMOS imager with pixel level analog-to-digital converter and reconfigurable SRAM/counter," 4th IEEE International Workshop on System-on-Chip for Real-Time Applications, pp.33–36, IEEE Comput. Soc, 2004.

[5] M. Sakakibara, K. Ogawa, S. Sakai, Y. Tochigi, K. Honda, H. Kikuchi, T. Wada, Y. Kamikubo, T. Miura, M. Nakamizo, N. Jyo, R. Hayashibara, S. Miyata, S. Yamamoto, Y. Ota, H. Takahashi, T. Taura, Y. Oike, K. Tatani, T. Ezaki, and T. Hirayama, "A 6.9-μm pixel-pitch back-illuminated global shutter CMOS image sensor with pixel-parallel 14-bit subthreshold ADC," IEEE J. Solid-State

Circuits, vol.53, no.11, pp.3017–3025, 2018.

[6] C. Shoushun, F. Boussaid, and A. Bermak, "Robust intermediate read-out for deep submicron technology CMOS image sensors," IEEE Sensors J., vol.8, no.3, pp.286–294, March 2008.

[7] D. Sugai and T. Hamamoto, "Image emphasis using high-speed intermediate images and design of a test circuit for image sensor," ITE Technical Report, vol.34, no.19, pp.1–4, 2010 (in Japanese).

[8] D. Handoko, S. Kawahito, Y. Tadokoro, and A. Matsuzawa, "A CMOS high-speed non-destructive intermediate image sensor," The Journal of the Institute of Image Information and Television Engineers, vol.55, no.2, pp.264–270, 2001 (in Japanese).

[9] A. El Gamal, "Trends in CMOS image sensor technology and design," Digest. International Electron Devices Meeting, pp.805–808, IEEE, 2002.

[10] S. Kurata, T. Ootaka, Y. Kameda, and T. Hamamoto, "CMOS image sensor with pixel parallel ADC and intermediate image readout for HDR reconstruction," The Tenth International Workshop on Image Media Quality and its Applications, IMQA2020, pp.33–36, 2020.