IEICE TRANS. FUNDAMENTALS, VOL.E105–A, NO.3 MARCH 2022

FOREWORD

Special Section on VLSI Design and CAD Algorithms

On behalf of the Guest Editors, I am pleased to present this special section on VLSI design and CAD algorithms. Although we have been in the coronavirus disease global pandemic since 2020, we know that IT and ICT technology help us to realize the promising New Normal life, and we believe they are supported by now and future semiconductor devices. These special sections aim to provide new VLSI design methodology and CAD algorithms to produce coming semiconductor VLSIs. These special sections help researchers to have the opportunity to get state-of-the-art of work on VLSI design and CAD algorithms.

In this special section, we have received 18 papers. We made thorough reviews, had online paper selection meetings of all editorial committee members, and finally selected 11 papers. These papers are categorized into 5 topics: 1) Device and Circuit Modeling and Analysis, 2) Circuit Design, 3) Physical Level Design, 4) Logic Synthesis, Test and Verification and 5) High-Level Synthesis and System-Level Design. They cover a wide variety of research areas.

On behalf of the guest editorial committee, I would like to express our sincere appreciation to all authors of papers submitted to this special section. I would also like to express my thanks to all members of the guest editorial committee and all reviewers for their work on judging the quality of papers. I should thank Professor Satoshi Komatsu from Tokyo Denki University and Professor Shimpei Sato from Shinshu University for their work as Guest Editors. Thanks are also due to the IEICE headquarters for the support to this special section.

Yoshinori Takeuchi, Guest Editor-in-Chief

Yoshinori Takeuchi *(Senior Member)* received his B.E., M.E., and Dr. Eng. degrees from Tokyo Institute of Technology in 1987, 1989 and 1992, respectively. From 1992 through 1996, he was a research associate of the Department of Engineering, Tokyo University of Agriculture and Technology. From 1996 through 2017, he was an assistant and associate professor with the Osaka University. He was a visiting scholar in University of California, Irvine from 2006 to 2007. From 2018, he is a professor of Department of Electrical and Electronic Engineering at Kindai University. His research interests include System Level Design, VLSI design and VLSI CAD. He is a member of IPSJ, ACM, and SP, CAS, and SSC Society of IEEE.