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PAPER Special Section on Analog Circuit Techniques and Related Topics

Delta-Sigma ADC Based on Switched-Capacitor Integrator with FIR Filter Structure

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SUMMARY This paper presents a novel delta-sigma modulator that uses a switched-capacitor (SC) integrator with the structure of a finite impulse response (FIR) filter in a loop filter configuration. The delta-sigma analog-to-digital converter (ΔΣADC) is used in various conversion systems to enable low-power, high-accuracy conversion using oversampling and noise shaping. Increasing the gain coefficient of the integrator in the loop filter configuration of the ΔΣADC suppresses the quantization noise that occurs in the signal band. However, there is a trade-off relationship between the integrator gain coefficient and system stability. The SC integrator, which contains an FIR filter, can suppress quantization noise in the signal band without requiring an additional operational amplifier. Additionally, it can realize a higher signal-to-quantization noise ratio. In addition, the poles that are added by the FIR filter structure can improve the system's stability. It is also possible to improve the flexibility of the pole placement in the system. Therefore, a noise transfer function that does not contain a large gain peak is realized. This results in a stable system operation. This paper presents the essential design aspects of a ΔΣADC with an FIR filter. Two types of simulation results are examined for the proposed first- and second-order, and these results confirm the effectiveness of the proposed architecture.

key words: *analog-to-digital converter, delta-sigma modulator, finite-impulse response filter, switched-capacitor integrator*

1. Introduction

Recent rapid improvements in complementary metal-oxide-semiconductor (CMOS) device processing technologies have resulted in CMOS devices that provide higher performance with reduced device sizes. The CMOS data converter is an important circuit. An analog-to-digital converter (ADC) can attain several possible architectures, including pipelines, successive approximation registers (SAR), and flash.

A delta-sigma ADC (ΔΣADC) is used in various conversion systems to achieve low-power, high-accuracy conversion using oversampling and noise shaping for audio, sensor, and wireless applications. The ΔΣADC has been implemented using two types of circuit architectures, based on discrete time (DT), and continuous time (CT), for which different integrator architectures are required. The CT type uses a resistor-capacitor (RC) integrator, which allows continuous operation and high-speed processing. The CT-type modulator is therefore often used in communication applications [1]. Commonly, the RC integrator uses a first-order, low-pass filter as an anti-aliasing filter. Therefore, the system can reduce the order of the anti-aliasing filter implemented in the previous stage. However, high-accuracy conversion is difficult when using CT architectures because of the variability of manufacturing errors in the RC filter, excessive loop delays, and characteristic jitter degradation. In contrast, the DT-type modulator can provide conversion with higher precision compared to the CT type. When using a DT-type modulator, it is possible to use an integrator with a switched capacitor (SC), which results in better coefficient matching, and excellent jitter tolerance.

The DT-type modulator is generally used in audio and sensor applications. ΔΣADC performance improvements are being sought in two areas, namely, high precision within a wide operating band, and low-power consumption. Higher-order, higher-oversampling ratios (OSRs), and multibit techniques, have been mainly proposed for the high-precision and broadband improvements. For example, double sampling and a time-interleaved structure have been used alternately in the integral operation of an operational amplifier (OPAMP), where each path is operated in parallel to increase the operating frequency [2], [3]. However, as the numbers of OPAMPs and routes increase, both the circuit area and the power consumption also increase. Additionally, it is necessary to use a compensation circuit to guarantee the level of accuracy pertaining to degradation owing to path mismatches, which ultimately leads to an increased circuit area [4], [5].

The use of higher-order and multibit methods also tends to increase both the circuit size and power consumption. Therefore, there is a trade-off relationship between increased precision and increased circuit speed in regard to power consumption, although various techniques have been proposed to allow reduced power consumption while performance levels are maintained [6], [7]. In addition, second- or third-order modulators are preferred methods in terms of power consumption reduction and maintenance of stability. However, these modulators are less able to modify coefficients, and thus their design flexibility is low. In order to improve SNR and/or signal bandwidth, there is a method that increases an integrator gain. However, this method cannot improve the performance because of stability issue [8]. This method is needed to adjust coefficients for pole placements to stabilize a ΔΣ loop, which degrades noise performance.

In this paper, we propose a SC integrator with the structure of a finite impulse response (FIR) filter in a loop filter configuration. This structure can realize broadband and high-precision performance, a high signal-to-quantization

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noise ratio, and increased integrator gain in the signal band. In addition, it is possible to maintain circuit stability using the degrees-of-freedom of the pole placement in the case of the loop filter configuration with the implementation of the FIR filter. This structure can be implemented using the SCs, and an existing integrator topology. The structure can also be easily verified using system simulations implemented in MATLAB/Simulink. The proposed method also uses a feed-forward delta-sigma ADC (FFΔΣADC) to improve circuit stability that is expected to simplify the feedback path [9].

Section 2 outlines the circuit performance achieved when using the conventional, increased-integrator-gain coefficient, the stability issue caused by moving the poles, and the nonlinearity effect owing to the amplitude limitation of the quantizer. Section 3 presents the structure and characteristics of the proposed method. A stability of proposed system with FIR filter to increase an integrator coefficient is discussed. And a novel design methodology to realize improving SNR and stability without increasing an order of ΔΣ modulator is explained in this section. Section 4 presents the simulation results for the proposed system and exemplifies the problems encountered in the actual circuit implementation as a combination of an offset effect and capacitor mismatch errors. Finally, we present our conclusions.

2. Increased Integrator Gain Coefficient and Stability

2.1 SNR Impact for Increased Integrator Gain and Issue of Pole Root Locus

An increased integrator gain coefficient is desirable to suppress quantization noise in the signal band [8]. The effects of an increased integrator gain coefficient on the typical second-order FFΔΣADC are described herein as an example, as shown in Fig. 1.

The transfer function of the second-order FFΔΣADC is as follows,

$$STF(z) = 1 \tag{1}$$

$$NTF(z) = \frac{(1 - z^{-1})^2}{1 - 2(1 - a)z^{-1} + (1 + ab - 2a)z^{-2}} \tag{2}$$

The noise transfer function (NTF) equation shows that it is possible to increase the coefficients a and b, and to reduce the noise floor in the signal band. Figure 2 compares the fast Fourier transform (FFT) spectra obtained from the normal- and high-gain systems. The simulation uses −6 dB of input and a 4-bit quantizer, not includes amplitude limitation of quantizer.

This figure shows that the quantization noise is reduced at low frequencies when the integrator gain coefficient is increased, in the case where $a = 1.8$ and $b = 1.8$. Figure 3 elicits an almost linear characteristic for the response of the signal-to-noise ratio (SNR) of a conventional second-order FFΔΣADC and the integrator's gain as the product of a and b. An improved SNR is elicited that is almost equivalent to the increased integrator gain coefficient.

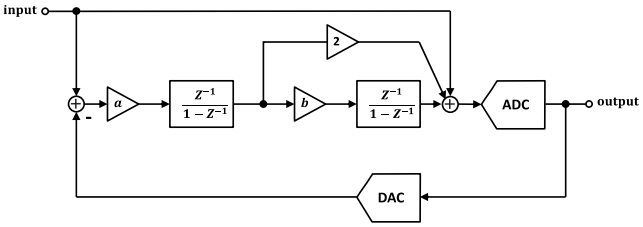


Fig. 1 Conventional second-order FFΔΣADC structure.

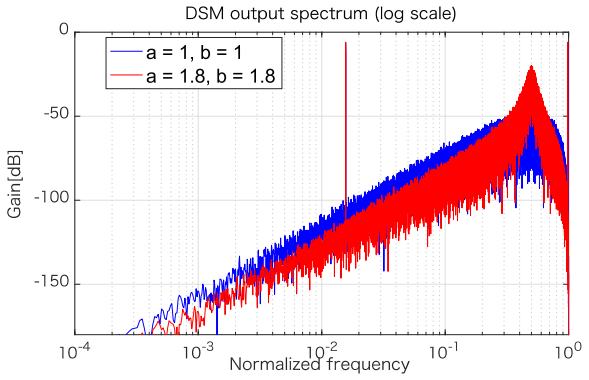


Fig. 2 Comparison of FFT spectra of normal- and high-gain systems.

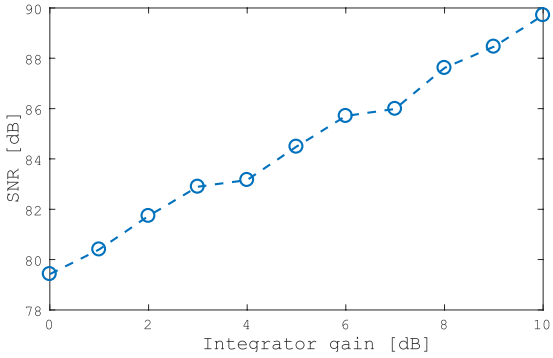


Fig. 3 SNR response as a function of integrator gain for the system depicted in Fig. 1.

However, there is an unstable peak near the Nyquist frequency, as shown in Fig. 2. Therefore, the system may become unstable when the integrator gain coefficient is too high. Figure 4 shows the pole root loci when the coefficients a and b of the integrator gain increase. The poles move towards −1 when the coefficients a and b of the integrators increase. We can see that the system remains stable until both a and b become equal to 2 on the pole plot.

2.2 Influence of Nonlinearity owing to Amplitude Limitation of Quantizer

However, we cannot assess the system's stability based on pole placement alone. Figure 5 shows the distributions of the input and output of the two integrators and the quantizer without saturation, shown in Fig. 1, when coefficients a and

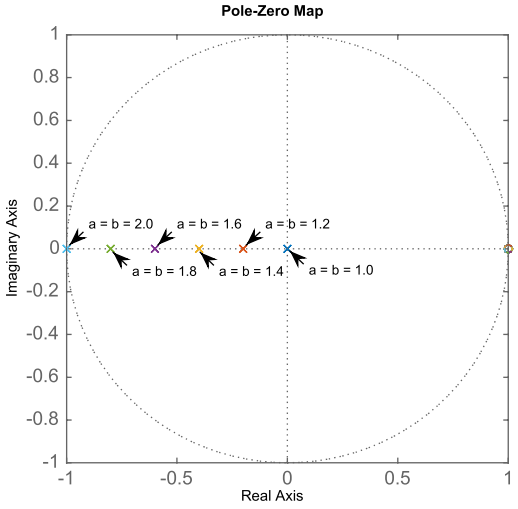


Fig. 4 Zero-pole plot of second-order FFΔΣADC with high gain.

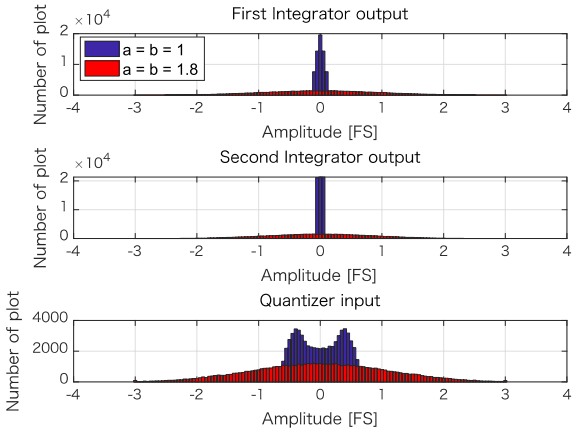


Fig. 5 Comparison of output distributions for both integrators and input of quantizer shown in Fig. 1.

b are both equal to 1.8. The maximum output amplitude is greater than 3.5. The simulation condition is same as Fig. 2. In case of the full-scale (FS) amplitude is defined in the range of 1 to −1, output signal amplitudes larger than ±1 are clipped at the integrator output. Clipping also occurs at the quantizer input when the signal amplitude exceeds the supply voltage range of the specific circuit's architecture. When it's added a saturator of 1 to −1 on each of the input and output of the two integrators and the quantizer, the system becomes unstable caused by a reduction of clipped feedback signal as shown in Fig. 6. The simulation condition is same as Fig. 2.

The system stability thus requires consideration of the pole placement, and consideration of the amplitude ranges of the integrator and the quantizer. This prevents system oscillation that is induced by the nonlinearity of the quantizer. The results show that reducing the noise floor in the signal band owing to the increased integrator gain coefficient imposes a trade-off relationship with stability.

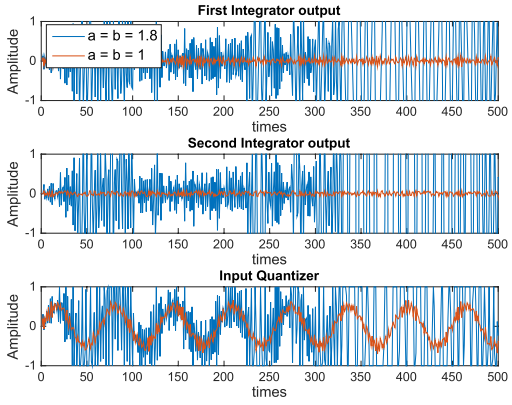


Fig. 6 Comparison of waveform for both integrators and input of quantizer with amplitude saturation for the system depicted in Fig. 1.

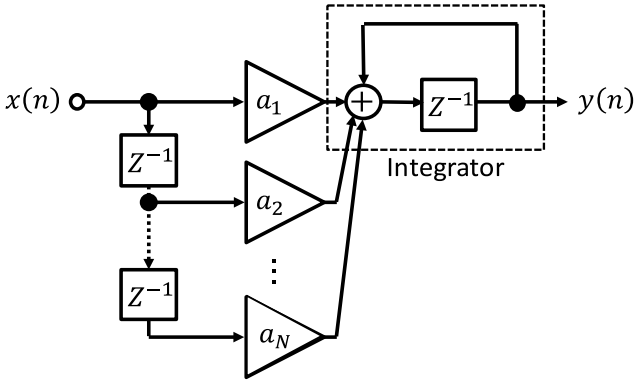


Fig. 7 Block diagram of the FIR filter structure.

3. Proposed Modulator Structure with FIR Filter Integrator

In this section, we propose a method to improve the integrator gain in the signal band, while maintaining stability using a SC integrator with the FIR filter structure.

3.1 Integrator using SC Circuits for Implementation of FIR Filter Structure

The architecture of the FIR filter system is shown in Fig. 7. The FIR filter is a discrete type of filter that consists of $N-1$ delay units, gain paths, and an adder at each integrator. The $N-1$ delay and gain are easily constructed using a parallel SC circuit. An adder circuit is used in the same way as a normal integrator [10].

The transfer function of the system block is defined in accordance to

$$\frac{y(n)}{x(n)} = \left(a_1 + a_2 z^{-1} + \cdots + a_N z^{-(N-1)}\right) \frac{z^{-1}}{1 - z^{-1}} \quad (3)$$

The FIR filter structure increases the number of zeros of the loop filter configuration, and its coefficient gain as the sum of a1, a2 and a3 around direct current (DC). The upper part

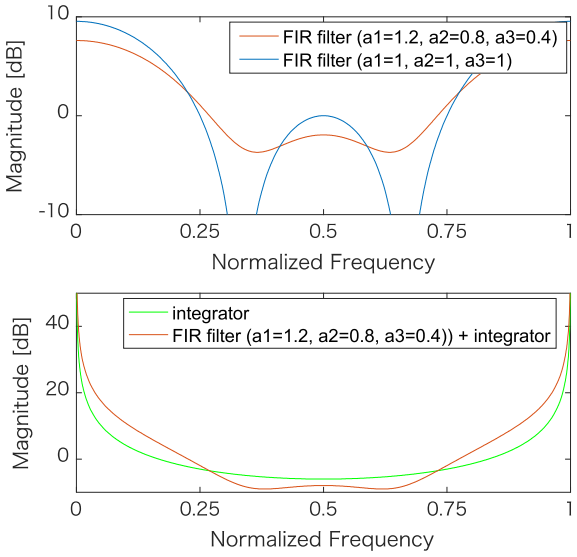


Fig. 8 Frequency characteristics of the FIR filter, the integrator, and their combinations.

of Fig. 8 shows the frequency characteristics of the three-tap, FIR filter structure.

Integrators containing this FIR filter can achieve any pole arrangement required by a modulator to adjust the gain coefficients for each path. In the case where a filter has been inserted into the system, several poles can be used to maintain stability by adjusting the pole placement of the ΔΣ modulator loop, thereby changing the gain coefficient.

The lower part of Fig. 8 shows the frequency characteristics of the integrator, and the corresponding characteristics of the combination of the FIR and the integrator. We can realize increased gains in the signal band until around 0.25 fs, and a stability that reduces the high-frequency and increases the low-frequency gains of the FIR filter. The integrator that uses the FIR filter can thus realize improved gain in the signal band.

Next, we show the implementation of the FIR filter circuit structure using a SC circuit. Figure 9(a) and (b) show the circuit structure and the clock timing, respectively, for a three-tap FIR filter, and an integrator.

An N-delay block is realized using 2(N + 1) clocks and (N + 1) SC circuits. One delay is realized using two SC circuits to charge their timings simultaneously. This delay is applied immediately to the integrator, in association with the temporal responses from each of the SC circuits. In this way, an FIR filter structure circuit is achieved without increasing additional OPAMP.

3.2 Design Essentials for Pole Placements

In this section, we introduce the design method for FFΔΣADC using the FIR filter-based SC integrator structure.

1. To increase the integrator gain coefficient in the signal band and reduce the noise floor to achieve the target SNR, the gain of the FIR filter in the signal band is determined as shown in Fig. 3. The gain of the FIR filter of signal band $G_b = G_{snr}$, where G_{snr} is the value of required SNR improvement
2. As the number of taps increases, the number of poles of the modulator also increases. The number of taps of the FIR filter will determine the target signal bandwidth. If the poles nearest to the signal band approach the outer edge of the unit circle, a steep noise floor curve may narrow the signal bandwidth. For example, a five-tap FIR filter reduces the noise floor to approximately for

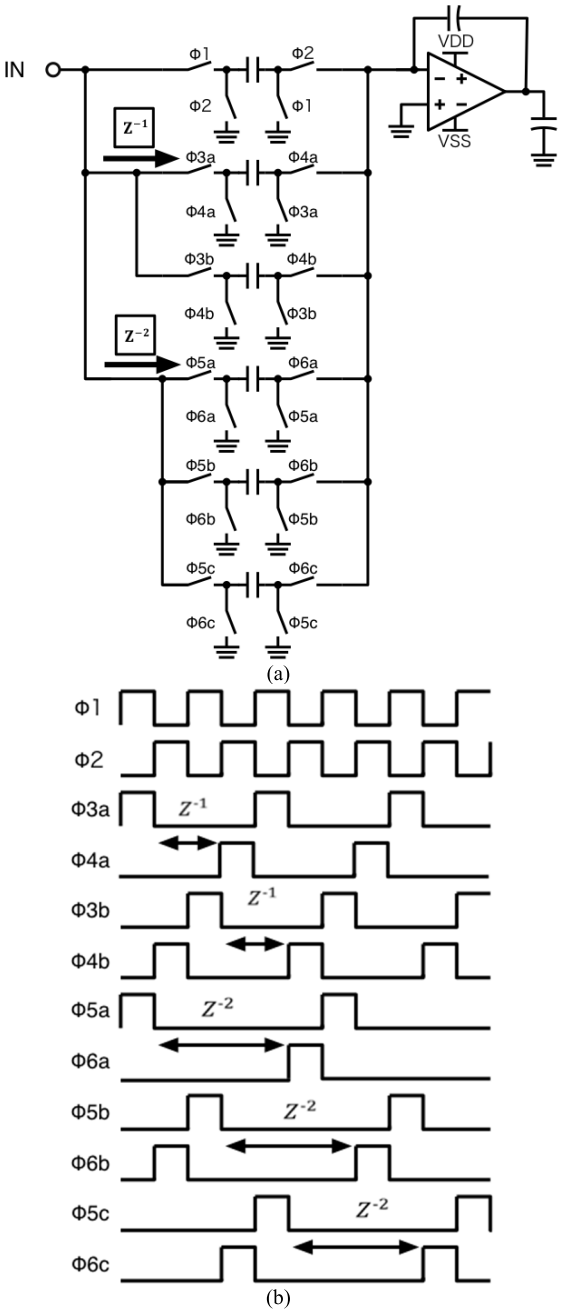


Fig. 9 (a) Circuit structure, and (b) clock timing of a three-tap FIR filter implemented with SC circuits.

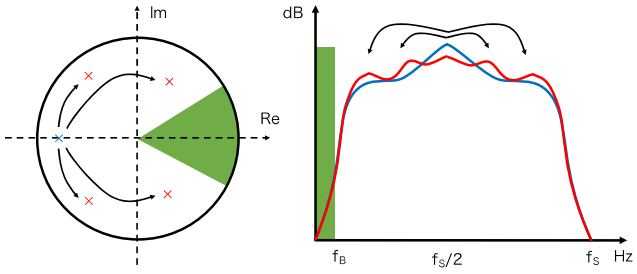


Fig. 10 Example of pole placement for five-tap FIR filters.

the bandwidth of one-tenth sampling frequency (0.1 fs). The nearest pole is placed on the inner side of the unit circle, thereby maintaining the signal bandwidth

3. The taps of the FIR filter should be set to maintain a distance between each of the poles for the system shown in Fig. 10. Blue mark and line are Example of pole placement without the FIR filter, Red one are with the FIR filter. This is because it is essential to prevent the increased amplitudes caused by the cluster of the modulator's poles. When the pole of the system made by the FIR filter is relocated to adjust the gain coefficient, both the pole placement and the amplitude of the output integrator and input quantizer should be confirmed using MATLAB/Simulink simulations

In summary, the FFΔΣADC that uses an FIR filter should be designed with the following three points in mind:

- The poles near the outer edge of the modulator need to be allocated to maintain a distance between each of the poles
- Increasing the integrator's gain using an FIR filter should be implemented with care both in terms of the pole placement, and the amplitude of the output integrator and input quantizer
- The pole of the system introduced by the FIR filter should be located so that it keeps the poles of the modulator outside the signal band

The next section shows first and second-order FFΔΣADCs using the FIR filter structure with MATLAB/Simulink models. These systems were designed in accordance to the design principles listed above.

4. Simulations

In this section, we describe the results of simulations of the proposed circuit performed using MATLAB/Simulink.

4.1 First-Order FFΔΣADC with a Three-Tap FIR Filter

Figure 11 shows a first-order FFΔΣADC with the inserted FIR filter structure. The transfer function of the system shown in Fig. 11 is as follows:

$$STF(z) = 1 \tag{4}$$

$$NTF(z) = \frac{1 - z^{-1}}{1 - (1 - a_1)\, z^{-1} + a_2 z^{-2} + a_3 z^{-3}} \tag{5}$$

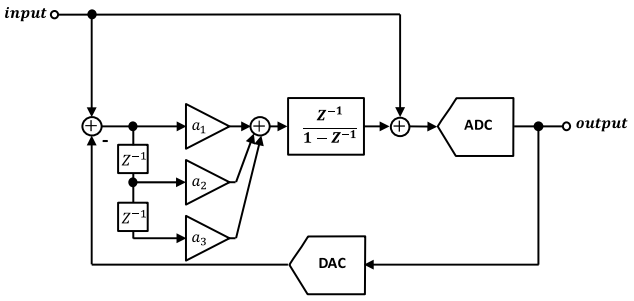


Fig. 11 Structure of first-order FFΔΣADC with FIR filter.

Table 1 FIR filter coefficients for second-order FFDSM.

Coefficient	a_1	a_2	a_3	Integrator gain
FIR Filter1	1.4	0.7	0.4	7.96 dB

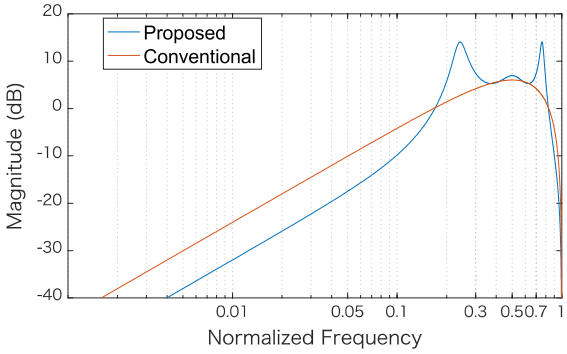


Fig. 12 Comparison of Bode plots of proposed first-order FFΔΣADC and conventional systems.

There are several terms on the denominator of (5), indicating that the poles of the modulator can be moved from their initial locations near half of sampling frequency (fs/2) to any desired frequency as shown in Fig. 10. The system is more stable in the first-order case than in the case where higher gain modulators are used. We can also set high-gain integrator values. The simulations used the coefficients listed in Table 1.

Figure 12 shows a comparison of the NTF bode plot of the first-order FFΔΣADC with the FIR filter and a conventional system, while Fig. 13 shows a zero-pole plot of the proposed FFΔΣADC. The figures indicate that the proposed system has a lower noise floor than the conventional system, and that all the poles are contained in a unit circle. The proposed system's noise floor curve defined in the vicinity of the signal bandwidth is lower than that of the conventional system. Thus, the system achieves a high SNR.

Figure 14 shows the FFT spectra of the proposed and conventional structures. The simulation conditions are listed in Table 2. Table 3 shows an SNR comparison of for the conventional and the proposed first-order FFΔΣADCs. The noise floor is not clear caused by tones, but the proposed system achieves an SNR increase of 7.8 dB that is almost equal to the gain increase of this system compared to the gain of the conventional system.

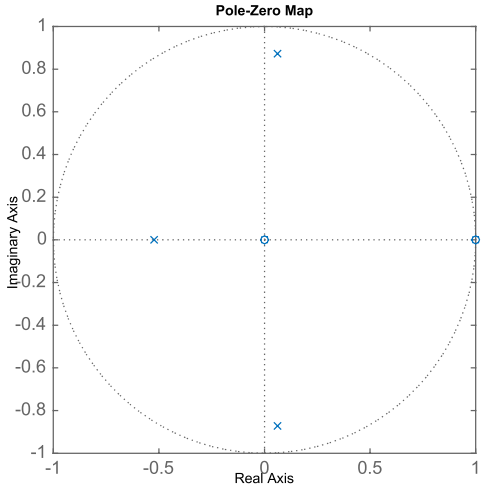


Fig. 13 Zero-pole plot of first-order FFΔΣADC with FIR filter.

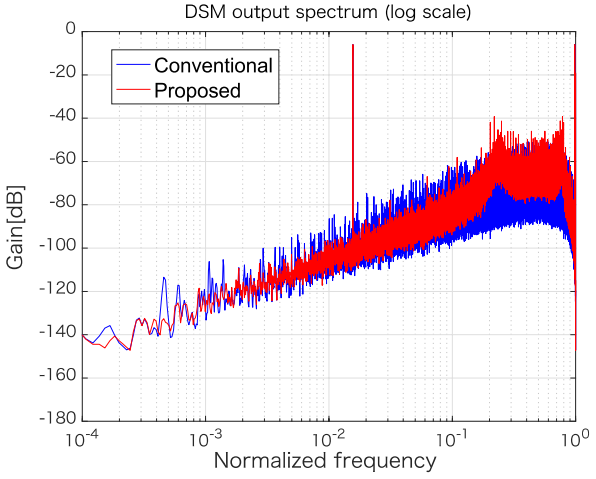


Fig. 14 Comparison of FFT spectra of proposed first-order FFΔΣADC and conventional system.

Table 2 Simulation conditions.

Input	T_S	OSR	Quantizer bits	Number of plots
−6 dBFS	1	32	4	2^{16}

Table 3 Comparison of SNR of first-order FFΔΣADC systems.

	SNR
Proposed system	66.6 dB
Conventional system	58.8 dB

4.2 Second-Order FFΔΣADC with Two Three-Tap FIR Filters

Figure 15 shows the second-order FFΔΣADC with the two FIR filter structures inserted into each of the integrators. The transfer function of the system is,

$$STF(z) = 1 \tag{6}$$

$$NTF(z) =$$

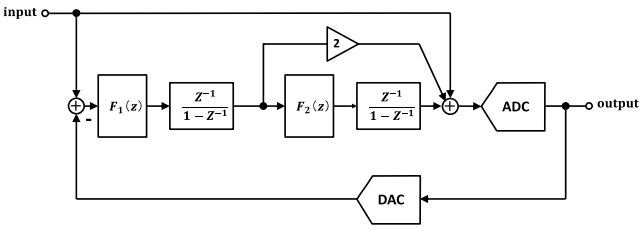


Fig. 15 Structure of second-order FFΔΣADC with FIR filter.

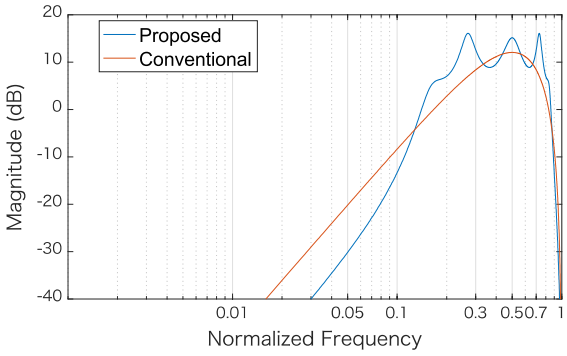


Fig. 16 Comparison of Bode plots of proposed and conventional second-order FFΔΣADC systems.

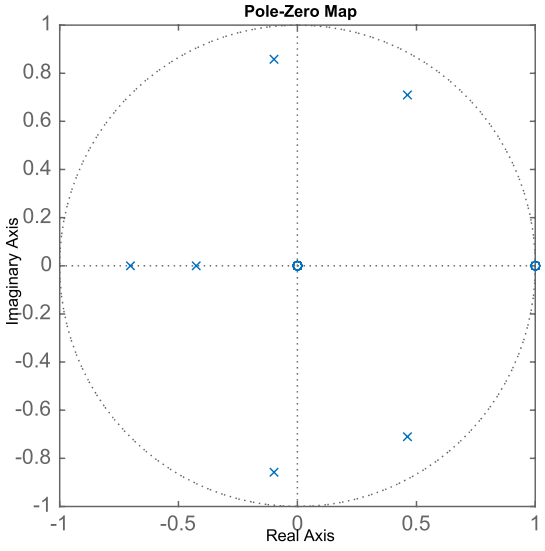


Fig. 17 Zero-pole plot of second-order FFΔΣADC using two FIR filters.

$$\frac{\left(1-z^{-1}\right)^2}{1-2\left(1-F_1(z)\right)z^{-1}+\left(1+F_1(z)F_2(z)-2F_1(z)\right)z^{-2}} \tag{7}$$

$$F_1(z) = a_1 + a_2 z^{-1} + a_3 z^{-2} \tag{8}$$

$$F_2(z) = b_1 + b_2 z^{-1} + b_3 z^{-2} \tag{9}$$

The frequency responses and the zero-pole arrangement are obtained as respectively shown in Figs. 16 and 17, based on the coefficients that are listed in Table 4. Note that the added poles are far from other poles. The nearest pole for the signal band is placed on the inner side of the unit circle.

Table 4 FIR filter coefficients for second-order FFDSM.

Coefficient	a_1	a_2	a_3	Integrator gain
FIR filter1	1.4	0.7	0.4	7.96 dB
	b_1	b_2	b_3	
FIR filter2	0.8	0.5	0.4	4.6 dB

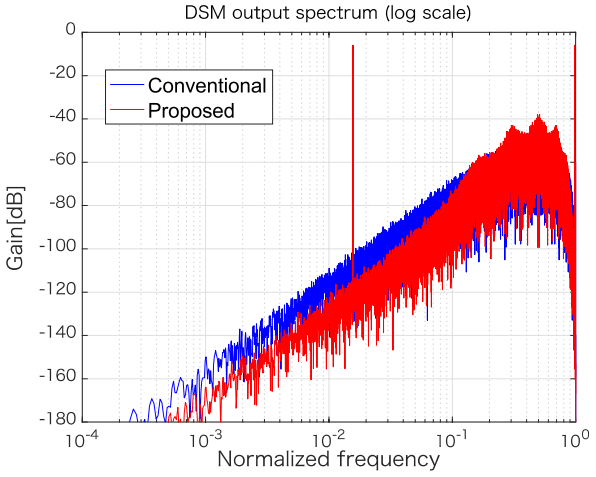


Fig. 18 Comparison of FFT spectra of proposed and conventional systems.

Table 5 Comparison of SNR responses of second-order FFΔΣADC systems.

	SNR
Proposed system	91.8 dB
Conventional system	79.6 dB

Figure 18 shows the FFT spectra of the proposed and conventional structures obtained using the simulation conditions listed in Table 2. Table 5 shows a comparison of the SNR responses of the conventional and proposed second-order FFΔΣADCs. When the FIR filter is used, the quantization noise in the signal band is reduced, and the SNR is improved by 12.2 dB. This improvement is considered to be almost equivalent to the increased integrator gain coefficient shown in the signal band.

4.3 Stability of FIR Filter Structure

Next, we confirm the influence of amplitude limitations of the proposed second-order FFΔΣADC systems. The output amplitude ranges of the integrator and the quantizer at an input of −6 dBFS are shown in Fig. 19. The full-scale amplitude is defined in the range of 1 to −1 as Fig. 5. The output amplitude of the proposed system increases slightly over that of the conventional system, but maintains the stability of the system.

As seen from the quantizer's amplitude in Fig. 19, this system is limited owing to the degradation in SNR that depends on the offset of the quantizer's input. The SNR response as a function of the quantizer offset for the modulator of the proposed system on MATLAB/Simulink simulation is shown in Fig. 20. The proposed system achieves to maintain ±2 dB SNDR performance for quantizer offsets in the

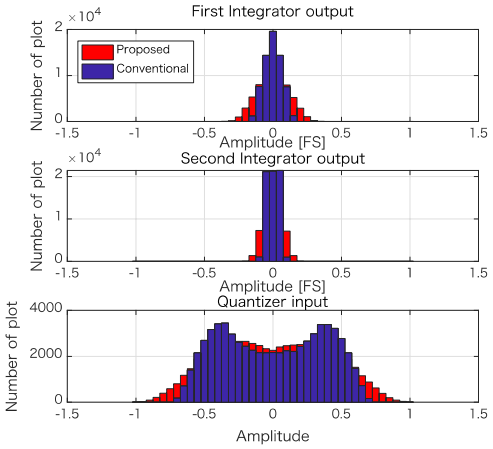


Fig. 19 Comparison of output distributions for both integrators and input of ADC shown in Fig. 15.

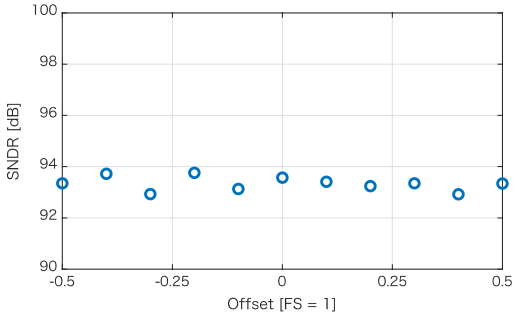
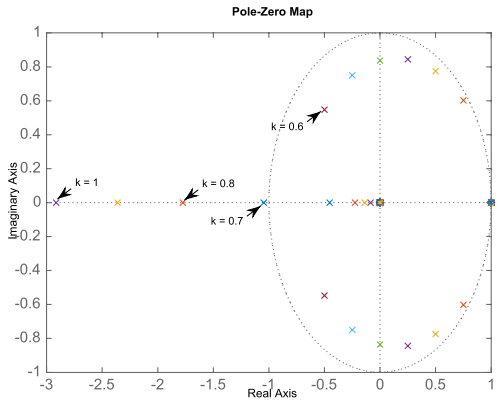


Fig. 20 SNDR response of proposed system as a function of the quantizer offset.

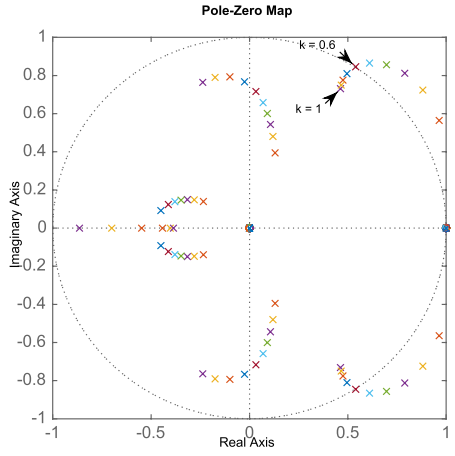
range of −0.5 and 0.5. Because quantizer offset influence is suppressed by the second integrator in the closed loop. The second integrator is acceptable the influence because it has ±0.7 margin for the range of output signal amplitude. These results justify the robustness of the proposed system for these influences.

Next, we discuss the stability of the proposed architecture using a linear model assuming that the gain of the internal ADC (quantizer) is k. It is a common method to confirm the nonlinearity effects of the quantizer using linear models [11]. If the input of the ADC exceeds the maximum range of ADC, the gain of ADC, k, looks like decreased. Herein, the inner parts of the ADC in Figure 1 and 15 are modeled using quantization and a gain value that is equal to k.

Therefore, $v = k\,y + q$, where v, y, and q, are the input of the ADC, the output of the ADC, and the quantization noise, respectively. By drawing the loci of these roots for $0 < k < 1$, the stability of the system can be predicted. If the input amplitude of the ADC is higher than the maximum amplitude of the ADC, k effectively decreases from 1 to 0. Figure 21(a) and (b) show the loci of the roots for NTF (2) and (7), respectively. The values of a and b of (2) are 2.5 and 1.7, which are the same DC gains as those for the FIR filter shown in Table 4. The root is already outside the unit



(a)



(b)

Fig. 21 (a) Root loci of conventional NTF, and (b) proposed NTF systems.

circle, even when $k = 1$, as shown in Fig. 21(a). By contrast, the root is kept inside the unit circle but moves outside for $k < 0.6$, as shown in Fig. 21(b). Thus, the proposed system improves the stability of the overall system, compared to systems without the use of FIR filter structures, even if the integrator gain coefficients are increased.

4.4 Effects of Capacitor Mismatch Error on Transfer Function

The coefficients of the FIR filter consisted of SC circuits depend on capacitor mismatch errors. The effects of the mismatches related to manufacturing variations can cause serious problems in the case of a wideband ΔΣADC, such as the type that uses double sampling and a time-interleaved function [4], [5]. Figure 22 shows the zero-pole diagram elicited from the Monte Carlo simulations obtained by adding a path-gain mismatch within the range of ±5% to the FIR filter.

Commonly, the relative mismatch of the capacitor is estimated to be approximately less than 1%. However, all

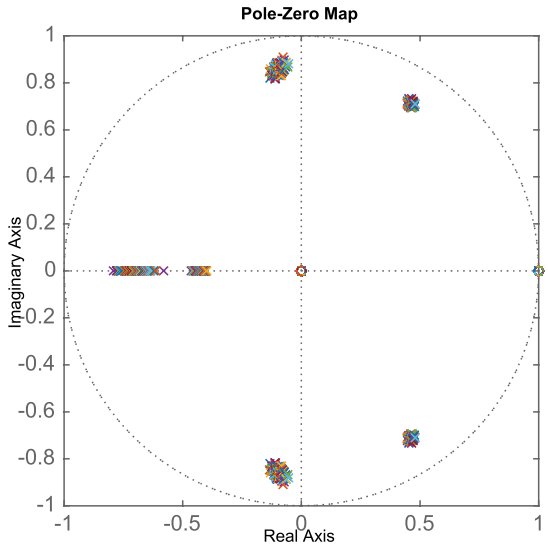


Fig. 22 Monte Carlo simulation results obtained by adding a path-gain mismatch within the range of ±5% to the FIR filter.

poles of the proposed architecture fell within the unit circle in the simulation. The proposed circuit is thus barely affected.

5. Conclusion

We proposed a design method for a ΔΣADC based on the use of an FIR filter into the integrator in the loop filter configuration. The system has an improved SNR that is almost equivalent to the increased integrator gain coefficient, yet maintains system stability. The proposed circuit can be adapted for both wideband and high-precision performance by varying the pole assignments. The stability of the proposed system was discussed on pole plot locus and limitation amplitude. The effects of the proposed design method were demonstrated using MATLAB/Simulink simulations. Manufacturing variations, which represent a problem in actual circuit implementation, did not significantly affect the performance. This was confirmed by the simulation results. Specific mismatch compensations, such as those described in [2] and [5], are not required in this case. The proposed method can be implemented by adding a simple circuit to the conventional SC circuit of the ΔΣADC.

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