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Low-Voltage Wireless Analog CMOS Circuits toward 0.5 V Operation

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SUMMARY This paper introduces several techniques for achieving RF and analog CMOS circuits for wireless communication systems under ultra-low-voltage supply, such as 0.5 V. Forward body biasing and inverter-based circuit techniques were applied in the design of a feedforward Δ - Σ A/D modulator operating with a 0.5 V supply. Transformer utilization is also presented as an inductor area reduction technique. In addition, application of stochastic resonance to A/D conversion is discussed as a future technology.

key words: analog, RF, CMOS, forward body biasing, transformer, stochastic resonance

1. Introduction

Wireless integrated transceivers based on RF-CMOS technology have advantages of scalability and performance (f_T and NF). The International Technology Roadmap for Semiconductors (ITRS) [1] predicts that the supply voltages of low-power digital circuits will decrease to 0.5 V in the near future. Considering the integration of RF and analog circuits with digital circuits, the development of receiver circuits operating at such a low supply voltage will be required.

However, with such a low voltage supply, degradation in performance due to non-idealities of the analog building blocks becomes a serious problem, especially for IF amplifier and A/D converters. For example, integrators of Δ - Σ A/D modulators with a supply voltage close to V_{TH} may force the transistors to operate in weak inversion, thereby inducing poor accuracy and low operation speed. At the same time, a low supply voltage also limits the integrator output swing, thereby degrading the performance of the A/D modulator.

Apart from low-voltage operation, the continuous scaling of CMOS technologies has imposed another challenge on CMOS radio-frequency integrated circuits (RFICs); a small chip area [2], [3]. Under the integration of RF circuits with digital circuits in advanced CMOS technologies, the development of low-voltage and small-area (low-cost) RF circuits is required. Although digital RF circuit design methodologies can help contribute to a solution [2], [3], analog-centric circuits still remain.

Even using a matured CMOS process, low-voltage operation RF and analog circuits are important and attract

some interest, especially in wireless sensor applications with requirements of long battery life time.

This paper introduces some techniques to achieve low-voltage operation such as 0.5 V. Sections 2 and 3 describe forward body biasing and inverter-based circuit techniques. These techniques were applied in design of a feedforward Δ - Σ A/D modulator operating at 0.5 V supply, as described in Sect. 4. Transformer utilization is also demonstrated as an inductor area reduction technique in Sect. 5. Section 6 outlines predictions of stochastic resonance application to future signal detection and A/D conversion techniques based on numerical simulations.

2. Forward Body Biasing Technique

For logic circuits and SRAM operating at ultra-low voltage (≤ 0.6 V), dynamic-threshold (DT)-MOS [4]–[6] and active-body-biasing techniques [7] have already been proposed. These techniques utilize the forward body bias effect with tied gate and body to realize a device with a low V_{TH} at the on-state with low off-state leakage current. Forward body biasing has other advantages, such as (1) reduction of the short channel effect [6] and (2) reduction of the V_{TH} mismatch due to random dopant fluctuations [7]. Focusing on the latter, the standard deviation of V_{TH} , $\sigma_{V_{TH}}$, among MOS devices with the same gate length L and width W on the same chip is expressed as [8]–[10]

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{LW}}, \quad (1)$$

where $A_{V_{TH}}$ is constant, depending on the process technology and body bias. Therefore, device scaling deteriorates matching, which is important in analog circuit design [11]. Under careful consideration, Eq. (1) is expected to be applied to estimate the V_{TH} mismatch, even in advanced structures of MOS devices, such as fully-depleted silicon-on-insulator (FD-SOI) devices [12]. This issue is essential in device scaling. Forward body biasing can reduce $A_{V_{TH}}$ through a decrease of the depletion layer width.

Forward body biasing is also useful to compensate device characteristic variations due to process and temperature. Figure 1 shows a simple implementation for 0.5 V logic circuits [13]. The temperature-variation compensation circuit compensates the threshold voltage of PMOS through its body. The logic-threshold correction circuit assures a balance between the drivability of the PMOS and NMOS de-

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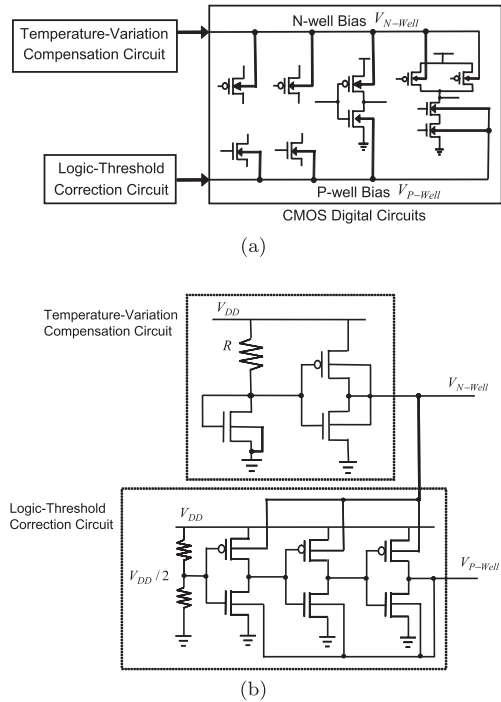


Fig. 1 (a) Compensation of device characteristic variations with forward body biasing, and (b) corresponding control circuits.

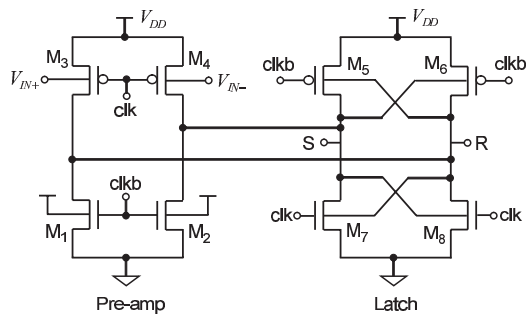


Fig. 2 A body-input gate-clocked comparator.

vices by monitoring the logic threshold voltage of a replica inverter.

For dynamic operation with a body terminal, the body resistance and parasitic capacitances [6] must be considered. The time constant related to the body is generally larger than that of the gate electrode. When signals applied to the gate and body are different, the lower-frequency signal can be selected to apply to the body in terms of speed. Note that the forward body biasing technique requires a triple-well CMOS structure. Latch-up in the circuit is avoided, because a 0.5 V supply cannot switch on the emitter-base junction of parasitic bipolar transistors.

A body-input gate-clocked comparator has been proposed, which employs body terminals of transistors for signal input (lower-frequency) while the gate terminals are used for clock input (higher-frequency) [14], [15]. Figure 2 shows that the comparator consists of pre-amp and latch stages, operating when the clock is ‘LOW’ and ‘HIGH’, re-

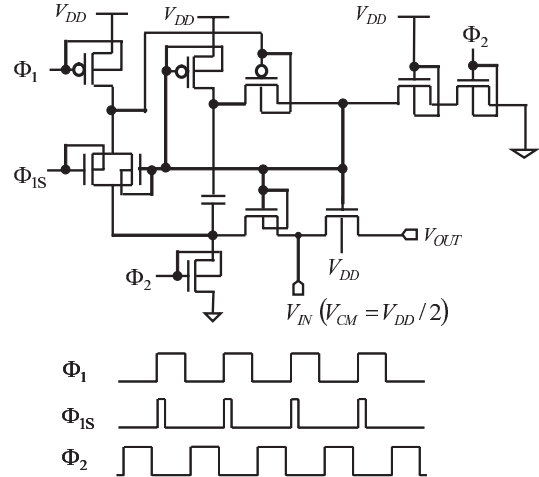


Fig. 3 Boot-strapped single NMOS switch with a local charge pump circuit.

spectively. The differential input signal with the common-mode level of V_{CM} is amplified by the body transconductance of the input PMOS transistors, and then latched by the following stage, which consists of two cross-coupled body-input inverters. Note that the body terminals of the NMOS transistors in the pre-amp are forward biased to ensure rapid on-state operation of the NMOS side in our work [15].

A signal with common-mode level at $V_{DD}/2$ is not sufficient to turn on a transistor switch with a 0.5 V supply. An effective solution is to employ a voltage higher (in the case of NMOS) than the supply with a charge pump to control the switch transistor gate. Figure 3 shows a boot-strapped single NMOS switch with a local charge pump circuit [15]. This boot-strapping circuit is fundamentally similar to previously proposed one [16] except for the forward body biasing. This allows rail-to-rail switch operation while limiting all gate-source and body-source voltages, and avoids any overstress in the gate oxide and body-source junction. Clock Φ_{IS} only gives sampling trigger at the beginning of Φ_1 .

3. Inverter-Based Circuit Topology

To develop a high-performance analog circuit with the condition of V_{DD} close to V_{TH} , such as for a 0.5 V supply, the advantages of the CMOS inverter’s high transconductance and good compatibility with digital circuits can be utilized. However, for a 0.5 V supply, the DC common-mode voltage is set to 250 mV and may cause weak inversion operation of the CMOS transistors for a typical transistor threshold voltage V_{TH} of approximately 450 mV. In order to achieve high performance transistor operation, techniques such as level shifting with a floating voltage source (FVS) [17], [18] are used to increase the gate-source voltage, thus achieving higher performance of analog circuits.

Figure 4 shows the proposed inverter-based operational amplifier (op-amp) used for switched-capacitor applications [15]. The proposed circuit is based on a previously proposed CMOS amplifier [19]. The op-amp mainly consists

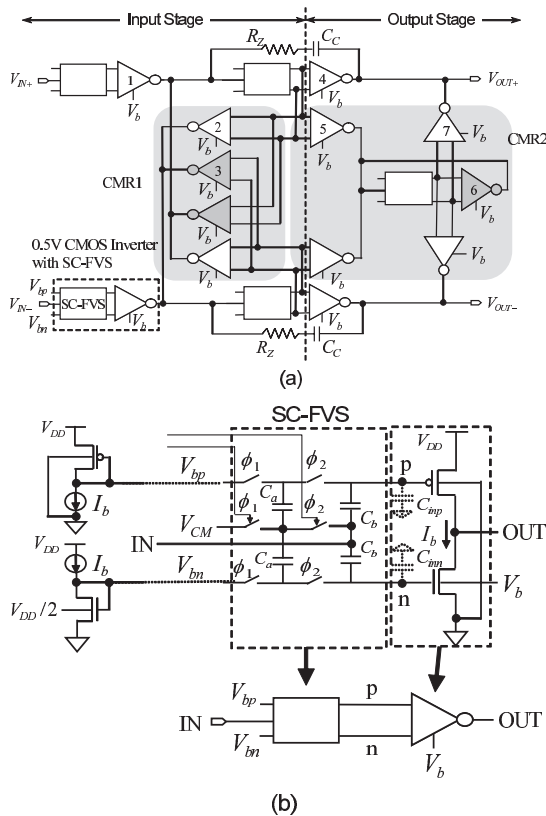


Fig. 4 (a) Inverter-based op-amp and (b) inverter with SC-FVS circuit.

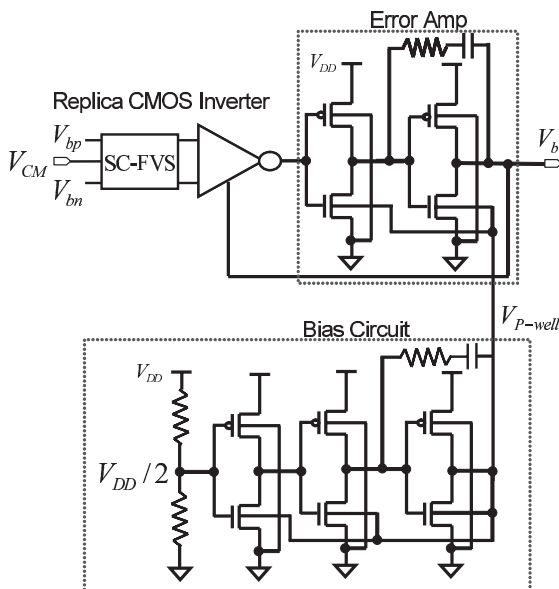


Fig. 5 Common-mode voltage adjustment circuit.

of four 0.5 V CMOS inverters with switched-capacitor floating voltage sources (SC-FVS), and two common-mode rejection circuits denoted CMR1 and CMR2 [20]. SC-FVS circuits are used to increase the gate-source voltage of the PMOS and NMOS transistors, while the two common-mode rejection circuits CMR1 and CMR2 increase the common-

mode rejection ratio (CMRR) and stabilize the DC output common-mode level. Given the total transconductance and output impedance of each inverter (1~7) $g_{m1\sim7}$ and $r_{o1\sim7}$, respectively, the differential DC gain is given by

$$Gain = \frac{g_{m1}g_{m4}(r_{o4}/r_{o7})}{1/(r_{o1}/r_{o2}) - (g_{m2} - g_{m3})}. \quad (2)$$

Inverters 4 and 7 with the same size ($g_{m4} = g_{m7}$) are used. The CMRR is represented by

$$CMRR = \frac{1/r_{o1} + g_{m2} + g_{m3}}{1/(r_{o1}/r_{o2}) - (g_{m2} - g_{m3})} \times \frac{1/r_{o5} + g_{m6}}{1/r_{o5} - (g_{m5} - g_{m6})}. \quad (3)$$

Equations (2) and (3) show that the DC gain and CMRR can be enhanced by slight changes in the size ratios of inverters 2 and 3, and inverters 5 and 6, respectively.

All the bodies of the NMOS transistors in the inverters are forward biased and are employed as common-mode feedback terminals, V_b , to provide accurate control of the DC common-mode output voltage and maintain good independence of process and temperature variations.

Figure 4(b) illustrates the detail of the SC-FVS blocks. The current mirrors provide accurate control of the quiescent current I_b flowing through the inverter [17]. All switches are controlled by nonoverlap clocks ϕ_1 and ϕ_2 . V_{bp} and V_{bn} are set to 0.1 and 0.4 V, respectively, so that there is no bootstrapped switch required at these two paths. The other two switches connected with V_{CM} are added to stabilize the DC common-mode output level, in comparison to the circuit in our previous work [20]. These two switches require clocks with higher levels than V_{DD} to ensure switching operation, and this requirement is met by the bootstrapped clock switches shown in Fig. 3. Each switching cycle refreshes the capacitors C_b , which maintains the voltage difference, $V_{bn} - V_{bp}$, between the inverter input nodes 'n' and 'p.' At the same time, the forward body bias lowers the V_{TH} by approximately 100~150 mV for a 0.18 μm CMOS process. Thus, the transistors operate in the moderate or even strong inversion region ($|V_{GS}| \geq V_{TH}$), even under such a low-voltage supply.

Figure 4(b) shows that a gain degradation of approximately $C_b/(C_b + C_{in})$ is caused by the parasitic capacitances C_{inp} and C_{inn} (assume $C_{inp} = C_{inn} = C_{in}$), which can be reduced by using a large C_b . A large C_b also alleviates the effect of charge injection during switching, but induces an area penalty. Therefore, C_b with a size greater than 5 times that of C_{in} was adopted for the design of the 0.5 V feedforward $\Delta\Sigma$ A/D modulator described in Sect. 4, while keeping the area and gain degradation small.

A replica inverter circuit with SC-FVS and an error amplifier, as reported in previously proposed ones [20], [21] were employed to provide the common-mode feedback voltage V_b in Fig. 4. Figure 5 shows the common-mode voltage adjustment circuit. When NMOS rather than PMOS devices are used for common-mode adjustment, the total sizes of

the MOS devices can be reduced. This technique can accurately set the DC common-mode output voltage to $V_{DD}/2$ with good independence of process and temperature variations, and the PMOS and NMOS transistors need not be carefully sized.

Figure 6 indicates the corner simulation results of the op-amp designed with a $0.18\mu\text{m}$ CMOS process. Under typical conditions (TT, 25°C), the op-amp has an open loop DC gain of 59 dB, a unity gain bandwidth of 42 MHz and a phase margin of 60° with a load of 8 pF. The power consumption is $168\mu\text{W}$. Additionally, the inverter-based op-amp shows excellent common-mode gain characteristics in the high frequency range, in addition to a good figure of merit (FOM; $\eta = (V_{DD} \cdot \text{GBW} \cdot C_L)/\text{Power}$) compared with other conventional 0.5 V op-amps [21].

Such a CMOS-inverter-based approach can also be applied to some RF circuits. The recently developed 5 GHz CMOS voltage-controlled-oscillator(VCO) operating with a 0.5 V supply uses CMOS inverters with capacitive coupling

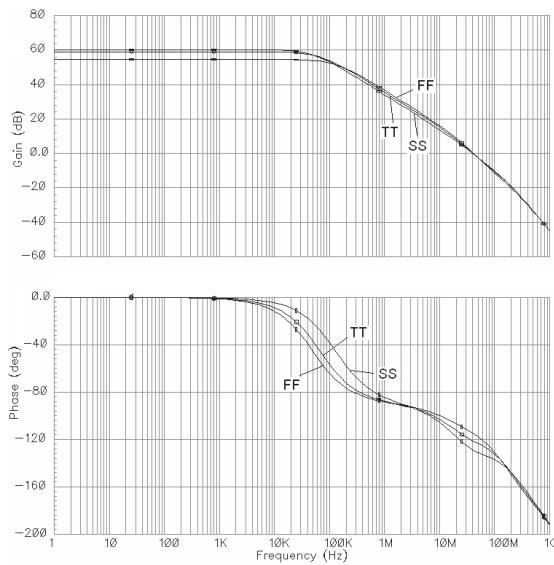


Fig. 6 Corner simulations of the proposed op-amp in open loop.

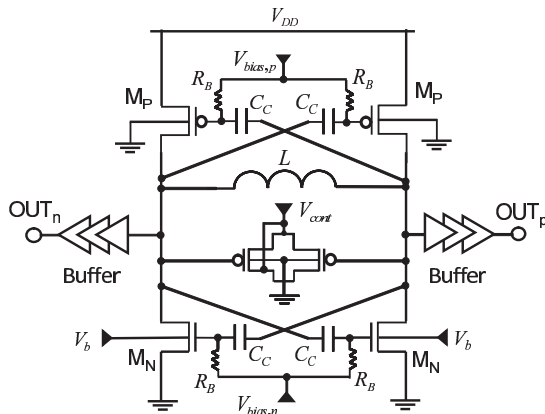


Fig. 7 Schematic of a low-voltage complementary cross-coupled LC-VCO.

to ensure strong inversion operation [22]. The CMOS VCO can be easily modified to realize good independence of process and temperature variations through the forward body biasing scheme, as shown in Fig. 7. The gate biases of the MOS devices in the VCO core can be optimized for phase noise performance [22].

4. Design of 0.5 V-Operation Feedforward Δ - Σ A/D Modulator

Wideband communication applications demand higher oversampling or higher order Δ - Σ A/D modulators to achieve the required performance. To meet such requirements, continuous-time (CT) Δ - Σ modulators have been widely developed [23]. However, a switched-capacitor (SC) Δ - Σ modulator is suitable for the CMOS-inverter-based op-amp described in Sect. 3. In addition, the use of SC Δ - Σ modulators have proven to be a very robust and linear technique that has a manufacturing advantage, because it does not require any tuning compared with CT Δ - Σ modulator. In this section, a 4th-order Δ - Σ A/D modulator using a CMOS-inverter-based op-amp operating at 0.5 V supply is explained as an example [15].

Full feedforward Δ - Σ topology was adopted with reduced sensitivity to integrator nonlinearities [24], making it appropriate in low-voltage wideband applications. Compared to feedback topology, the quantization noise transfer function of the feedforward topology remains the same and the signal transfer function is unity, so that it is difficult for this modulator to be affected by the non-idealities of analog building blocks. In this modulator, the internal signal swing can be well controlled by optimizing the loop coefficients, and thus significantly reducing modulator distortion. Furthermore, only one feedback D/A converter is required, which remarkably simplifies the feedback circuit, and is especially helpful for high-order design.

Figure 8 shows the topology of a 4th-order feedforward Δ - Σ A/D modulator [25]. It mainly consists of four inverter-based integrators, denoted as $I(z)$, and a 1-bit comparator. The coefficients $[a_1, a_2, a_3, a_4; c_1, c_2, c_3, c_4]$ are selected as $[0.2, 0.4, 0.1, 0.1; 1, 1, 1, 2]$ to maintain loop stability. MATLAB behavior simulations show a good SNR, and each of the integrator output levels is limited in the range of $0.1\sim 0.4$ V under 0.5 V supply and with a reference voltage of $V_{ref} = \pm 0.3$ V.

The circuit implementation of the designed low-voltage A/D modulator is shown in Fig. 9. The switched-capacitor integrator is used in this design. The body-input gate-

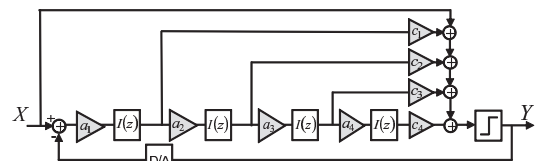


Fig. 8 A 4th-order feedforward Δ - Σ modulator.

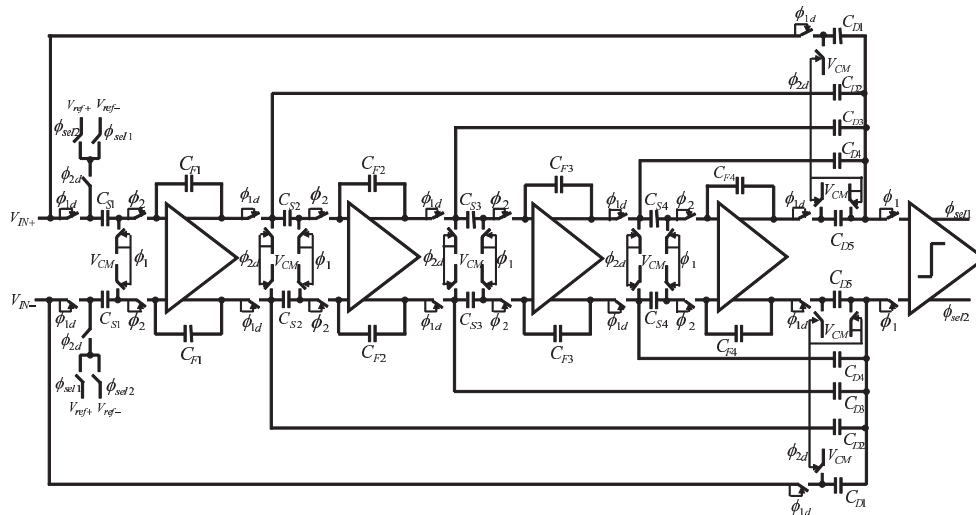


Fig. 9 Circuit implementation of the designed A/D modulator.

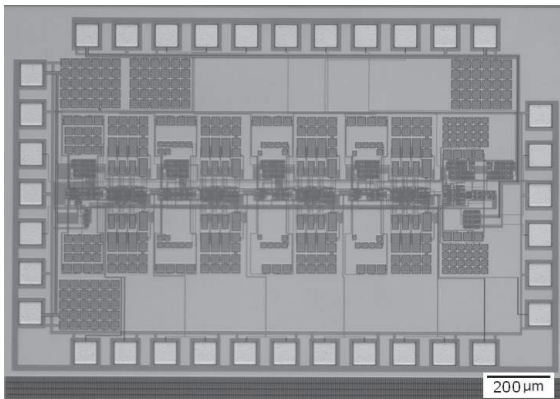


Fig. 10 Micrograph of a 0.5 V feedforward Δ - Σ A/D modulator fabricated in a 0.18 μm CMOS process.

clocked comparator shown in Fig. 2, boot-strapped single NMOS switches as shown in Fig. 3, and the CMOS-inverter-based op-amp as shown in Fig. 4 are utilized in this design. At the same time, forward body biasing is used in the digital SR latch following the comparator and output buffers to increase the operation speed. The reference voltages of $V_{ref\pm} = V_{CM} \pm 0.15\text{ V}$ are used, corresponding to $V_{ref} = \pm 0.3\text{ V}$ in MATLAB behavior simulations.

However, the use of bootstrapping capacitance induces a large area penalty. Therefore, the switches in this design are classified. Each of the switches at a signal path has an individual bootstrapped clock circuit to reduce signal distortion, while the other switches connected with V_{CM} share bootstrapped clocks according to their clock phases. In this way the chip area is significantly decreased.

The feedforward Δ - Σ A/D modulator is designed in a standard 0.18 μm CMOS process with metal-insulator-metal (MIM) capacitors and six metal layers with a 0.5 V supply. A micrograph of the chip is shown in Fig. 10. Excluding the bonding pads and other peripheral circuitry, the core area is approximately $0.5 \times 1.5\text{ mm}^2$. Figures 11 and 12

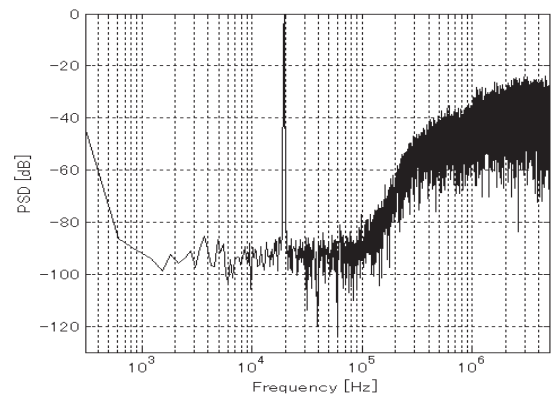


Fig. 11 Measured output spectrum at $V_{in} = -8\text{ dB}V_{ref}$ (Spectrum computed with 32768-point FFT).

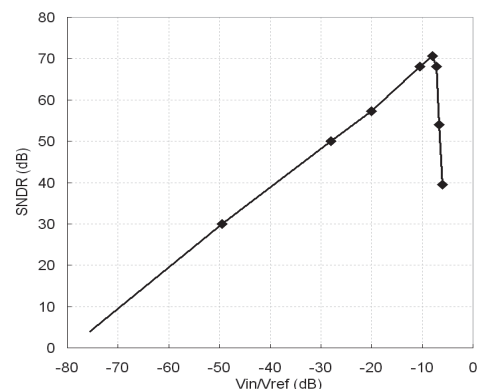


Fig. 12 Test SNDR vs. input amplitude.

show the output spectrum characteristics and the main performance parameters are summarized in Table 1. The sampling frequency is 10 MHz and the spectra are computed with a 32768-point fast Fourier transform (FFT). Test results show a good FOM, in that a peak SNDR of 71 dB is achieved for a 78 kHz signal bandwidth with power consumption of

Table 1 Main performance of 0.5-V feedforward Δ - Σ A/D modulator fabricated in 0.18 μm CMOS process.

Parameter	This study
Supply [V]	0.5
Sampling Frequency [MHz]	10
Bandwidth [kHz]	78
SNDR [dB]	71
Power [μW]	860
FOM* [pJ/conv.]	1.9
Op-amp DC Gain [dB]	59
Op-amp UGB [MHz]	42
Op-amp Power [μW]	168

*FOM = $\frac{\text{Power}}{2 \times \text{ENOB} \times 2 \times \text{Bandwidth}}$

860 μW under 0.5 V supply.

5. Area-Efficient Transformer Folded-Cascode CMOS Low-Noise Amplifier

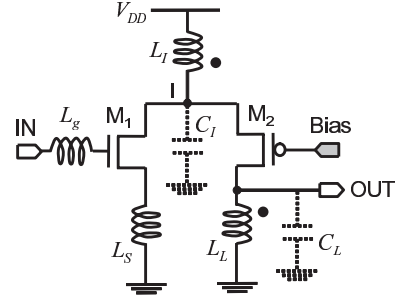
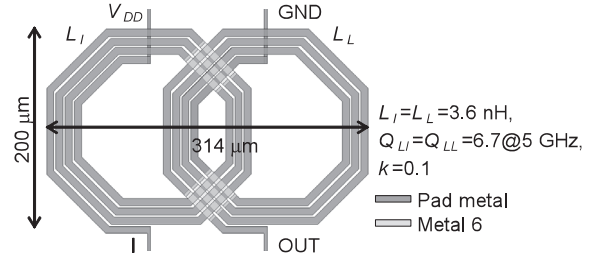
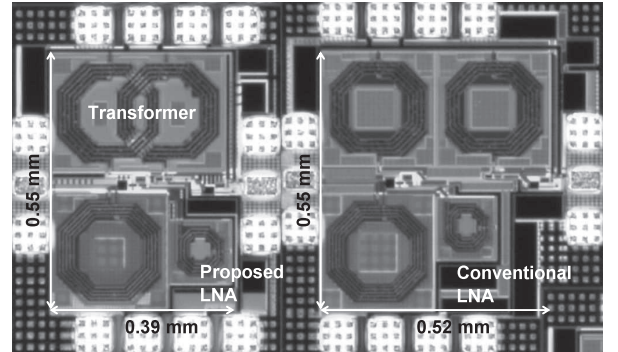
Continuous CMOS technology scaling imposes two challenges on RFICs; low-voltage operation and a small chip area. Previously reported low-voltage low-noise amplifiers (LNAs) [26]–[29] require many inductors, which increase both the chip area and the cost. Although folded-cascode LNAs [26], [29] are more suitable for low voltage operation ($V_{DD} > V_{DS,sat}$), they require more inductors, which leads to an increase in the chip area. In this section, a low-voltage transformer folded-cascode CMOS LNA is proposed [30].

Figure 13 shows the proposed LNA based on a conventional folded-cascode LNA with inductive source degeneration. The gate and source inductors, L_g and L_s , provide input impedance matching at an operating frequency [31]. The PMOS transistor M_2 reduces the Miller effect of the gate-drain capacitor of the input transistor M_1 , and improves the reverse isolation performance of the LNA. The internal inductor L_I resonates with parasitic capacitance C_I at node I and provides a high impedance, thereby the signal current amplified by M_1 flows into M_2 . The load inductor L_L also resonates with parasitic capacitance C_L , resulting in a high impedance. These inductors, L_I and L_L , are magnetically coupled to form a transformer in such a way so as to have positive magnetic coupling while retaining the LNA performance. The transformer shifts the peak of the LNA gain to a lower frequency. The peak frequency ω_p is approximately expressed as

$$\omega_p \approx \sqrt{\frac{1-nk}{1-k^2}} \frac{1}{\sqrt{L_L C_L}}, \quad (4)$$

where $n = \sqrt{L_L/L_I}$ and k are the turn ratio and coupling factor of the transformer, respectively. Based on careful consideration on peak frequency of the LNA gain, the partially coupled transformer ($k \approx 0.1$) shown in Fig. 14 can give less performance deterioration in input matching, peak gain, and NF, compared to the conventional one.

The proposed LNA was implemented in a 90 nm digital CMOS process. For comparison, the conventional folded-cascode LNA was also implemented on the same chip. Micrographs of the fabricated LNAs are shown in Fig. 15. The

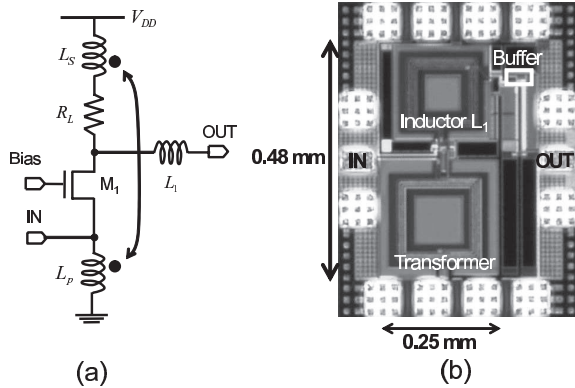
**Fig. 13** Schematic of the transformer folded-cascode CMOS LNA.**Fig. 14** Layout of a partially-coupled transformer.**Fig. 15** Micrographs of the proposed LNA (left) and conventional folded-cascode LNA (right), fabricated in a 90 nm digital CMOS process.

active chip areas (excluding pads) of the proposed and conventional LNAs are $0.39 \times 0.55 \text{ mm}^2$ and $0.52 \times 0.55 \text{ mm}^2$, respectively. The S-parameters, NFs, and linearity of the LNAs were measured using on-wafer RF probes. The power consumption, excluding the buffer, was 1.0 mW at a supply voltage of 0.5 V. The proposed LNA obtained $|S_{11}| < -10 \text{ dB}$, $|S_{21}| = 16.8 \text{ dB}$, and $\text{NF} = 3.9 \text{ dB}$ at 4.7 GHz. The magnetic coupling in the proposed LNA had a small impact on the S_{11} and NF performance. Table 2 shows a summary of the performance and a comparison with previously reported low-voltage ($< 0.7 \text{ V}$) CMOS LNAs for 5 GHz application. The proposed LNA achieved performance comparable with the conventional folded-cascode LNA, while having only 75% of the chip area of the conventional LNA. FoM in Table 2 is defined in Ref. [26], [30]. Among the reported low-voltage CMOS LNAs, the proposed LNA obtained the best FoM with the smallest chip area.

Recently, we developed an ultra-wideband (UWB)

Table 2 Measured performance and comparison of low-voltage CMOS LNAs.

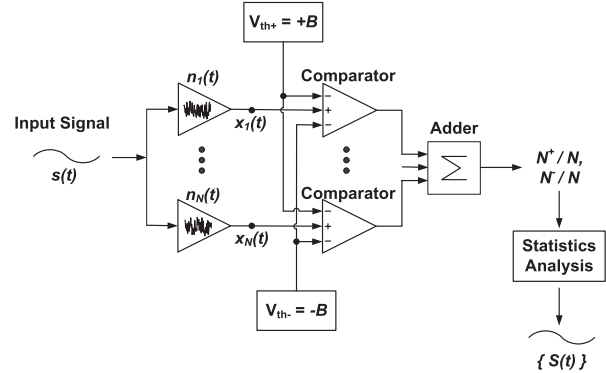
Reference	CMOS Technology	Frequency [GHz]	NF [dB]	Gain [dB]	IIP ₃ [dBm]	P _{in-1 dB} [dBm]	Supply [V]	Power [mW]	Area [mm ²]	FOM [mW ⁻¹]
This work	90 nm	4.7	3.9	16.8	-14.8	-27	0.5	1.0	0.21	4.8
Folded-cascode LNA	90 nm	5.0	4.1	16.1	-14.8	-27	0.5	1.0	0.29	4.1
[26]	90 nm	5.5	3.6	9.2	-7.25	-15.8	0.6	1.0	0.30	2.2
[27]	130 nm	5.1	5.3	10.3	N/A	-22	0.4	1.0	0.75	1.4
[28]	180 nm	5.0	4.5	9.2	-16	-27	0.6	0.9	0.54	1.8
[29]	180 nm	5.8	2.9	7.0	N/A	-9	0.7	12.5	0.40	0.2
[32]	180 nm	5.0	3.65	14.1	-17.1	-25	0.6	1.68	0.46	2.3

**Fig. 16** (a) Proposed transformer noise-canceling UWB CMOS LNA and (b) micrograph of the LNA fabricated in a 90 nm digital CMOS process.

CMOS LNA with transformer noise-canceling [33], as shown in Fig. 16. The transformer composed of magnetically coupled inductors L_p and L_s cancels the noise produced by M_1 and the load resistor R_L . This transformer technique can also contribute to chip area reduction. One approach to chip area reduction is the use of transformers instead of inductors. The transformer in the UWB LNA shown in Fig. 16 is a fully-coupled type used to enhance noise canceling.

6. Signal Detection Suitable to Mismatch and Noise

Receiver architectures based on conventional A/D converters are approaching their limit in maintaining resolution under low-voltage operation [11], [34]. Even if A/D converters follow the gain stages of amplifiers in the receiver chain to maintain resolution, the amplifiers themselves will have difficulty in retaining nonlinear-distortion with sufficient gain under such a low supply voltage. For example, comparison with linear-in-dB variable gain amplifiers (VGAs) with almost the same topology, which are designed under different supply voltages and different process technologies (2.5 V in a 0.25 μm CMOS process and 1.5 V in a 150 nm FD-SOI CMOS process), reveals scaling merits in bandwidth and occupied area, while they can have only similar IIP₃, NF, and gain ranges by adjusting the central value of gain [35], [36]. If a larger gain is set under a low supply voltage, the VGAs have less linearity (smaller IIP₃). Therefore, new signal detection techniques to break through this limitation have be-

**Fig. 17** Schematic diagram of the proposed signal detection system.

come an urgent research target.

Although noise-aided detection of weak signals in neurons has been the subject of considerable attention in connection with the phenomenon of stochastic resonance (SR) [37], [38], recent research has also demonstrated SR in nanoscale electron devices [39], [40]. As described in the comprehensive review by Gammaitoni et al. [38], the SR phenomenon can be generally observed in bistable threshold-based systems that are forced by both of two components: (1) a signal with an amplitude lower than the system threshold, and (2) noise that is inherent in the system. This phenomenon can be interpreted as a reduction in system threshold, which is simply modeled using Brownian particles in a quartic-double-well potential [38]. Recently, a novel subthreshold signal detection technique was developed for a communication system, which is suitable for implementation in future nanoscale CMOS technology [41]. This section briefly introduces this faint-signal detection technique.

Figure 17 shows a schematic representation of the proposed system. Using an analog comparator as a detection device, it is assumed that the input signal of the comparator is smaller than the noise level, in addition to the threshold value. As the input signal is shared with N amplifiers of the same gain, each output signal $x(t)$ is the sum of the amplified input signal and the inherent yet uncorrelated noise generated in each amplifier. The comparator then converts the output signal $x(t)$ to a digital signal by comparison with the threshold levels, $+B$ and $-B$. From the N comparator outputs, the number of output signals that are larger than $+B$ is represented as N^+ , and that smaller than $-B$ as N^- . As a

result, two output values, N^+ and N^- , are obtained from one input signal $s(t)$.

Note that the thermal and shot noise in electrical devices are represented as typical Gaussian white noise [42]. Under such Gaussian white noise, the input signal $s(t)$ can be restored from the probability for detection of a signal using the time or ensemble statistics of the comparator outputs, that is, N^+/N and N^-/N , as follows.

$$S(i) = \begin{cases} B - \sqrt{2} \sigma_n \operatorname{erf}^{-1} \left\{ 2 \left(\frac{1}{2} - \frac{N^+}{N} \right) \right\} & (N_i^+ > N_i^-), \\ -B - \sqrt{2} \sigma_n \operatorname{erf}^{-1} \left\{ 2 \left(\frac{N^-}{N} - \frac{1}{2} \right) \right\} & (N_i^+ < N_i^-), \\ 0 & (N_i^+ = N_i^-). \end{cases} \quad (5)$$

Here σ_n is the standard deviation of the noise, and $S(i)$ represents the sample value of $s(t)$ at $t = iT_s$ ($i = 0, 1, 2, \dots$), where T_s is the sampling period.

In order to estimate the detection sensitivity or limit of the proposed system, numerical simulations are carried out under a set-up of unity gain amplifiers for simplification. For the m -phase-shift-keying (m -PSK) modulated input signal, a bit error rate (BER) less than or equal to 10^{-3} is required for reliable signal detection in typical wireless communications, which provides the detection sensitivity for the subthreshold signal. The minimum amplitude of the input signal satisfying this requirement, $A_{s,min}$, can be obtained by the numerical simulations. $A_{s,min}/B$ is used as the detection sensitivity, which is normalized by the threshold B . A smaller $A_{s,min}/B$ indicates better detection sensitivity.

The numerical simulation results shown in Fig. 18 can be approximated by

$$\frac{A_{s,min}}{B} = \frac{P}{Q} \sqrt{\frac{m}{OSR \times N}} \frac{\sigma_n}{B} \exp \left(Q^2 \frac{B^2}{2\sigma_n^2} \right), \quad (6)$$

where $P \approx 2.4$ and $Q = (\sigma_n/B)_{\text{opt}}$ are fitting parameters. The deduction of Eq. (6) is described in Ref. [41]. For large N , Eq. (6) explains the detection behavior very well. As seen in Fig. 18, the increase of N can enhance the detection sensitivity and also provide a slightly wider margin for the optimal threshold value. This behavior is similar to that in many SR systems [37]–[40].

Figure 19 reveals the enhancement in detection sensitivity with the increase of N and oversampling ratio (OSR). This indicates that the performance of the proposed architecture can be improved with scaling-down of the integrated circuit. The detection sensitivities for the QPSK and 8PSK modulated input signals differ from that for BPSK by a factor $\sqrt{2}$ and 2, respectively. This means that OSR or N should be doubled and quadrupled for the QPSK and 8PSK input signals, respectively, to achieve the same sensitivity as that for BPSK. These results are consistent with the theoretical results from Eq. (6).

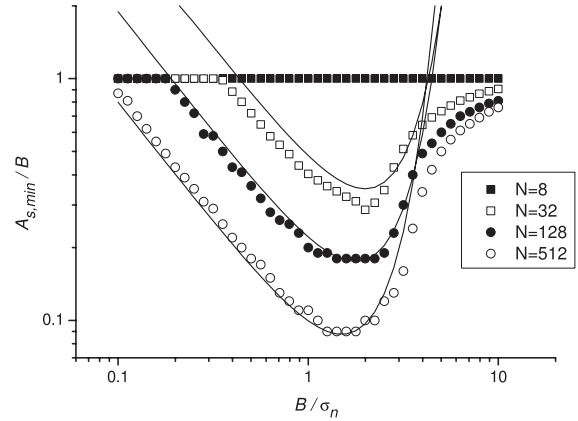


Fig. 18 Detection sensitivity $A_{s,min}/B$ as a function of B/σ_n ($OSR = 4$, BPSK). The solid lines represent the data approximated using Eq. (6).

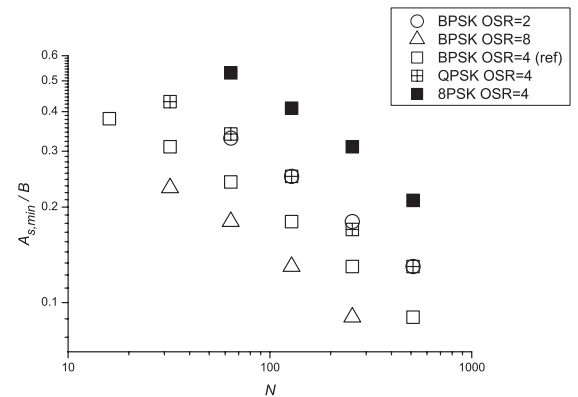


Fig. 19 Detection sensitivity $A_{s,min}/B$ as a function of N , OSR and m -PSK ($B/\sigma_n = 1.77$).

Device parameter mismatches in the chip tend to limit the resolution of many analog integrated circuits [11]; therefore, acceptable parameter mismatches were investigated for the proposed signal detection system. In the proposed system, the mismatch of each arrayed circuit can be evaluated equivalently as DC noise. Thus, the total noise and device mismatch can be expressed as

$$\sigma_{total} = \sqrt{\sigma_n^2 + \sigma_{th}^2 + \sigma_{gain}^2 A_s^2 / G^2}, \quad (7)$$

where σ_n , σ_{th} and σ_{gain} are the standard deviations of noise, comparator threshold B , and amplifier gain G , respectively. The mismatches of threshold and gain approximately follow the Gaussian distribution, which is based on experimental device mismatch data [9], [10]. The numerical simulation results shown in Fig. 20 reveals no degradation in performance for the proposed signal detection system, even for 20% parameter mismatches, and even exhibits sensitivity improvement in the case of high threshold. These results indicate that the parameter mismatches are effectively equivalent to the DC noise. Recently, a flash A/D converter using offset variations of comparators instead of references was reported [43]. The performance of the flash A/D converter supports the present numerical simulations.

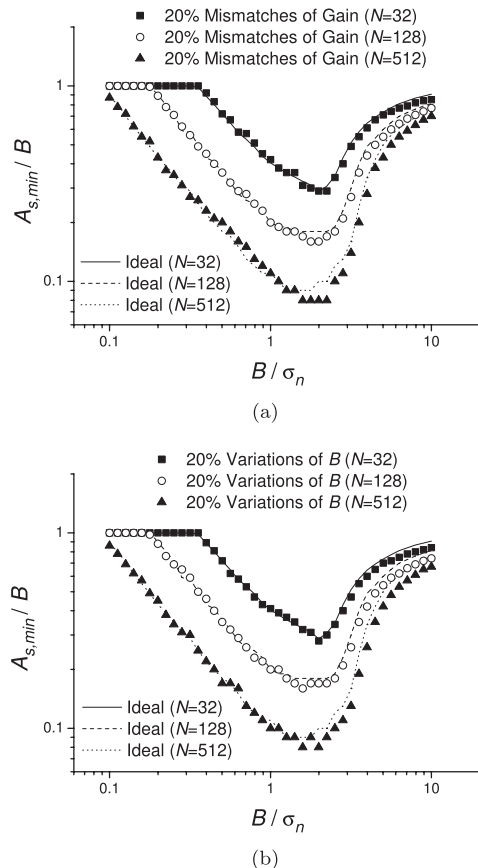


Fig. 20 Detection sensitivity with consideration of the variation in (a) gain, and (b) threshold ($OSR = 4$, BPSK).

The proposed signal detection technique can have superior detection sensitivity, beyond that of conventional A/D-converter-based CMOS receivers, and provide a solution for maintaining resolution under low-voltage operation. In addition, improved performance in signal restoration is expected when combined with a q -bit A/D converter ($q > 2$). In other words, the proposed technique can provide super-resolution features beyond the LSB of conventional q -bit A/D converters. This feature is useful for high-speed A/D converters with low-to-moderate resolution that can easily have scaling advantages. Even in Δ - Σ A/D modulators, SR may help to enhance resolution [44]. Whereas dynamic element matching, which is applied for the improvement of D/A converters and programmable gain amplifiers [45], [46], relaxes the influence of device mismatches on circuit precision, this technique instead utilizes device mismatches.

This technique is at an early stage of development; therefore, there is much room for further investigation, such as circuit design. However, it is our belief that the proposed technique will provide a new design paradigm for wireless receivers.

7. Conclusions

There are some techniques available to achieve low-voltage

analog circuits, such as forward body biasing, inverter-based circuit techniques, area-efficient passive elements, and SR signal detection. Forward body biasing can enhance device drivability while maintaining low off-state leakage current. This technique is also useful to compensate for device characteristic variations due to process and temperature. Inverter-based circuit techniques ensure the possibility of analog CMOS circuit utilization when digital CMOS circuits can be realized. Use of area-efficient passive elements, such as transformers in RF circuits, can reduce the total occupation area of the passive elements. Although the area efficiency may not be sufficient, it is one promising technique for analog-centric RF circuit designs. Although application of SR to CMOS signal detection circuits is in the early stage of development, it promises to provide a new design paradigm for ultra-low-voltage analog circuit design.

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