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A Low-Power Multi Resolution Spectrum Sensing Architecture for a Wireless Sensor Network with Cognitive Radio

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SUMMARY Concomitantly with the progress of wireless communications, cognitive radio has attracted attention as a solution for depleted frequency bands. Cognitive radio is suitable for wireless sensor networks because it reduces collisions and thereby achieves energy-efficient communication. To make cognitive radio practical, we propose a low-power multi-resolution spectrum sensing (MRSS) architecture that has flexibility in sensing frequency bands. The conventional MRSS scheme consumes much power and can be adapted only slightly to process scaling because it comprises analog circuits. In contrast, the proposed architecture carries out signal processing in a digital domain and can detect occupied frequency bands at multiple resolutions and with low power. Our digital MRSS module can be implemented in 180-nm and 65-nm CMOS processes using Verilog-HDL. We confirmed that the processes respectively dissipate 9.97 mW and 3.45 mW.

key words: *MRSS, multi-resolution spectrum sensing, cognitive radio, wireless sensor network, low power*

1. Introduction

Society is confronting bandwidth exhaustion problems because frequency bands, which are useful for wireless communications, are limited. Moreover, putting new wireless communication systems into practice is difficult. For those reasons, cognitive radio has attracted attention [1], [2]. It dynamically senses a frequency spectrum and uses available frequency bands for communication. In so doing, it can dramatically improve bandwidth efficiency.

Furthermore, cognitive radio is useful to enhance power efficiency in a wireless sensor network. A combination system of cognitive radio and wireless sensor networks was proposed in earlier reports [3], [4]. Using the cognitive wireless sensor network, sensor nodes can reduce collisions and interference in data communication, thereby extending the network lifetime, especially for applications that frequently execute communications such as "flooding". Nevertheless, several technical issues must be resolved for the use of cognitive radio in wireless sensor networks.

- Spectrum sensing techniques that can recognize surrounding radio wave conditions correctly.
- A reconfiguration system that changes communication parameters appropriately based on sensing results.
- A dynamic interference avoidance system.

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Spectrum sensing techniques are the most important for cognitive radio. Because cognitive radio is anticipated for use in various environments in a wireless sensor network, flexibility in spectrum sensing (such as sensing bandwidth, sensing time, and sensing sensitivity) is required. However, that turns out to entail enormous power consumption. Conventional multi-resolution spectrum sensing (MRSS) [5], [8] also consumes large amounts of power: it mainly comprises analog circuits in which a sensing bandwidth and sensing sensitivity are altered by an analog variable filter. To make matters worse, analog circuits will be increasingly unable to adapt to future process scaling.

As described herein, we specifically examine low-power MRSS techniques for spectrum sensing in the cognitive wireless sensor network. Low-power spectrum sensing techniques are demanded to realize the sensor network system with the cognitive radio because sensor nodes have limited battery power. We propose a new low-power MRSS architecture, mainly consisting of digital circuits, to address the problems related to conventional MRSS. We model our MRSS architecture using MATLAB (The MathWorks Inc.); then it is implemented using Verilog-HDL. Finally, we estimate the power consumption of our proposed module and compare it with that of conventional MRSS.

2. Multi Resolution Spectrum Sensing (MRSS): Conventional Architecture

In general, spectrum sensing requires many frequency filters with different characteristics to detect available frequency bands as sensing targets. On the other hand, MRSS senses the widespread spectrum using a flexible filter, which can change its characteristics in center frequency and bandwidth. The advantages of MRSS are therefore to have flexibility in terms of the center frequency and bandwidth, and not to necessitate preparation of various frequency filters. For example, a filter's bandwidth can be set arbitrarily. Then a center frequency can be scanned for sensing of the spectrum.

The sensing time is also varied. If the bandwidth is greater, it takes less time to scan the whole frequency spectrum; it takes more time in narrow-bandwidth scanning. In other words, a tradeoff exists between the frequency sensitivity and sensing time. Progressive sensing, by which coarse sensing is followed by fine sensing, is also possible.

Figure 1 portrays a receiver block diagram in the con-

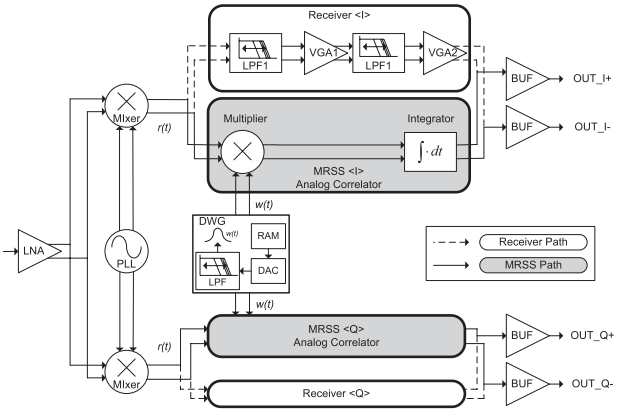

Fig. 1 Block diagram showing a conventional MRSS receiver.

ventional MRSS architecture.

The receiver has a low intermediate frequency (IF) architecture with differential signaling. The receiver has receiver paths and MRSS paths after the mixer stages. In the analog correlator in MRSS, a spectrum is sensed using an energy detection method, which detects the presence of a carrier frequency in the target bandwidth, judging from the integrator's output. In reality, this conventional method carries out filtering in a frequency domain by multiplying a window function and integrates it in a time domain. This concept is called "windowing". Formulas (1) and (2) show the concept of windowing using a cross-correlation operator:

$$\begin{aligned}(w * r)(x) &= \int_{-\infty}^{\infty} w^*(t)r(x+t)dt \\ &= \int_{-\infty}^{\infty} w(t)r(x+t)dt \\ &= \int_{-\infty}^{\infty} W(f)R(f)e^{j2\pi fx}df \end{aligned} \quad (1)$$

$$\begin{aligned}(w * r)(0) &= \int_{-\infty}^{\infty} w^*(t)r(t)dt \\ &= \int_{-\infty}^{\infty} w(t)r(t)dt = \int_{0}^{t_w} w(t)r(t)dt \\ &= \int_{-\infty}^{\infty} W(f)R(f)df \end{aligned} \quad (2)$$

where $w(t)$ is the window function:

$$w(t) = \begin{cases} w(t_w - t), & \text{if} \quad 0 < t < t_w \\ 0, & \text{elsewhere} \end{cases} \quad (3)$$

Therein, $r(t)$ is a baseband signal that is down-converted using a mixer. By sweeping a frequency of a phase-locked loop synthesizer (PLL), an input signal with a wide frequency band can be down-converted to a baseband signal. Then it is multiplied by $w(t)$ generated using a digital window generator (DWG). The $w(t)$ has the same characteristic as a low pass filter (LPF) in the frequency domain. The sensing bandwidth is inversely proportional to t_w (the pulse width of $w(t)$): a narrow window in the time domain has a wide bandwidth in the frequency domain (a wide window has a narrow bandwidth) [6]. Because of these characteristics, the conventional method can change its bandwidth dynamically.

The DWG consists of random access memory (RAM), a digital-to-analog converter (DAC), and an LPF. The RAM stores window data, and the DAC and LPF reconstruct the window signal with a variable pulse width. The pulse width, t_w, can be controlled using two methods: changing the clock frequency and addressing the RAM.

Then, the multiplier's output is integrated. The integrator is reset for the next MRSS operation as soon as multiplication of $r(t)$ and $w(t)$ finishes. The average output value from the integrator is evaluated as the signal intensity.

The conventional MRSS architecture described above presents several issues. First, it consumes much power because the MRSS block has many analog circuits: the DAC, LPF, multiplier, and integrator. Therefore, it is difficult to adapt to process scaling: analog circuits cannot be scaled down or cannot achieve low power, even in a scaled process. Second, in the conventional architecture, wide t_w is necessary to narrow a bandwidth. It spends a long time for sensitive spectrum sensing.

3. Multi Resolution Spectrum Sensing (MRSS): Proposed Architecture

To address the problems in the conventional MRSS architecture, we propose another MRSS using a digital filter with a variable bandwidth. Sensitivity and bandwidth in sensing can be altered by changing the filters' characteristics. Figure 2 presents an overview of the proposed MRSS.

Actually, F_{PLL} is a current frequency in the phase lock loop (PLL); the current sensing width is PLL_{step}. In other words, the current sensing range is F_{PLL} to $F_{PLL} + PLL_{step}$. The sensing width, PLL_{step}, is divided into N_{filter} filters: N_{filter} is PLL_{step}/F_{step}, where F_{step} is an interval between the filters. The center frequency of the current filter is defined as F_c, which is initially F_{PLL} and which is increased by F_{step} in every filter. The filter bandwidth BW is presumed to be fixed at this time, but it can be changed dynamically.

The transition to the next sensing range is achieved by renewing F_{PLL} (e.g. $F_{PLL} = F_{PLL} + PLL_{step}$). In this operation, the number of filters in a sensing width (sensitivity) is dependent on F_{step}.

3.1 Block Diagram

Figure 3 shows the receiver architecture of the proposed digital MRSS architecture. The MRSS block is located after the analog-to-digital converter (ADC) for processing in the digital domain. The following subsections describe the RF front-end, ADC, MRSS block, and demodulator/decision block.

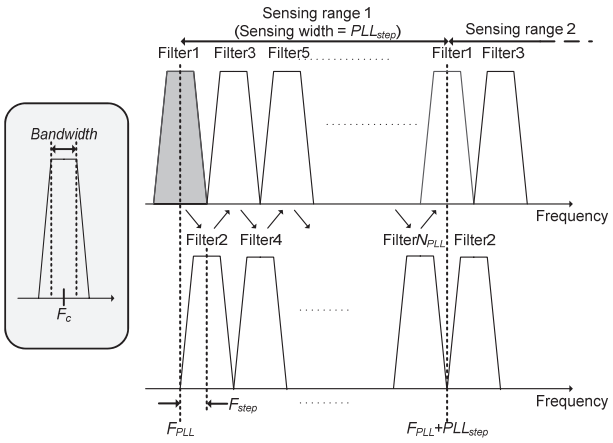

Fig. 2 Overview of proposed MRSS.

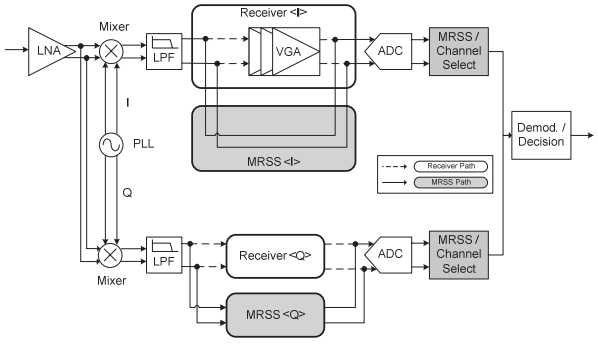

Fig. 3 Proposed MRSS receiver.

3.2 RF Front-End

The RF front-end including the PLL is almost identical to the conventional MRSS architecture; the receiver path and MRSS path are divided and switched. The MRSS path is forwarded directly to the ADC because the MRSS merely detects the existing spectrum. In contrast, the receiver path, which is used for data communication, passes through a variable gain amplifier (VGA). For data communications, the MRSS block must operate as a channel selection filter. Therefore, the VGA is activated in the receiver path.

3.3 Analog-to-Digital Converter (ADC)

The PLL and ADC in the proposed architecture require little overhead because a PLL and ADC are necessary even in the conventional one as well.

The conventional analog MRSS scheme achieves a dynamic range from −74 dBm to −42 dBm at a 1.8-V supply voltage. We aim for a dynamic range from −80 dBm to −40 dBm using the ADC. At the same time, we assume that a gain of the RF front-end is 28 dB [7]. Therefore, the received signal becomes 22.36 μV–2.236 mV as an input voltage to the ADC. We set a resolution of the ADC to seven bits with a dynamic range between 0 V and 2.8 mV. In this

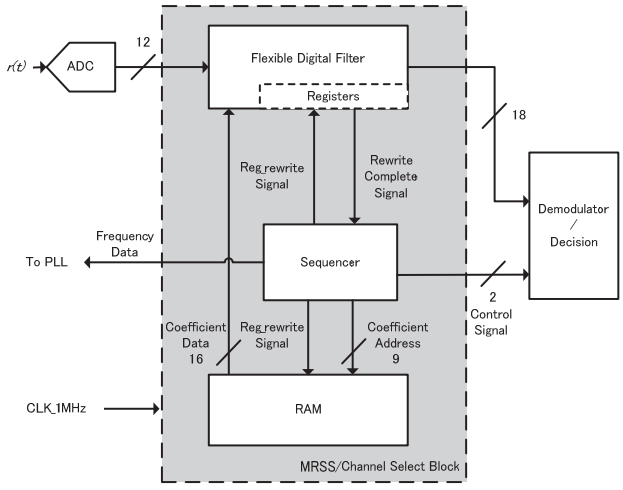

Fig. 4 Block diagram of MRSS.

case, because the LSB is equal to 21.97 μV, the ADC can detect the minimum input signal.

Note that, the specifications of RF frontend circuits located before our proposed MRSS blocks could change depending on system requirements. In this paper, we suppose that the PLL and ADC in the proposed MRSS and the conventional MRSS have the same specification, except the bit resolution in the ADC as mentioned above.

3.4 MRSS Block

In this subsection, we describe the proposed digital MRSS block. The MRSS function is implemented with a flexible digital filter, SRAM for data of the filter's coefficient, and a sequencer (Fig. 4). The sequencer controls not only the MRSS module itself but also the frequency output from the PLL and the subsequent demodulator/decision block.

a) Workflow

Figure 5 shows a flowchart for the sequencer in the proposed MRSS block. Each process is described as follows:

A: BW (filter bandwidth), F_c (filter center frequency), N_{data} (number of reference data), F_{step} (interval between filters), $N_{filters}$ (number of filters in a sensing range), N_{range} (number of sensing ranges), and PLL_{step} (frequency step of the PLL) are set up.
B: Initialize i_{range} (number of counts for changing the PLL frequency).
C: Initialize i_{filter} (number of counts for changing coefficient data).
D: Coefficient data for the present F_c is read out from RAM and stored in registers in the flexible digital filter.
E: Filtering by BW and F_c are conducted N_{data} times using a flexible digital filter.
F: i_{filter} is incremented; it updates F_c ($F_c = F_c + F_{step}$)
G: If i_{filter} equals $N_{filters}$, then go to H. Otherwise, return to D.
H: i_{range} is incremented.
I: If i_{range} equals N_{range}, then go to J. Otherwise, update

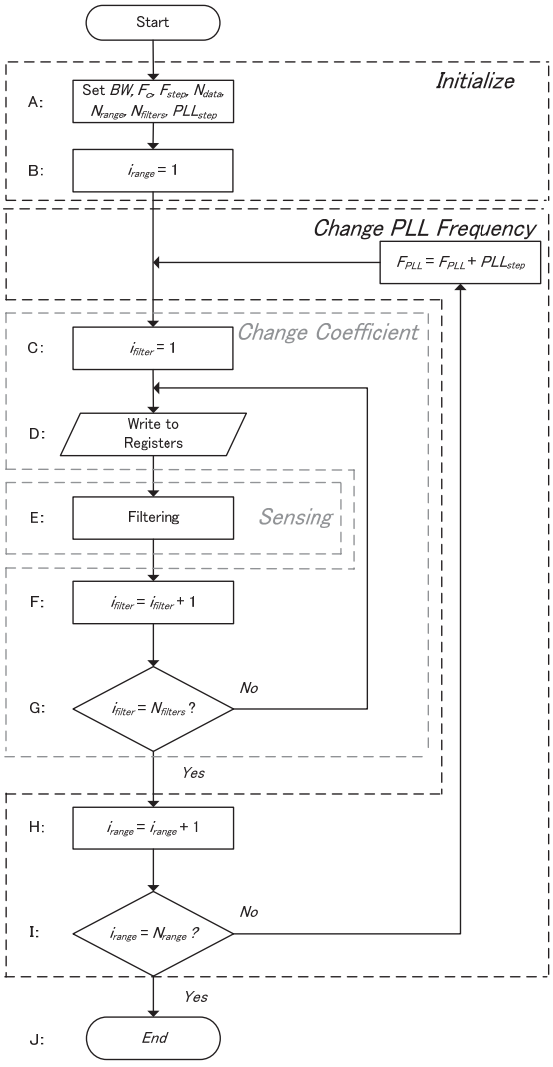

Fig. 5 Flowchart in MRSS.

F_{PLL} ($F_{PLL} = F_{PLL} + PLL_{step}$); then return to C.

J: MRSS ends.

b) Flexible Digital Filter

We adopted an infinite impulse response (IIR) filter to reduce a filter order. In particular, we implemented an Elliptic IIR filter because it can achieve low power and steep edges. The filter characteristic is depicted in Fig. 6. In this design, as described previously, the target dynamic range is set from −80 dBm to −40 dBm. Even if the maximum power (−40 dBm) is received in an out-of-band (lower than F_{out1} or higher than F_{out2}), it can be rejected because the maximum gain (A_{stop}) in the out-of-band is set to −50 dB. In this filter, the bandwidth ($F_{pass2} - F_{pass1}$) can be set from 12.5 kHz to 400 kHz.

Figure 7 presents an illustration of the block diagram of the flexible filter comprising the six-stage Biquad circuits and coefficient registers (see Fig. 8 for a Biquad circuit; one corresponds to a second-order filter). The sequencer in the MRSS block reads the coefficient data from the SRAM (512 words × 16 bits), and writes them to the registers. Once the variable range of the bandwidth is set from 12.5 kHz to 400 kHz, the minimum and maximum filter orders result in 8 and 12, respectively. The Biquad circuit(s) at stage 5 and/or 6 can be clock-gated in some cases to reduce the filter power consumption.

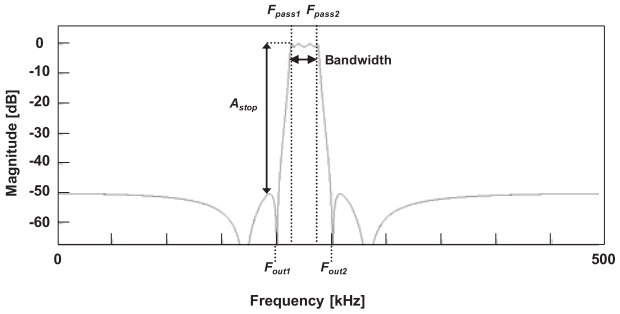

Fig. 6 Filter characteristic.

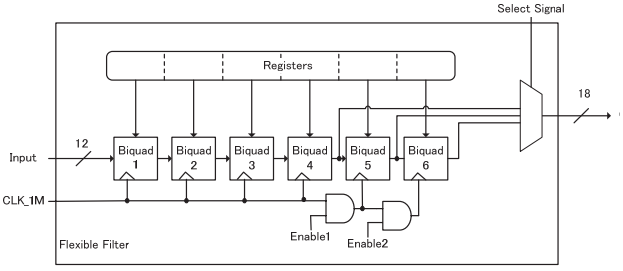

Fig. 7 Block diagram of the flexible filter.

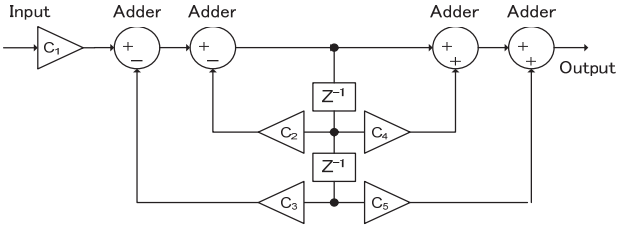

Fig. 8 Biquad circuit.

3.5 Demodulator/Decision Block

Figure 9 presents an illustration of the demodulator/decision block. In the receiver mode, this block demodulates received data, although it only determines whether a spectrum exists or not in the MRSS mode.

3.6 Sensing Time of MRSS

The total sensing time, t_{total}, in performing the proposed MRSS can be calculated as

$$t_{total} = N_{range} \times ((t_{filter} + t_{reg}) \times N_{filter} + t_{sw}) \quad (4)$$

where t_{filter} is a time for processing a flexible digital filter, t_{reg} is a time for rewriting data to the coefficient register, and

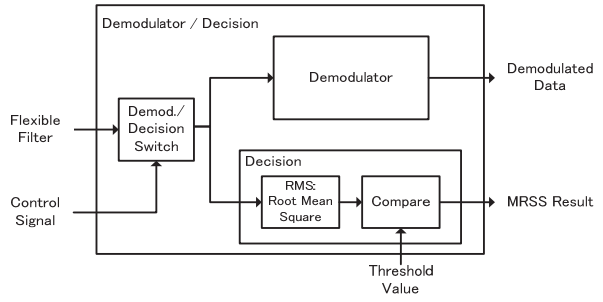

Fig. 9 Block diagram of Demodulator/Decision.

t_{sw} is a switching settling time of the PLL. Thus, t_{filter}, t_{reg}, and N_{range} are represented as follows:

$$t_{filter} = N_{data} \div F_{clock} \tag{5}$$

$$t_{reg} = N_{reg} \div F_{clock} \tag{6}$$

$$N_{range} = \frac{(F_{end} - F_{start})}{PLL_{step}} \tag{7}$$

In these equations, F_{clock} is a sampling frequency of the filter, N_{reg} is the number of coefficient registers, and $F_{end} - F_{start}$ is a frequency range for the MRSS. In this architecture, we set F_{clock} at 1 MHz. For example, if BW is 100 kHz and the spectrum sensing frequency ranges from 600 MHz to 606 MHz, PLL_{step} is 400 kHz, N_{filter} is 4, N_{data} is 1000, N_{reg} is 30. Hence, from (5)–(7), t_{filter} is 0.001 sec, t_{reg} is 30 μsec, N_{PLL} is 15. By defining t_{sw} as 300 μsec [5], the total sensing time will be 0.0663 sec. This number meets the requirement of the draft of IEEE 802.22 specifications that demands the channel sensing time to be completed in less than 2 sec [5].

Under the same condition, the total sensing time in performing the conventional MRSS once will be 1.467 msec by the number of frequency sweeps [5]. In this case, the number of frequency steps is 50 kHz, and the number of frequency sweeps is 121. Therefore, the total sensing time will be 0.177 sec. In the conventional architecture, the number of frequency sweeps becomes large because it uses an LPF. On the other hand, because our proposed architecture uses a band pass filter (BPF), the number of frequency sweeps can be smaller. The proposed MRSS reduces the total sensing time by 62% compared to the conventional analog scheme.

4. Design and Performance Evaluation

This section describes simulation results and presents a comparison of performance to the conventional architecture.

4.1 RTL Simulation

To evaluate the proposed digital MRSS architecture, we implemented it with Verilog-HDL, and conducted a simulation using NC-Verilog. Figure 10 presents a spectrum input example for testing, generated using MATLAB (The MathWorks, Inc.). The test spectrum includes three signals shown in Table 1. We conducted a simulation using this test

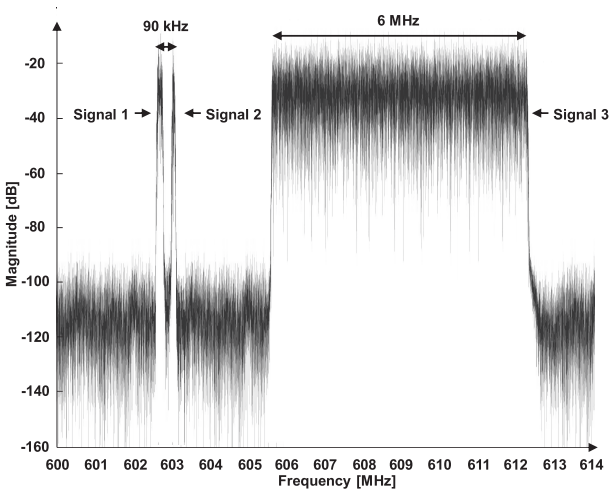

Fig. 10 Input spectrum.

Table 1 Charcteristics of input signals.

	Signal 1	Signal 2	Signal 3
Center Frequency [MHz]	602.56	602.65	609
Band Width [MHz]	0.025	0.01	6

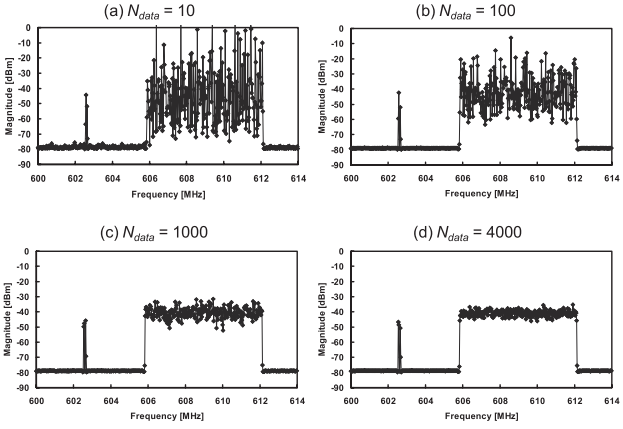

Fig. 11 Simulation results: BW = 25 kHz.

spectrum and the observed output signal.

Figures 11 and 12 portray simulation results obtained when N_{data} was set to be 10, 100, 1000, and 4000. In Fig. 11, BW, F_{step}, PLL_{step}, and N_{filter} were set to be 25 kHz, 25 kHz, 250 kHz, and 10, respectively. In Fig. 12, they were set respectively to 250 kHz, 0 kHz (no interval in filtering = filtering once), 250 kHz, and one.

We performed some simulations: BW was set to 12.5 kHz, 100 kHz, 250 kHz, and 400 kHz. Figure 13 shows σ (standard deviation) of the MRSS output. Smaller σ signifies that the sensing accuracy is higher. To reduce the variation of the MRSS outputs, a large N_{data} or large BW is needed. The time of sensing is, however, increased when N_{data} is increased. Meanwhile, if BW is increased, then the sensing time can be reduced because N_{filter} can be reduced. For example, Fig. 13 shows that all sets, (BW, N_{data})

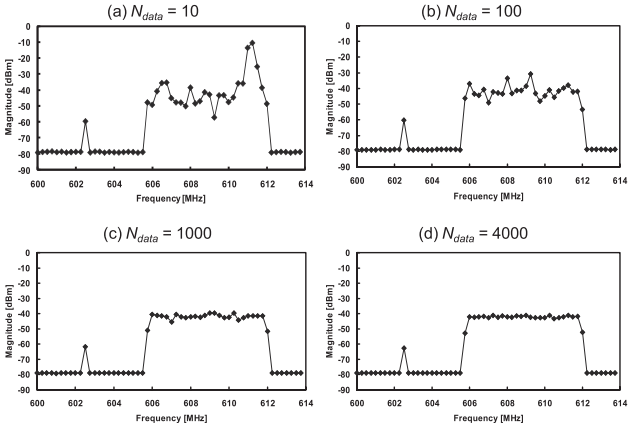

Fig. 12 Simulation results: BW = 250 kHz.

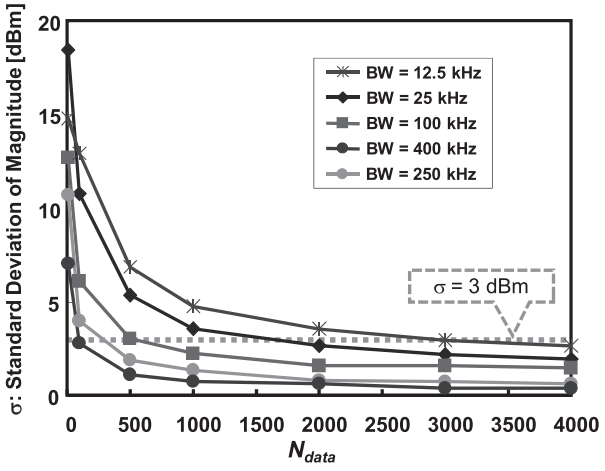

Fig. 13 Standard deviation σ vs. Ndata.

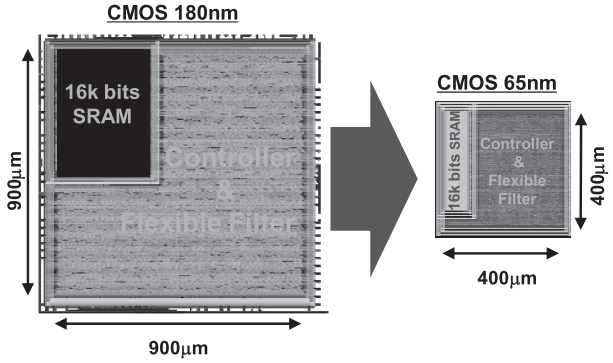

Fig. 14 Chip layouts of proposed MRSS at 180-nm and 65-nm nodes.

= (12.5 kHz, 3000), (25 kHz, 2000), and (100 kHz, 1000) achieve σ of less than ±3 dBm.

4.2 VLSI Implementation

Figure 14 portrays a chip layout of the proposed MRSS core in a 180-nm and 65-nm CMOS technology. The respective core areas are $900 \times 900\,\mu m^2$ and $400 \times 400\,\mu m^2$. These results show that the proposed MRSS has process scalability and that its chip area can be reduced through process scaling.

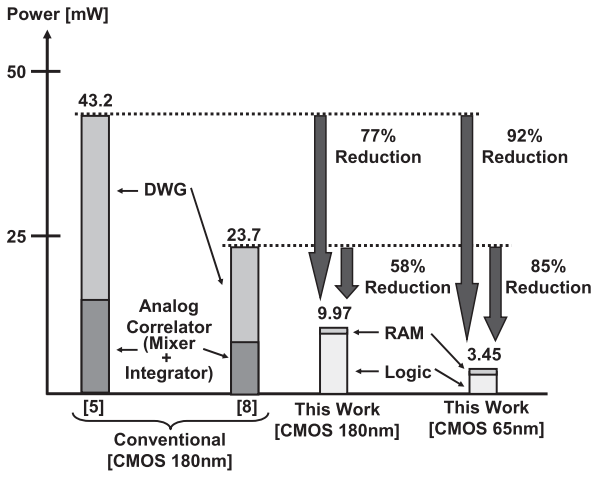

Fig. 15 Comparison of power consumption.

4.3 Power Consumption

To verify the effectiveness of the digital MRSS architecture, we estimated the power consumption on the proposed MRSS block using a Synopsys Power Compiler. Figure 15 presents a comparison between the conventional and proposed MRSS. We compare the power of the MRSS block only because they have almost identical peripheral circuits aside from the MRSS blocks. The proposed MRSS in the 180-nm CMOS technology reduces power consumption by 77% and 58% compared to the conventional analog schemes in [5] and [8], respectively. Furthermore, the 65-nm CMOS technology can reduce the respective power consumptions by 92% and 85%.

5. Conclusion

As described herein, we presented a low-power digital MRSS architecture with digital variable bandwidth filters. We implemented the proposed MRSS module using Verilog-HDL in a CMOS 180-nm process and CMOS 65-nm process, which respectively consume power of 9.97 mW and 3.45 mW, indicating that our proposed architecture is suitable for process scaling, unlike the analog scheme.

In a future work, we will implement the entire receiver. Since the area of a MRSS block is larger than our prediction, reduction of the circuit area is also required.

Acknowledgments

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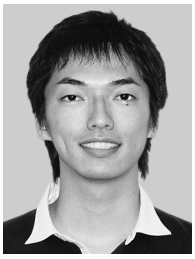

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