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PAPER

A Low Capture Power Test Generation Method Based on Capture Safe Test Vector Manipulation*

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SUMMARY In at-speed scan testing, capture power is a serious problem because the high power dissipation that can occur when the response for a test vector is captured by flip-flops results in excessive voltage drops, known as IR-drops, which may cause significant capture-induced yield loss. In low capture power test generation, the test vectors that violate capture power constraints in an initial test set are defined as capture-unsafe test vectors, while faults that are detected solely by capture-unsafe test vectors are defined as unsafe faults. It is necessary to regenerate the test vectors used to detect unsafe faults in order to prevent unnecessary yield losses. In this paper, we propose a new low capture power test generation method based on fault simulation that uses capture-safe test vectors in an initial test set. Experimental results show that the use of this method reduces the number of unsafe faults by 94% while requiring just 18% more additional test vectors on average, and while requiring less test generation time compared with the conventional low capture power test generation method.

key words: *low power, test generation, capture safe test vectors, test vector synthesis, unsafe faults*

1. Introduction

With shrinking feature sizes, growing clock frequencies, and decreasing power supply voltage, modern integrated circuits are increasingly suffering from the impact of timing related defects, such as small delays [1]. At-speed scan testing based on the launch-on-capture (LOC) scheme [2] is widely used to detect timing related defects due to its simplicity, high fault coverage, and strong diagnostic support [3].

In a full-scan sequential circuit, all functional flip-flops (FFs) are replaced with scan FFs that operate in two modes: shift and capture. The shift mode is used to load a test vector into the scan FFs and to observe the test response. In the capture mode, scan FFs operate as functional FFs and capture the test response of the combinational portion for a test vector into themselves.

Test power in the shift mode is called shift power, while test power in the capture mode is called capture power. Excessive shift power might lead to circuit-damaging high temperatures, while excessive capture power can cause the excessive voltage (IR-drop) problem [4]. Since excessive IR-drop significantly increases path delay, and thus might result in timing errors, such testing induces unnecessary yield loss [5].

In this paper, we focus on the capture power problem for at-speed scan testing based on LOC. In at-speed scan testing based on LOC, it is important to reduce launch switching activity (LSA). Numerous LSA reduction methods, generally classified into circuit modification and test vector manipulation, have been proposed to date. Methods based on circuit modification [6]–[9] attempt to reduce capture power by modifying the circuit structures or by inserting some additional hardware in the circuit under test (CUT). In contrast, methods based on test vector manipulation [10]–[22] generate capture-safe test vectors [10] that will not consume excessive power during testing.

The test vector manipulation methods are generally classified into X-filling and test vector regeneration. The X-filling method assigns logic values (0 or 1) to the don't-care (X) bits in test cubes in order to minimize LSA. In [11]–[18], low-capture-power (LCP) X-filling methods are proposed. However, in these methods, it is hard to significantly reduce LSA when the specified bits used to detect faults in a test cube can, themselves, cause high LSA. For the above reasons, these methods depend on an initial test set.

In contrast, in test vector regeneration methods [19]–[22], test vectors are regenerated to satisfy the capture power constraint. These methods employ the conventional automatic test generation (ATG) procedure (like PODEM [23]) by adding the constraints for backtrack and dynamic compaction processes to directly generate LCP test sets. However, since these methods are based on complete deterministic algorithms, long test generation time and complex implementation are required.

Given a test set and a threshold value of capture power for LSA, test vectors are classified into capture-safe test vectors [10] and capture-unsafe test vectors [10]. Capture power values for LSA of capture-unsafe test vectors are more than the threshold value. Since capture-unsafe test vectors should not be used for at-speed low power scan testing, unsafe faults [10] which can only be detected by capture-unsafe test vectors remain undetected. It is important to reduce the number of unsafe faults to improve fault coverage.

In this paper, we propose a new low-capture-power test generation method for transition faults based on LOC. The method is based on fault simulation that uses capture-safe

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test vectors that have low LSAs in the initial test sets. The proposed test generation method uses fault propagation path information for capture-safe test vectors to generate new test vectors for unsafe faults. This simulation-based approach reduces the test generation time, and the simplicity of the proposed algorithm facilitates simple implementation.

The remainder of this paper is organized as follows: Sect. 2 describes the motivation behind this paper. Section 3 proposes the new low-capture-power test generation method. Section 4 shows our experimental results, and Sect. 5 concludes the paper.

2. Motivation

2.1 Capture Power Problem

To estimate LSA, several metrics have been proposed [20], [22]. Most previous studies use simple metrics due to the need for computation efficiency. For example, the toggle count metric considers node state changes (FFs or gates) while the launched weighted switching activity (WSA) metric considers both node state changes and the number of node fan-outs. In this paper, the WSA metric is used to estimate the LSA. The WSA value of a gate is defined as the number of transitions at that gate, which is multiplied by $(1 + fanout(g_i))$. If a transition occurs at gate g_i, $tran(g_i)$ is set to 1; otherwise $tran(g_i)$ is set to 0. The WSA value of an entire circuit for one test vector is the sum of the WSA value for each gate in the circuit, which is shown as follows:

$$WSA(v_j) = \sum_{i=1}^{G} tran(g_i) \times (1 + fanout(g_i))$$

In this equation, v_i represents the each test vector, and G represents the number of gates in the circuit.

We define capture-unsafe test vectors, capture-safe test vectors, a capture-unsafe test set, a capture-safe test set, unsafe faults, and safe faults using a test set T and a threshold value P_{th} of WSA before describing capture power problem.

(Definition 1: Capture-unsafe test vectors)
Given a test set T and a threshold value P_{th} of WSA, when the WSA value of a test vector in T is more than P_{th}, the test vector is defined as a capture-unsafe test vector. Otherwise, the test vector is defined as a capture-safe test vector.

(Definition 2: Capture-unsafe test set)
A set of capture-unsafe test vectors in T is defined as a capture-unsafe test set. While a set of capture-safe test vectors in T is defined as a capture-safe test set.

(Definition 3: Unsafe faults)
Faults which can only be detected by the capture-unsafe test set are defined as unsafe faults. While faults which can be detected by the capture-safe test set are defined as safe faults.

In at-speed scan testing, test vectors that violate capture power constraints are more likely to induce yield loss.

```
C : Circuit
fp : Flipped percentage of bits in primary inputs and pseudo primary inputs
analysis( C ){
1.  V = generate_random_vectors();
2.  for each vector v_i in V{
3.      before_i = WSA( C, v_i );
4.      v_i' = invert_bit( v_i , fp);
5.      after_i = WSA( C, v_i' );
6.  }
7.  return correlation_coefficient( BEFORE, AFTER );
}
```

Fig. 1 Procedure of preliminary experiment

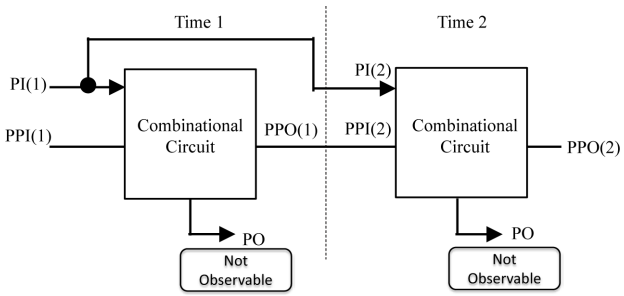

Fig. 2 LOC test generation model

This means, for the abovementioned reasons, those test vectors cannot be used for testing. Therefore, it is necessary to maximize the number of faults that can be detected by capture-safe test vectors, or, in other words, to minimize the number of unsafe faults. The capture-safe test generation problem can be formalized as follows:

Capture Safe Test Generation Problem:
(Input) a capture-safe test set T_{safe} and a capture-unsafe test set T_{unsafe}
(Output) a final test set T' that the WSA values of each test vector are equal or less than P_{th}
(Constraint) a threshold of WSA value P_{th}
(Optimization) minimizing the number of unsafe faults

2.2 Test Vector Manipulation and Capture Power

We evaluated the changes of WSA values for LSA by test vector manipulation. We conducted a preliminary experiment, the procedure for which is shown in Fig. 1.

In Fig. 1, an initial vector set V is randomly generated (Step 1). In this experiment, the number of initial vectors is 1024. For each test vector in V, steps 3 to 5 are the iteration phase. In step4, we randomly flipped specified percentage (fp) of bits, and the WSA values obtained before and after test vector manipulation are calculated. Finally, the correlation coefficient of WSA values obtained before and after test vector manipulation is calculated (Step 7).

Figure 2 shows a test generation model [2] of a transition fault for at-speed scan testing based on LOC. A scan

design circuit is unrolled into a 2-time expansion model. In Fig. 2, PI denotes primary inputs, PO denotes primary outputs, PPI denotes pseudo primary inputs (the outputs of scan flip-flops), and PPO denotes pseudo primary outputs (the inputs of scan flip-flops). The numbers of the parenthesis denote time. In this model, PI(1) and PPI(1) are controllable, and PPO(2) is observable. A test vector is set to PI(1) and PPI(1). A test response is observed at PPO(2). The values of PI(1) are set to PI(2). The values of PPO(1) are set to PPI(2). PO(1) and PO(2) are not observable.

The results obtained utilizing the ISCAS'89 and ITC'99 benchmark circuits are summarized in Table 1. In this table, "#of PI+PPI" and "correlation coefficient" denotes the number of (pseudo) primary inputs and the correlation coefficient of WSA values before and after test vector manipulation, respectively.

In this experiment, the bit flip ratios were set as 5, 10, 20, and 30%, and the correlation coefficient of before and after test vector manipulation is given by the following equation.

$$CC = \frac{\sum_{i=1}^{n}(before_i - \overline{before})(after_i - \overline{after})}{\sqrt{\sum_{i=1}^{n}(before_i - \overline{before})^2}\sqrt{\sum_{i=1}^{n}(after_i - \overline{after})^2}}$$

In this equation, $before_i$ and $after_i$ represent the WSA of before and after test vector manipulation, $\overline{before}$ and $\overline{after}$ are the WSA average before and after test vector manipulation and n represents the number of random vectors. As shown in Table 1, the WSA correlation coefficients before and after test vector manipulation were both close to 1.0 when the flipped bit ratios were very small. Therefore, we consider it likely that the after test vector manipulation WSA values correlate with the before test vector manipulation WSA values when the ratios of flipped bits are very small. We consider that test vectors generated by test vector manipulation using capture-safe test vectors is more likely to be capture-safe if the ratios of flipped bits are very small. The preliminary experimental results motivated us to propose a new capture-safe test generation method is based on test vector manipulation using capture-safe test vectors.

Table 1 Correlation coefficient for WSA values before and after vector manipulation

Circuit	# of PI+PPI	correlation coefficient(CC)			
		5% inverted	10% inverted	20% inverted	30% inverted
s5378	214	0.82	0.64	0.39	0.25
s9234	247	0.85	0.71	0.43	0.26
s13207	700	0.85	0.74	0.48	0.33
s15850	611	0.83	0.69	0.45	0.25
s35932	1763	0.86	0.75	0.54	0.34
s38417	1664	0.81	0.62	0.39	0.21
s38584	1464	0.88	0.79	0.57	0.35
b14	277	0.91	0.84	0.75	0.73
b15	485	0.77	0.66	0.38	0.22
b17	1452	0.78	0.60	0.37	0.20
b18	3357	0.81	0.64	0.45	0.26
b19	6666	0.80	0.67	0.46	0.29
b20	522	0.80	0.69	0.53	0.42
b21	522	0.80	0.68	0.53	0.41
b22	767	0.80	0.70	0.50	0.38

3. Proposed Test Generation Method

3.1 Main Idea

In this section, we describe the main idea behind the proposed capture-safe test generation method. Figure 3 shows the concept. A test cube that detects a fault is roughly classified into assignments for fault excitation and assignments for fault propagation. In this paper, the (pseudo) primary input values for fault excitation are defined as a fault excitation cube, while those for fault propagation are defined as a fault propagation cube. Hence, a new test vector can be generated by synthesizing a fault excitation cube and a fault propagation cube. In Fig. 3, the fault excitation cube (X, 1, X, 0, X) and the fault propagation cube (1, 1, X, X, 0) are synthesized and a new test cube (1, 1, X, 0, 0) that can detect a target fault f, is generated. In this test generation method, the fault excitation cubes are extracted from capture-unsafe test vectors in an initial test set that detects a target unsafe fault f. We conjectured that the number of specified bits required for a fault excitation cube is very small. Based on the results of our experiments in Sect. 4, we found that the number of specified bits required for a fault excitation cube was only 5 to 10% of the (pseudo) primary inputs for many circuits on average. On the other hand, capture-safe test vectors that can propagate the fault effect to pseudo primary output are used as for the fault propagation cube. Thus, from the preliminary experimental results, even if a capture-safe test vector is modified by test vector synthesis with a fault excitation cube, the modified test vector could probably keep capture-safe.

3.2 Overview of Proposed Test Generation Method

As shown in Fig. 4, the whole algorithm of the proposed capture-safe test generation method is composed of test vector synthesis base on fault simulation and static test compaction.

The capture-safe test set T_{safe} and the capture-unsafe test set T_{unsafe} are identified from an initial test set T, are given. As can be seen in the figure, the target unsafe fault set F_{target} is first obtained in Step 1. Then, for each fault f_i in F_{target}, test vector synthesis based test generation are

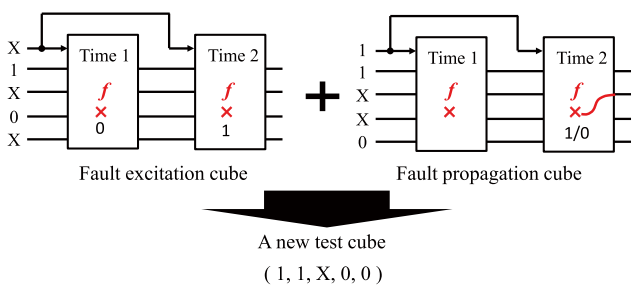

Fig. 3 Concept of the proposed method

```
C : Circuit
T_safe : Capture Safe Test Set
T_unsafe : Capture Unsafe Test Set
test_generation( C, T_safe, T_unsafe ){
1.   F_target = target_fault_selection( C, T_safe, T_unsafe );
2.   for each fault f_i in F_target {
3.     v' = synthesis_based_test_generation( C, T_safe, T_unsafe, f_i );
4.     If (v' != φ) {
5.       F_target = fault_simulatiuon( C, v' , F_target);
6.       T_gen = T_gen ∪ v';
7.     }
8.   }
9.   T_comp = static_test_compaction( C, T_gen );
10.  T' = T_comp ∪ T_safe;
}
```

Fig. 4 Whole algorithm of capture safe test generation

Table 2 Example of Target Fault Identification

WSA	T	f1	f2	f3	f4	f5	f6	f7	f8	f9	f10
unsafe	tp1	●	●	○							
unsafe	tp2		●	○	○						
safe	tp3			○	○	○	○				
safe	tp4						○	○	○		
safe	tp5								○	○	○

performed (Steps 2-8). If a capture-safe test vector v' is generated, fault simulation is performed, detected faults are deleted from F_{target}, and v' is added into T_{gen} (Step 4-7). Then, static test compaction is performed (Step 9). Finally, the test set T' is obtained from the union of T_{comp} and T_{safe} (Step 10).

3.3 Target Fault Selection

In the proposed test generation method, only those faults that are detected by capture-unsafe test vectors are identified as a target unsafe fault set F_{target}. Table 2 shows an example of target fault identification. In this table, the initial test set is $T = \{tp1, tp2, tp3, tp4, tp5\}$. Now, let's suppose that tp1 and tp2 are capture-unsafe test vectors, and tp3, tp4, and tp5 are capture-safe test vectors. Thus, $T_{unsafe} = \{tp1, tp2\}$, and $T_{safe} = \{tp3, tp4, tp5\}$. The fault simulation result by T is also shown in Table 2. In Table 2, a circle in a row *tpi* and a column *fj* shows that a fault fj is detected by a test vector tpi. The set of faults that are only detected by test vectors in T_{unsafe} is $F_{target} = \{f1, f2\}$.

3.4 Test Vector Synthesis Based Test Generation

In this section, we describe the algorithm of the test vector synthesis based capture safe test generation method, an outline of which is shown in Fig. 5. As can be seen in the figure, first, the fault excitation cube t_{ex} is extracted from a capture-unsafe test vector that can detect the target unsafe fault f_{target} (Step1). The capture-safe test vector t_{base} is selected in a way that ensures the propagation for the fault

```
C : Circuit
T_safe : Capture Safe Test Set
T_unsafe : Capture Unsafe Test Set
f_target : Target Unsafe Fault
synthesis_based_test_generation( C, T_safe, T_unsafe, f_target ){
1.   t_ex = get_fault_excitation_cube( T_unsafe, f_target );
2.   while(( t_base = select_reuse_test_vector( T_safe, f_target )) exists ){
3.     t_gen = test_vector_synthesis( t_base, t_ex );
4.     WSA( C, t_gen );
5.     fault_simulation( C, t_gen, f_target );
6.     if( t_gen is capture-safe && t_gen detects f_target ){
7.       return t_gen;
8.     }
9.   }
10.  return φ;
}
```

Fig. 5 Flow of synthesis based test generation method

effect of f_{target} to the pseudo primary outputs (Step2). Steps 2 to 9 are iterated until t_{base} does not exist. If t_{base} is selected, it generates a new test vector t_{gen}, which is synthesized from t_{base} and t_{ex} (Step3).

WSA value of t_{gen} is calculated, and fault simulation is then performed to determine whether t_{gen} can detect f_{target} or not (Step4-5). If t_{gen} is a capture-safe test vector and can detect the target fault f_{target}, t_{gen} is returned as a new test vector (Step6-8). Otherwise, go to Step2. When the test generation fails to generate a capture-safe test vector, the test vector synthesis based test generation method returns ϕ (Step10).

Fault Excitation Cube Extraction

The extraction of a fault excitation cube is similar to X-identification [24], in that assignments to excite the target unsafe fault f_{target} are identified via path tracing. We extract fault excitation cubes based on fanout-free regions. A fanout-free region is a combinational circuit part with a single output where any fanout is not included. Faults in a fanout-free region certainly pass through the output of that to be detected at pseudo primary outputs. Therefore, a fault excitation cube must not only excite f_{target}, but also propagate the fault effect to the output of a fanout-free region which includes the fault site. Let FFR_{target} be the fauout-free region where f_{target} exists. In the fault excitation cube extraction step, only assignments to excite target fault f_{target} and propagate a fault effect to the output of FFR_{target} are extracted. Figure 6 shows an example of fault excitation cube extraction. As can be seen in the figure, the fault excitation cube of the target unsafe fault f_{target} is (X, 1, 0, X, X, X).

Capture-Safe Test Vector Selection

Figure 7 shows an example of capture-safe test vector selection. As can be seen in the figure, there are two capture-safe test vectors. The test vector t_{base} must satisfy the following conditions:

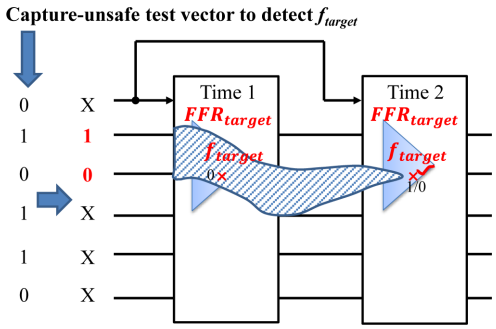

Fig. 6 Example of fault excitation cube extraction

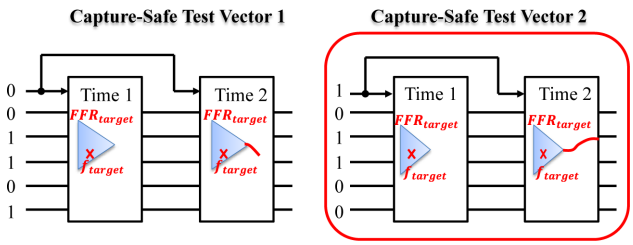

Fig. 7 Example of capture-safe test vector selection

Table 3 Operation for Test Vector Synthesis

t_{base} \ t_{ex}	0	1	X
0	0	1	0
1	0	1	1

Condition-1: t_{base} is a capture-safe test vector.
Condition-2: When defining FFR_{target} as a fan-out free region, including a signal of target unsafe fault f_{target}, a fault effect on the output signal of FFR_{target} can be propagated to pseudo primary outputs.

Since f_{target} exists in FFR_{target}, if a capture-safe test vector can propagate a fault effect to an output signal of FFR_{target}, we consider it likely that f_{target} can be detected by a test vector that is generated from the capture-safe test vector manipulation. As described in Sect. 2, bit manipulation of a test vector by 5∼10% has a limited effect on its WSA value. Therefore, it is highly probable that the generated test vector is capture-safe.

In Fig. 7, Capture-Safe Test Vector 2 is selected as t_{base} since the fault effect on the output of FFR_{target} is propagated to the pseudo primary output by the test vector. Note that, if there are more than one t_{base} candidates, a test vector with the minimum WSA value is selected.

Test Vector Synthesis

In this step, a new test vector is generated from the operation of a capture-safe test vector (t_{base}) and a fault excitation cube (t_{ex}), as shown in Table 3. Figure 8 shows an example of test vector synthesis. The fault excitation cube

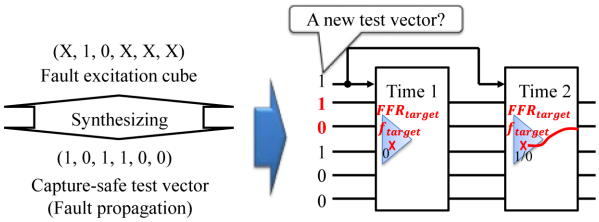

Fig. 8 Test Vector Synthesis

of the target unsafe fault f_{target} is (X, 1, 0, X, X, X), and the capture-safe test vector t_{base} is (1, 0, 1, 1, 0, 0). As the result of the test vector synthesis operation, a new test vector (1, 1, 0, 1, 0, 0) is generated. Note that detection of f_{target} and capture-safety by the new test vector are not guaranteed.

3.5 Static Test Compaction

The proposed static compaction method is based on double detection [25]. For original double detection, the order of test vectors is determined as follows: Test vectors that can detect essential faults [25] are simulated first. Next, other test vectors are simulated in reverse order. In the proposed static compaction method, first, test vectors that can detect essential faults are simulated. Next, fault simulation by other test vectors is performed in the ascending order of WSA values.

4. Experimental Results

The proposed method was implemented in the C language and experiments were conducted on ISCAS'89 and ITC'99 benchmark circuits that could generate a complete test set with 100% fault efficiency in realistic time using 3.4-GHz Intel Core i7 4770 central processing unit (CPU) with 8 GB of memory on Windows 8.1 operating system. We did not evaluated b18, b19, b20, b21 and b22 since ATG tool terminated with remaining aborted faults in realistic time. Since the Synopsys TetraMAX power-aware ATG for transition faults supports a low-capture-power test generation mode, we compared the results of that system with the experimental results obtained using our proposed method. TetraMAX was performed using 3.5-GHz Intel Xeon E3-1280 CPU with 16 GB of memory on SUSE operating system. We could not give the threshold value of WSA to TetaMAX. We could give the threshold value of the ratio for flip-flops with transition to TetraMAX. TetraMAX could also generate test vectors with the minimum number of transitions on flip-flops in the low-capture-power test generation mode. We firstly tried the former. We set the threshold value to 20, 30, 40, and 50. TetraMAX identified many faults as undetectable fault under the constraints for benchmark circuits. It was difficult to determine the appropriate threshold value. Therefore, we finally used the latter. The test set for transition fault model was generated by our in-house Boolean Satisfiability (SAT)-based ATG tool. After that, the static test compaction described in 3.5, X-identification [24] and

Table 4 Initial test set

Circuits	#Det	Max_WSA	#Vec	#Safe_vec	#Unsafe_vec	#Unsafe_flt	Thr
s5378	6546	1588	223	211	12	156	1111.6
s9234	13813	2513	581	510	71	519	1759.1
s13207	19261	2742	627	575	52	372	1919.4
s15850	20009	3218	498	490	8	120	2252.6
s35932	49278	12486	113	91	22	4922	8740.2
s38417	73736	11746	1307	1261	46	2688	8222.2
s38584	50138	6428	1820	1807	13	1448	4499.6
b14	40115	10623	1696	1473	223	1551	7436.1
b15	34298	4777	1644	1459	185	1565	3343.9
b17	119436	14093	4936	4862	74	723	9865.1

Table 5 Experimental results for the number of unsafe faults and test generation time

Circuits	Ini_unsafe_flt	Fin_unsafe_flt		Reduction_ratio_unsafe_flt (%)		Tgen_time (s)	
		Proposed	TetraMAX	Proposed	TetraMAX	Proposed	TetraMAX
s5378	156	0	156	100.00	0.00	0.19	0.12
s9234	519	49	493	90.56	5.01	4.55	50.39
s13207	372	2	358	99.46	3.76	3.20	25.96
s15850	120	0	120	100.00	0.00	1.62	2.05
s35932	4922	0	4922	100.00	0.00	80.17	0.65
s38417	2688	8	2673	99.70	0.56	449.59	39.00
s38584	1448	0	1448	100.00	0.00	77.75	0.84
b14	1551	182	740	88.27	52.29	107.71	7768.30
b15	1565	519	692	66.84	55.78	1727.20	833.45
b17	723	4	245	99.45	66.11	2281.17	5157.52

JP-fill [13] that was a don't care filling method for low capture power were applied to the test set. The generated test set was regarded as the initial test set. In [10], the threshold value used to identify the capture-unsafe test vectors was set to 90% of the maximum capture-power metric values in the initial test set, and in [21], the threshold values were set to 15% and 20% of the theoretical maximum WSA values which was calculated when transitions occurred on all signal lines in a circuit. In this experiments, the threshold value used to identify the capture-unsafe test vectors was set to 70% of the maximum WSA values in the initial test set.

Table 4 shows the information of initial test sets. In this table, "Circuits" denotes the circuit name, "#Det" denotes the number of detected faults, "Max_WSA" denotes the maximum WSA value in the initial test set, "#Vec" denotes the number of test vectors, "#Safe_vec" denotes the number of capture-safe test vectors, "#Unsafe_vec" denotes the number of capture-unsafe test vectors, "#Unsafe_flt" denotes the number of unsafe faults, and "Thr" denotes the threshold value of WSA used to identify the capture-unsafe test vectors. The ratios of unsafe faults to detected faults were 0.6 to 10.0%.

The experimental results for the number of unsafe faults and the test generation times are summarized in Table 5. In this table, "Circuits" denotes the circuit name, the "Ini_unsafe_flt" denotes the number of unsafe faults in the initial test set, "Fin_unsafe_flt" denotes the number of unsafe faults after capture-safe test generation is applied to initial unsafe faults, "Reduction_ratio_unsafe_flt" denotes $\frac{(Ini\_unsafe\_flt - Fin\_unsafe\_flt)\times 100}{Ini\_unsafe\_flt}$, and "Tgen_time" denotes test generation time for the initial unsafe faults. "Proposed" and "TetraMAX" denote the experimental results of our proposed test generation method and TetraMAX power-aware ATG, respectively. The fault efficiencies of the initial test sets for a transition fault model were 100%. The proposed method reduced the numbers of capture-unsafe faults by 94% on average. In contrast, TetraMAX reduced the number of capture-unsafe faults by 15% on average. This means that our proposed method can easily detect unsafe faults under given capture power constraints. As can be seen in the table, the proposed method reduced the test generation time about 72 times as the maximum, compared with TetraMAX. Since the proposed test generation method is based on fault simulation, we consider that the proposed method would be effective for large circuits.

Table 6 shows the experimental results for the number of test vectors before and after the application of our proposed method. In this table, "Circuits" denotes the circuit name, "Ini_safe_vec" denotes the numbers of capture-safe test vectors in the initial test sets, "Add_safe_vec" denotes the number of capture-safe test vectors generated by the proposed capture-safe test generation, "Fin_safe_vec" denotes Ini_safe_vec + Add_safe_vec, "Fin_safe_vec_DD" denotes the number of final capture-safe test vectors after the static test compaction is applied, "Ini_vec" denotes the number of initial test vectors, and "Increase_ratio_testvec" denotes $\frac{(Fin\_safe\_vec - Ini\_vec)\times 100}{Ini\_vec}$. As can be seen in Table 6, the proposed capture-safe test generation method generated additional test vectors by 1 to 49% for the circuits (except for s35932) compared with the numbers of capture-safe test

Table 6 Experimental results for the number of test vectors

Circuits	Ini_safe_vec	Add_safe_vec	Fin_safe_vec	Fin_safe_vec_DD	Ini_vec	Increase_ratio_testvec(%)
s5378	211	66	277	266	223	19.28
s9234	510	159	669	635	581	9.29
s13207	575	182	757	724	627	15.47
s15850	490	28	518	506	498	1.61
s35932	91	1305	1396	1094	113	868.14
s38417	1261	939	2200	1958	1307	49.81
s38584	1807	435	2242	2183	1820	19.95
b14	1473	580	2053	1796	1696	5.90
b15	1459	405	1864	1670	1644	1.58
b17	4862	356	5218	5023	4936	1.76

Table 7 Experimental results for fault excitation cube and test generation success

Circuits	Ave (%)	Min (%)	Max (%)	Mode (%)	#PI+#PPI	#Try	#Suc	#Fail	Success_ratio_testgen (%)
s5378	7.21	0.93	30.37	0.93	214	66	66	0	100.00
s9234	8.59	0.40	24.70	8.50	247	228	159	69	69.74
s13207	1.76	0.29	5.00	0.71	700	187	182	5	97.33
s15850	5.39	0.33	8.84	8.84	611	28	28	0	100.00
s35932	0.39	0.11	1.30	0.40	1763	1305	1305	0	100.00
s38417	0.45	0.06	3.25	0.12	1664	964	939	25	97.41
s38584	0.63	0.07	6.83	0.20	1464	436	435	1	99.77
b14	18.19	1.81	63.90	17.69	277	797	580	217	72.77
b15	20.77	0.62	40.21	18.56	485	1009	405	604	40.14
b17	6.68	0.21	17.15	0.34	1452	382	356	26	93.19

vectors in the initial test sets. We need to study a dynamic test compaction method for capture-safe test generation to reduce the number of capture-safe test vectors.

Table 7 shows the experimental results for fault excitation cubes and the number of the success in test generation. In this table, "Circuits" denotes the circuit name, "Ave" denotes the average ratio of care bits in fault excitation cubes, "Min" denotes the minimum ratio of care bits, "Max" denotes the maximum ratio of care bits, "Mode" denotes the mode value for the ratio of care bits, "#(PI+PPI)" denotes the number of primary inputs and pseudo primary inputs, "#Try" denotes the number of test generation for initial unsafe faults, "#Suc" denotes the number of the success in test generation, "#Fail" denotes the number of the failure in test generation, and "Success_ratio_testgen" denotes $\frac{Suc \times 100}{Try}$. The ratios of care bits in fault excitation cubes were 0.39 to 20.77% on average. The ratios were less than 10% for all circuits except for b14 and b15. Thus, the ratios of the success in capture-safe test generation were 69 to 100% for all circuits except for b14 and b15. We consider that the ratios (93 to 100%) were high except for s9234. On the other hand, the ratios of care bits in fault excitation cubes were 18.19 and 20.77 for b14 and b15, respectively. The ratios of the success in capture-safe test generation were 72 and 40% for b14 and b15, respectively. Since the ratios of care bits in fault excitation cubes were high, we consider that the ratios of the success in capture-safe test generation were low.

5. Conclusion

In this paper, we proposed a simulation based test generation method that works by manipulating capture-safe test vectors. Our results show that the proposed test generation method could reduce the number of unsafe faults by an average of 94% while only requiring an average of 10% more test vectors for the circuits (except for s35932) than the initial test set. We also found that proposed test generation method could reduce test generation time about 72 times, based on the of ITC'99 benchmark circuit average as compared with TetraMAX.

Our future work will include developing an effective dynamic test compaction method.

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