FOREWORD

Special Section on Multiple-Valued Logic and VLSI Computing

Welcome to this Special Section on "Multiple-Valued Logic and VLSI Computing." The papers in this section are extended versions of the abstracts presented at the IEEE 46th International Symposium on Multiple-Valued Logic (ISMVL 2016), which was held in Sapporo, Japan on May 18–20, 2016, and include a substantial amount of information beyond the presentations. The purpose of this Special Section is to share an overview of recent research progress in various aspects relating to post-binary and non-standard VLSI computing paradigm with many readers of this transaction, who are interested in innovative new-concept-based VLSI computing and its applications. This Special Section consists of two invited and 9 contributed papers. The first invited paper is on BDD/ZDD-Based Techniques for Discrete Structure Manipulation and their practical applications, while the second one describes a novel biomimetics image retrieval platform. In the former paper, it is demonstrated that multiple-valued data representation and its operation are powerful to enumerate data processing, which is useful for realizing an efficient and powerful data-retrieval system. The latter paper points out the promising candidate of novel application fields using multiple-valued computing techniques. The contributed papers cover a broad range from logic design, VLSI architecture, communication for VLSI, and circuit implementations and soft computing applications to Intelligent Medical and Welfare Engineering. We would like to thank all the authors of invited and contributed papers for their efforts in preparing the manuscripts, and the reviewers who worked diligently to make sure that the papers are worth publication.

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Takahiro Hanyu *(Senior Member)* received the B.E., M.E. and D.E. degrees in Electronic Engineering from Tohoku University, Sendai, Japan, in 1984, 1986 and 1989, respectively. He is currently a Professor and a deputy director (2016–2017) in the Research Institute of Electrical Communication, Tohoku University. His general research interests include nonvolatile logic circuits and their applications to ultra-low-power and/or highly dependable VLSI processors, and post-binary computing hardware algorithm and its application to brain-inspired VLSI systems. He received the Sakai Memorial Award from the Information Processing Society of Japan in 2000, the Judge's Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002, the Special Feature Award at the University LSI Design Contest from ASP-DAC in 2007, the APEX Paper Award of Japan Society of Applied Physics in 2009, the Excellent Paper Award of IEICE, Japan, in 2010, Ichimura Academic Award in 2010, the Best Paper Award of IEEE ISVLSI 2010, the Paper Award of SSDM 2012, the Best Paper Finalist of IEEE ASYNC 2014, and the Commendation for Science and Technology by MEXT, Japan in 2015. Dr. Hanyu is a Senior Member of the IEEE.