FOREWORD

Special Section on Parallel and Distributed Computing and Networking

The technology of parallel- and distributed- computing and networking is fundamental in the coming Big-data and Internet-of-Things (IoT) era, in which enormous amount of data generated by trillions of IoT devices will be collected and aggregated on distributed computing and networking systems to extract 'valuable' information from data for human beings. The key enabling technologies in the era include network-on-chip, image processing, data mining, green computing, cluster/grid systems, distributed network storage, cloud and distributed computing, and ubiquitous/mobile computing, all of which could be applications of algorithms and system architectures covered by the field of parallel- and distributed- computing and networking.

This special section brings together high-quality and timely papers on the recent progress in the interdisciplinary area of parallel- and distributed- computing and networking. These papers include the extended versions of conference papers presented at the International Symposium on Computing and Networking (CANDAR'15) and the International Symposium on Embedded Multicore/Many-core System-on-Chip (MCSoC'15), in addition to bland-new contributions from our IEICE members.

The submitted papers to this section were 34 papers and 2 letters, which were from six countries: 27 from Japan, 4 from China, 2 from Korea, 1 from Taiwan, 1 from Iran, and 1 from Brazil. Through the fair and strict reviewing process by expert reviewers, 17 papers were finally accepted for publication. We had received a lot of interesting papers but did not accept some of them unfortunately, because manuscripts that require major revisions need to be rejected, which is the editorial policy of IEICE transactions. We hope the improved versions of these manuscripts will appear in the future publications of IEICE transactions.

It was my honor to serve as the guest editor-in-chief of this special section. I first would like to thank all of the authors who submitted their papers to this section for their contributions. I also wish to express my gratitude to all the reviewers and the guest associate editors for their efforts. Finally, I am most grateful to guest editors, Dr. Fumihiko Ino and Dr. Ryoichi Shinkuma, for their devotions to this special section.

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Yasuhiko Nakashima (Nara Institute of Science and Technology), Guest Editor-in-Chief

Yasuhiko Nakashima (*Senior Member*) received B.E., M.E. and Ph.D. degree in Computer Engineering from Kyoto University in 1986, 1988 and 1998 respectively. He was a computer architect in the Computer and System Architecture Department, FUJITSU Limited from 1988 to 1999. From 1999 to 2005, he was an associate professor in Graduate School of Economics, Kyoto University. Since 2006, he has been a professor in the Graduate School of Information Science, Nara Institute of Science and Technology. His research interests include computer architecture, emulation, circuit design, and accelerators. He is a member of IEEE CS, ACM and IPSJ.