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PAPER

Analysis of Body Bias Control Using Overhead Conditions for Real Time Systems: A Practical Approach*

Carlos Cesar CORTES TORRES[†a)], ***Nonmember***, **Hayate OKUHARA**[†], ***Student Member***, **Nobuyuki YAMASAKI**[†], ***Member***, ***and*** **Hideharu AMANO**[†], ***Fellow***

SUMMARY In the past decade, real-time systems (RTSs), which must maintain time constraints to avoid catastrophic consequences, have been widely introduced into various embedded systems and Internet of Things (IoTs). The RTSs are required to be energy efficient as they are used in embedded devices in which battery life is important. In this study, we investigated the RTS energy efficiency by analyzing the ability of body bias (BB) in providing a satisfying tradeoff between performance and energy. We propose a practical and realistic model that includes the BB energy and timing overhead in addition to idle region analysis. This study was conducted using accurate parameters extracted from a real chip using silicon on thin box (SOTB) technology. By using the BB control based on the proposed model, about 34% energy reduction was achieved.

key words: *silicon-on-insulator, SOTB, body bias, low power design, time-overhead, energy-overhead*

1. Introduction

Real-time systems (RTSs) are part of our daily lives; they are used in different domains, such as home appliances, medical systems, robotics, security, aeronautics, and many others. One class of these systems is used for highly time-critical tasks that should be executed in a predefined deadline. When failing to meet this deadline, the executed task's results can be corrupted, or even the entire system might fail, possibly leading to catastrophic consequences.

At the same time, and with the increasing popularity of Internet of Things (IoT), the need to design RTSs that can be embedded in small devices has become a necessity. Also, these types of embedded RTSs require a long lasting battery life and should operate on a limited power budget. As technology continues to scale, the leakage current will keep increasing, and a strict control is needed to find an optimal operational region. Hence, the energy consumption should be kept minimum while making sure that the timing constraints are met.

The RTS energy efficiency has been extensively studied, and some have focused on very-large-scale integration (VLSI) designs. Various techniques, including power gating (PG) [1] for dynamic power management (DPM) [2], and dynamic voltage scaling (DVS) [3] have been introduced in RTSs. These techniques can improve energy efficiency; however, they often require a large amount of power since they must control the supply voltages of the systems.

Body bias (BB) control is another solution that can improve RTS energy efficiency as it can manage the tradeoff between power leakage and performance without affecting the power supply [4], [5]. Its effect is further endorsed when systems are enabled with silicon on thin box (SOTB) technology [6], which is a novel and advanced fully depleted silicon on insulator (FD-SOI) technology. Thus, combining the benefits of SOTB and adaptive BB can drastically suppress the leakage current. However, when controlling the BB on RTSs, the BB must be controlled dynamically so as not to miss the deadline. Although the energy for statically maintaining the BB voltage is quite small, the dynamic control of the BB requires considerable energy. Although several studies on dynamic BB control have been conducted [4], [7], [8], they were not based on accurate real-chip measurements that include the BB switching-voltage overhead.

Based on the above, we investigated RTS energy efficiency by analyzing the dynamic BB control on performance and energy, including the physical energy and timing overheads when executing the voltage transitions. To this aim, we propose a practical timing and a power mathematical models capable of determining the energy consumption based on the task execution while taking into account a given deadline constraint. Thus, the contributions of this paper can be outlined as follows:

- The timing and energy overheads when switching the BB voltages are measured with a real microcontroller implemented with SOTB technology.
- By using these measurements, a practical power model for scaling the BB according to the switching behavior, operational frequency, clock cycles per instruction (CPI), and time for a deadline is proposed. The proposed model can calculate the energy consumption for each task of a given RTS application.
- The energy saved with the proposed model is analyzed.

This paper is organized as follows. Section 2 provides a background of studies related to energy optimization in RTSs. Sections 3 and 4 are dedicated to explaining our timing and power models. The evaluation setup and results are presented, analyzed, and discussed in Sects. 5 and 6. Finally, Sect. 7 summarizes the findings and outlook of this paper.

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[†]The authors are with the Department of Information and Computer Science, Keio University, Yokohama-shi, 223–8522 Japan.

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a) E-mail: cortesc@am.ics.keio.ac.jp

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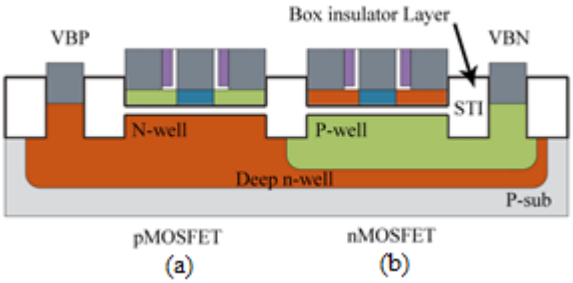


Fig. 1 Cross-sectional view of SOTB MOSFET: (a) pMOS and (b) nMOS

2. Body Bias Control

2.1 Silicon on Thin Box

An SOTB is a FD-SOI device [6]. It has benefits of latch-up immunity, superior high temperature, performance, radiation hardness, and high BB sensitivity. These characteristics are possible due to its insulating "buried oxide" layer widely used in SOI devices [9], [10]. These body-driven characteristics enable high caliber energy reduction using the BB. Unlike other conventional FD-SOI devices, a SOTB device is formed on an ultra-thin box layer (about 10 nm), as shown in Fig. 1, enabling a wide range of BB control. Consequently, SOTB ensures more efficient reduction in leakage current using BB control than other conventional metal-oxide-semiconductor field-effect transistors (MOSFETs).

We denote the BB voltage of nMOS as VBN, that of pMOS as VBP, and supply voltage as VDD. As other FD-SOI technologies, the default state of a given MOSFET (VBN = 0 and VBP = VDD) in SOTB is called zero body bias (ZBB). If a lower voltage is applied to the nMOS body (VBN < 0) and higher voltage is applied to the pMOS body (VBP > VDD), the depletion width increases; hence, the threshold voltage increases. This condition is known as reverse body bias (RBB). In contrast, if a higher voltage is applied to the nMOS body (VBN > 0) and a lower voltage is applied to the pMOS body (VBP < VDD), the depletion width decreases; thus, the threshold voltage decreases. This condition is known as forward body bias (FBB).

The FBB can achieve high operating speeds, increasing the performance at the cost of leakage current, while the RBB reduces performance and leakage current at the price of gate delay. Although the RBB for RTSs is useful in reducing the leakage current in the sleep mode, the timing and values must be carefully controlled so as not to miss the deadline.

2.2 Related Work

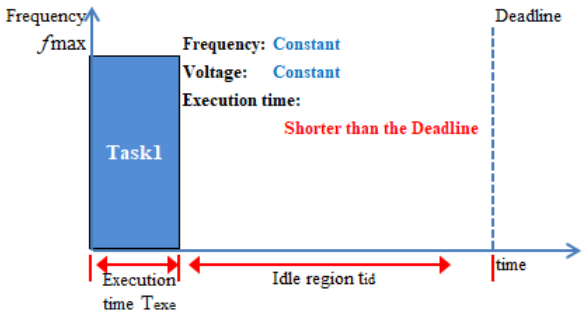
A significant number of studies have been carried out to enhance the energy efficiency in embedded RTSs. The DPM is a technique that reduces the energy dissipation of RTSs with low power idle states [2]. However, under the condition that a power supply is cut-off for idle states, volatile data are discarded. When data need to be preserved, a certain level of voltage has to be supplied as a power supply. Hence, power-leakage reduction is restricted to such conditions. The DVS is a technique that decreases the power supply voltage while keeping application deadlines [3]. It can drastically reduce the dynamic power due to the quadratic power-supply dependency. However, the range for power-supply scaling is highly restricted when the power supply voltage is near the threshold region [11]. Such limitations can drastically impact the efficiency of energy saving.

Some studies have analyzed the benefits of combining DVS and adaptive BB for energy reduction [4], [7]. Yan et. al. proposed a task-scheduling algorithm and energy models for RTSs usage [4]. These models can calculate an optimal power supply and BB voltage for each operational frequency. By using the obtained voltages, the algorithm schedules a task so as not to violate the deadline. Namely, the authors assume ideal voltage regulators that can output any voltage obtained from the models. However, the actual voltage drivers have a certain limitation in terms of output-voltage resolution. Akgul et. al. proposed a power-management method considering these voltage constraints [7]. The authors assumed discrete power-supply voltages and succeeded to reduce the energy even under the restrictions mentioned earlier. However, these studies did not treat actual overheads of BB control, which also has energy consumption and switching delay.

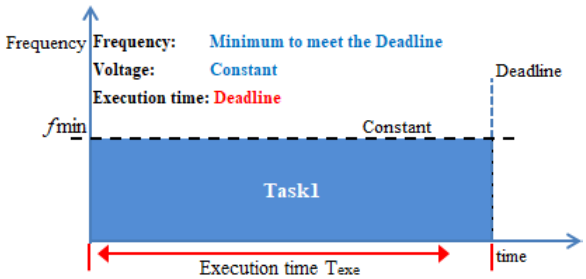
Several works have been proposed to improve energy efficiency. When considering overhead conditions or analyzing idle regions, however, all these approachesare at circuit level [12]–[14]. In our previous study [5], [8], we developed a power model using BB control. The model is based on real-chip measurements in terms of leakage current, switching current, and maximum operational frequency. However, ideal BB switching is also assumed. Hence, to the best of our knowledge, none of the studies presented above incorporated these timing and energy overhead conditions in their energy-saving approaches targeted for RTSs.

3. Proposed Model

Without power-saving control, a task is executed in time t_{op} and finishes at the given deadline. The frequency and voltage are constant all through the deadline. Hence, the power leakage consumed in the idle region is wasted, as shown in Fig. 2 (a). To reduce power leakage, most conventional models lower or shut down the power supply in the idle time. However, this requires a power-management circuit for controlling power supply, which requires a certain amount of current. Also, when the power gating is used, the data in the storage are lost without special mechanisms to save them. They are sometimes too heavy for tiny RTSs used for IoT. Instead, we investigated power-leakage control using the BB. Specifically, when the SOTB is used, power leakage with the strong RBB is extremely low, yet all



(a) Conventional Real Time Execution



(b) Frequency scaling

Fig. 2 Conventional real-time execution. (a) The frequency and voltage are set to maximum, so task finishes in period shorter than the deadline, frequency and voltage remain constant, and power is wasted at idle region. (b) Frequency scale is set to minimum and remains constant, which allows task to finish at deadline, saving power.

data in the memory and registers are kept. Since the static power required for maintaining the BB is also small, it can be controlled by straightforward low-power circuits using the charge pump [15]. The power-supply voltageand clock frequency can be adjusted for each application but assumed to be constant during the execution. Since the clock gating is applied during the idle time, the dynamic power during this time is assumed to be zero.

In this paper, we focus on two possible scenarios to execute a given task on an RTS while considering a predefined deadline. In the first scenario, the system works at the minimum frequency at which the task execution finishes at the deadline. This means that the minimum VDD and ZBB voltages are supplied. This scenario is our baseline. The second scenario, shown in Fig. 3, consists of optimizing the VDD to boost the frequency according to the alpha power law; hence, the task is executed in much less time than the first scenario. During the remaining time until the deadline, we apply the RBB to reduce power leakage. The goal of this study was to obtain optimized VDD and RBB control for a given task and deadline.

We first present the RTSs timing model followed by our power and energy model to illustrate the energy characteristics of each scenario. The target is a microcontroller consisting of a processing unit and memory module. Both components are optimized by being separately controlled with different BB. On the other hand, to avoid level-shifter overhead, a common VDD is used for both components.

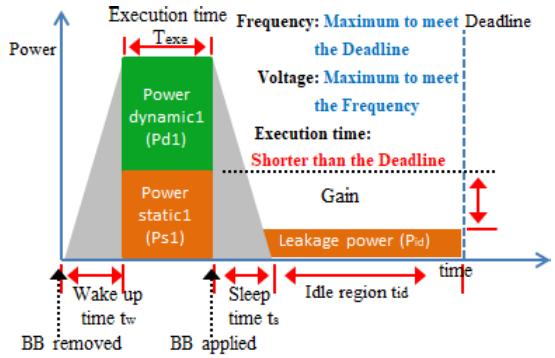


Fig. 3 Evaluation. Dynamic Power Management (DPM) with BB, which works at maximum frequency. Dynamic and static energy are consumed only at execution time. There are switching overheads and leakage current during idle period.

We give the same BB to the nMOS and pMOS transistors under the assumption that both transistors are designed so that their characteristics are balanced. That is, the following equation holds.

$$VBP = VDD - VBN \tag{1}$$

Hereafter, the BB voltage is denoted as VBN.

3.1 Timing Model

We define T_{exe} as the execution time of a given critical task, which is executed with N instructions. Assuming that each instruction is executed in CPI cycles and the clock period is T, T_{exe} can be represented as:

$$T_{exe} = N \cdot CPI \cdot T \tag{2}$$

Under the RTS paradigm, T_{exe} should satisfy Eq. (3):

$$T_{exe} + T_{ovs} \leq D \tag{3}$$

where D is the given deadline at which the critical task should be executed. For clarity, we assume $T_{exe} = D$ in the first scenario. The term T_{ovs} represents the additional time required for acquiring the necessary operational frequency. In other terms, it is the time to establish the necessary VDD and VBN when switching to and from active and idle states. It can be defined as the sum of the wake-up and sleep-down times, t_w and t_s, represented as:

$$T_{ovs} = t_w + t_s \tag{4}$$

3.2 Power Model

Considering the timing constraints, we propose a power and energy model. The ideal power consumption of a VLSI system P_{ideal} is generally defined as:

$$P_{ideal} = P_s + P_d \tag{5}$$

where P_s and P_d are the static and dynamic power, respectively, which can be obtained from the following equations [5]:

$$P_s = I \cdot 10^{A \cdot VDD + B \cdot VBN} \cdot VDD \quad (6)$$

$$P_d = \alpha_{at} \cdot C \cdot VDD^2 \cdot f \quad (7)$$

In Eq. (6), I is the leakage current, and A and B are coefficients of exponential terms for VDD and VBN, respectively. In Eq. (7), α is the switching-activity factor, C is the capacitance, and f is the minimum operating frequency (minimum frequency required to meet the deadline).

The static energy at the execution time E_s, represented in Figs. 2 and 3, can be calculated as:

$$E_s = I \cdot 10^{A \cdot VDD + B \cdot VBN} \cdot VDD \cdot T_{exe} \quad (8)$$

Using Eqs. (2) and (7), the dynamic energy E_d can be expressed as:

$$E_d = \alpha_{at} \cdot C \cdot VDD^2 \cdot N \cdot CPI \quad (9)$$

By applying the above equations, the total energy consumption for the first scenario is:

$$E = I \cdot 10^{A \cdot VDD} \cdot VDD \cdot Texe + \alpha_{at} \cdot C \cdot VDD^2 \cdot N \cdot CPI \quad (10)$$

Furthermore, referring to the second scenario, another portion of energy should be considered. When the task execution is completed prior to the deadline, the system can enter into an idle state. Although the RBB can reduce the leakage current, it is still consumed, as shown in Fig. 3 (b). Besides this leakage energy, the BB switching also consumes some energy E_{ovs}, which can be calculated as:

$$E_{ovs} = \int_{t_{si}}^{t_{sf}} VBN(t)I(t)dt \quad (11)$$

where t_{si} is the BB-transition starting point and t_{sf} is where it ends. The term $I(t)$ is the current flowing in the BB terminal. It is important to mention that only the sleep-down energy was considered. This is due to the fact that the sleep-down energy represents the current charging while the wake-up voltage refers to the current discharge.

As shown in Eq. (8), the energy consumption at the idle state E_{id} for the second scenario can be:

$$E_{id} = I \cdot 10^{A \cdot VDD + B \cdot VBN_{id}} \cdot VDD \cdot T_{id} \quad (12)$$

The VBN_{id} is the applied RBB and T_{id} is the idle time. Using Eq. (3), T_{id} can be calculated as:

$$T_{id} = D - T_{exe} - t_w - t_s \quad (13)$$

Finally, considering the overhead caused by dynamic BB control (transition period) and the leakage energy at T_{id}, the total energy is:

$$E = E_s + E_d + E_{ovs} + E_{id} \quad (14)$$

3.3 Finding Optimal VDD

To determine the VDD at a given frequency f_{max}, we use the alpha power law as:

$$f_{max} = F \cdot \frac{(VDD - Vth)^{\alpha}}{VDD} \quad (15)$$

where F is a coefficient related to frequency and $1 \leq \alpha \leq 2$ is the saturation coefficient, which is equal to 2 in the case of the SOTB technology [5], [16]. From the above equation, the optimal VDD at the operational state can be expressed as:

$$VDD = \frac{(V_{th} + \frac{f_{max}}{F}) + \sqrt{(V_{th} + \frac{f_{max}}{F})^2 - 4V_{th}^2}}{2} \quad (16)$$

4. Methodology

4.1 Target System: V850 E-Star

The proposed models can be applied to any RTS. Nevertheless, to evaluate its efficiency, we used V850 E-Star (V850) as the target system. It is a high-performance low-power 32-bit RISC microcontroller for car electronics, digital signal processing, and digital servo-motor control. It is composed of a five-stage standard pipeline with 46.2-k gate logic cells and 128-kb instruction/data memory modules [17]. The chip used was implemented with LEAP 65-nm FD-SOI SOTB technology. A photograph of the chip is shown in Fig. 4. Chip measurement was done with an evaluation board, as illustrated in Fig. 5. The VDDs can be statically altered using DC-DC converters, and the V850 state can be controlled using the attached field-programmable array (FPGA). The V850 basically executes one instruction per clock cycle; hence, $CPI = 1$. The V850 contains a processing core and on-chip memory. These two components have different timing and power characteristics; thus, different BB voltage terminals, called VBN and VBP for the core, and VBNM and VBPM for the memory, respectively.

4.2 Model Coefficients

Both core and memory components should be modeled in-

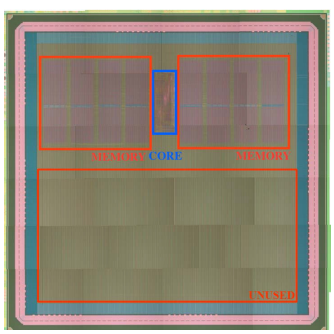


Fig. 4 Chip photograph of V850E-Star microcontroller.

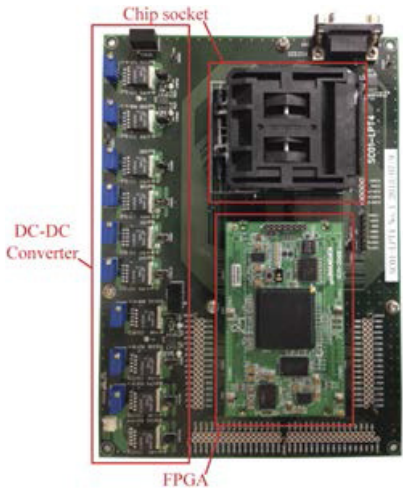


Fig. 5 Evaluation board of V850 E-Star.

Table 1 Coefficients for proposed power model.

Parameter	Core	Memory
I	0.2587×10^{-3}	3.0523×10^{-3}
A	0.51921	0.45172
B	1.7926	2.1563
F	6.6641×10^{8}	6.8350×10^{8}
$\alpha_{at}C$	0.6247×10^{-10}	1.3669×10^{-10}

dependently; hence, the total energy consumption of the target microcontroller for both scenarios E_{sc1} and E_{sc2} can be represented using Eq. (17) for the first scenario and Eq. (18) for the second scenario.

$$E_{sc1} = E_{score} + E_{smem} + E_{dcore} + E_{dmem} \quad (17)$$

$$E_{sc2} = E_{score} + E_{smem} + E_{dcore} + E_{dmem} + E_{ovscore} + E_{ovsmem} + E_{idcore} + E_{idmem} \quad (18)$$

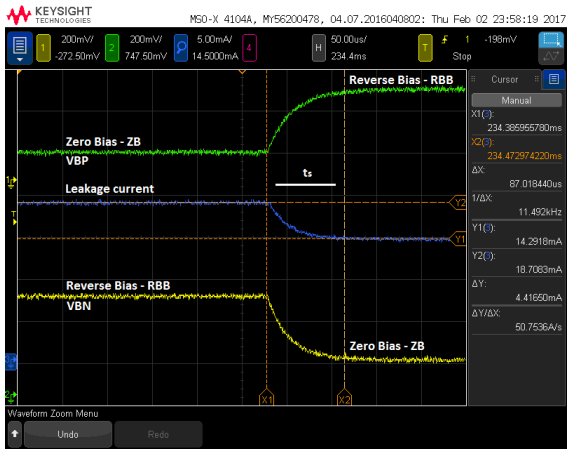
For these equations, parameters I, A, B, and $\alpha_{at}C$ can be obtained from real-chip measurements, as shown in [5]. Table 1 lists these power-model coefficients.

5. Evaluation of Dynamic BB Scaling Overheads

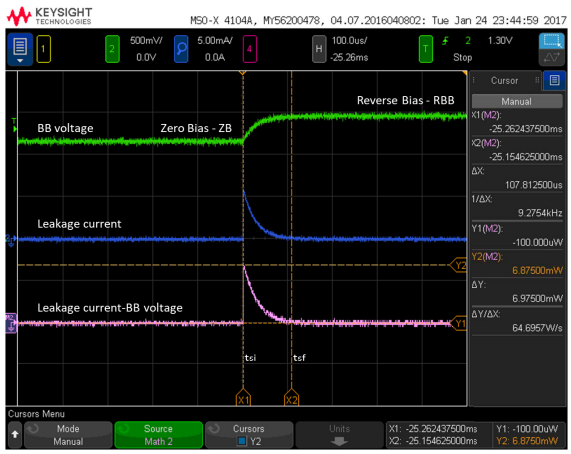
5.1 Experimental Set Up

To investigate the effect of BB overheads, we conducted a real-chip evaluation with the V850Estar microcontroller. For these experiments, SG-4322, which is a function generator provided by Iwatsu Electric Co. Ltd., was used as the BB generator. Both VBP and VBN were changed simultaneously. The energy and timing overheads were measured using the Keysight MSOX 4104A oscilloscope and N2820A current probe.

For the timing-overhead measurement, the N2820A was connected between the VDD terminal of the V850 and an off-chip power supply driver for determining whether the effect of the BB is obtained by observing the leakage-current behavior. In this experiment, we defined the timing overhead as the period of the leakage-current transition. Figure 6 (a) illustrates the actual behavioral response obtained from this experiment.



(a) Timing



(b) Energy

Fig. 6 Waveforms obtained with real chip: (a) Timing-overhead evaluation. (b) Energy-overhead evaluation.

For the overhead-energy measurements, the current probe was connected to the function generator and BB terminals of the V850. Therefore, immediately when BB was changed, we observed a current spike when charging the well capacitor, as shown in Fig. 6 (b), which is decreased accordingly, the capacitor charges. This period lasted during the sleep time. We integrate the BB voltage and the leakage current, as shown in Fig. 6 (b) by "Leakage current-BB voltage".

In SOTB chips, all I/O pads for the BB are just metal without any resistors or capacitors. Also, all decoupling capacitors on the board are removed so that the power and timing overhead can be measured without any influence from outside the chip. The BB voltage was changed from RBB (ZBB) to ZBB (RBB) voltages. The RBB voltage for pMOS (nMOS) swept from 1300 mV (−700 mV) to 800 mV (−200 mV). We applied the same range of voltages to the core and memory for modeling purposes. However, these voltages were applied separately and analyzed in the same fashion.

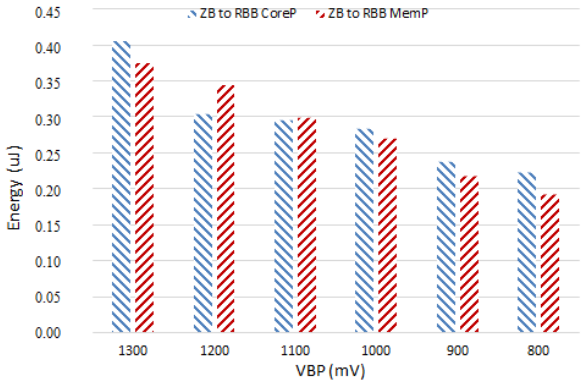


Fig. 7 Energy consumption for ZB-RBB transition relationship between core and memory for pMOS transistor.

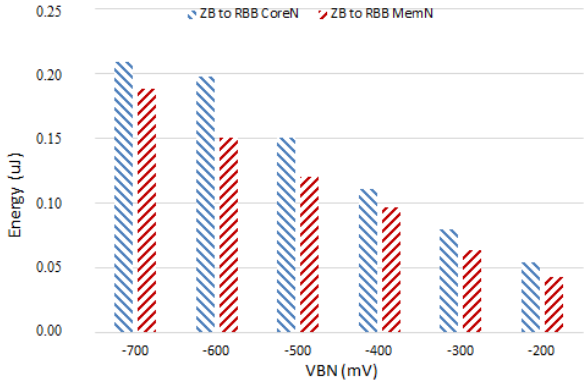


Fig. 8 Energy consumption for ZB-RBB transition relationship between core and memory for nMOS transistor.

5.2 Body-Bias Energy-Transition Evaluation

As previously mentioned, since the target system consumes energy when applying the RBB, only the sleep-down transition was considered for analysis. The results are shown in Fig. 7 for VBP and Fig. 8 for VBN. From these graphs, we can observe that the amount of charge for pMOS is larger than that of nMOS. According to the well structure of SOTB, the pMOS (nMOS) was formed on the n-well (p-well), as previously represented in Fig. 1. This means that the p-well has a larger area of the p-n junction and larger capacitance. In fact, in Fig. 7, the pMOS shows the maximum value of 400 nJ and minimum value of 190 nJ. While in Fig. 8, the nMOS shows the maximum of 210 nJ and minimum of 47 nJ. The energy of pMOS is twice that of nMOS at its highest settings and four times the energy at its smallest. Furthermore, there is a clear pattern where the energy overhead decreased when the RBB voltage decreased, having values in the nano-Joule (nJ) order. Finally, when averaging the results of both pMOS and nMOS, the core consumed more energy than the memory modules. The reason for this is that the core shares the BB for all the chip area except the memory region as well as the core region shown in Fig. 4. Such an area includes many filler cells and buffer cells, which consume the static power.

As in our earlier paper [18], the efficiency of the dynamic BB scaling can be characterized by the break even time (BET) and can be used as a rule of sum. Devices should enter into the low-power state only when the idle duration is long enough to compensate for the energy overhead necessary to switch to the low-power state [19].

The BET is a function of the static power consumed at the active state P_s, amount of power consumed during the idle state P_{id}, and energy overhead of the sleep-down transition E_{ts}, as illustrated in Fig. 3 (b). This can be calculated using Eq. (19):

$$BET = \frac{E_{ts}}{P_s - P_{id}} \tag{19}$$

By evaluating this equation across several voltages, we can determine the BET behavioral region. Therefore, we include in this equation our power-model coefficients (listed in Table 1) and shown in Eq. (10), measured leakage current, switching activity, VDD, and VBN voltages and incorporate our obtained overhead coefficients. Figure 9 illustrates this working region. We assume a VDD = 600 mV, which is a nominal value.

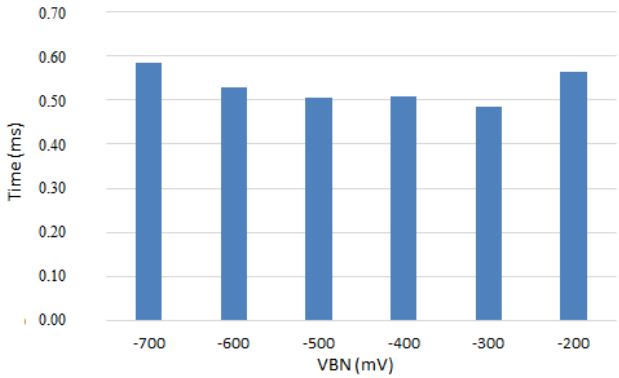


Fig. 9 Break Even Time curve, set VDD = 600 mV.

While a high RBB saves significant static power in the idle state, the switching overhead becomes larger. We can see a bell curve that has its lowest points at −300 mV of VBN and 900 mV of VBP voltages. Under this condition, about 0.48 μs of BET is obtained. However, when averaging, we can observe a trend that a bell curve having lower voltage points from −500 mV to −300 mV, this means around 0.5 ms of BET.

5.3 Body-Bias Transition Time

As in our earlier paper [20], a certain time (timing overhead) is needed for sleeping down or waking up by changing the BB voltage. We measured the BB transition time with the same sleep-down conditions as mentioned in the previous subsection. The results are shown in Fig. 10. The transition timing trended to decrease when BB voltage decreased. The memory transition time was about a half that for the core; thus, a strategy of only sleeping memory might be advantageous in some situations. We count the slowest transition

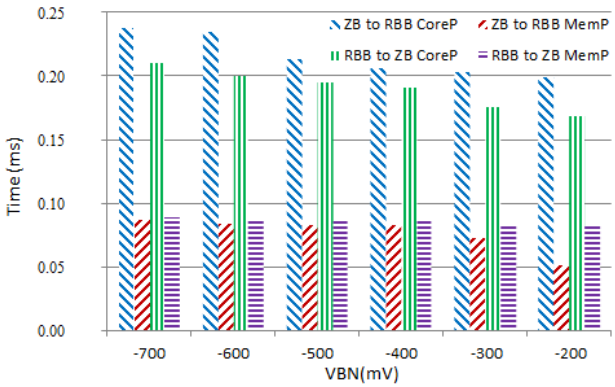


Fig. 10 Timing-transition relationship for wake-up (ZB) and sleep-down (RBB).

time as an overhead and assume the worst-case energy saving, that is, leakage is not reduced during the transition. The slowest transition time increases with a large BB voltage; thus, reducing the leakage with a large reverse BB voltage requires timing overhead as well as energy overhead.

6. Effect of Dynamic BB Scaling

In this section, we discuss the optimal RBB for the second scenario and evaluate its energy reduction.

6.1 Optimized VDD for Active State

First, we focus on the active state. As stated earlier, the number of instructions N was determined from the first scenario with $CPI = 1$. Since the V850 includes a single local memory, one instruction is executed in a clock cycle [21], [22]. Hence, higher operational frequencies than that of the first scenario allow the instruction execution of each task to finish prior to the deadline. When a periodic real-time task finishes execution, the system can be put into idle state by the next active state.

The VDDs for each operational frequency are obtained with Eq. (16). We compute and use the optimized voltage conditions for VDD that are appropriate to each frequency according to the alpha power law. The VDD is determined beforehand and fixed through all the active and idle periods. We do not change it dynamically due to the high cost of doing so, as described earlier. In the active state, the BB is set to the ZBB. This VDD optimization method does not have any penalties regarding the target microcontroller or the platform [5]. These settings are summarized in Table 2.

6.2 Optimal RBB and Power Reduction by BB Scaling

The BET can ensure static energy reduction; however, we must select the optimal VBN considering all energy combinations in the second scenario. As an exemplification, let us assume a scenario in which the deadline is 3 ms. We use Eqs. (8), (9), and (12) to calculate E_s, E_d, and E_{id}, respectively. For E_{ovs}, we simplify the use of Eq. (11) and use the

Table 2 Scenario 2 voltage settings. VDD optimized for given frequency according to alpha power law.

FrEq. (MHz)	VDD (mV)	VBN-Active State.
10	304.11	
20	340.99	
30	371.97	Zero Bias
40	403.52	
50	437.84	
60	470.87	

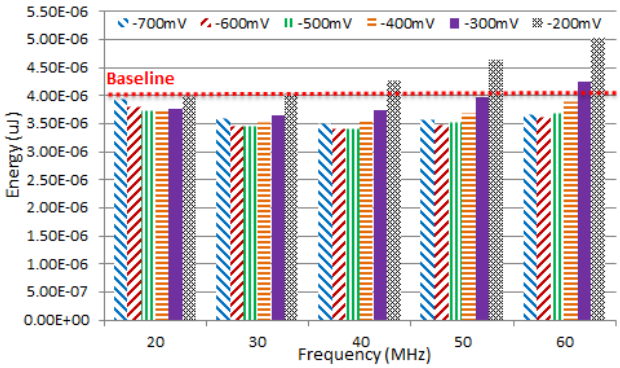


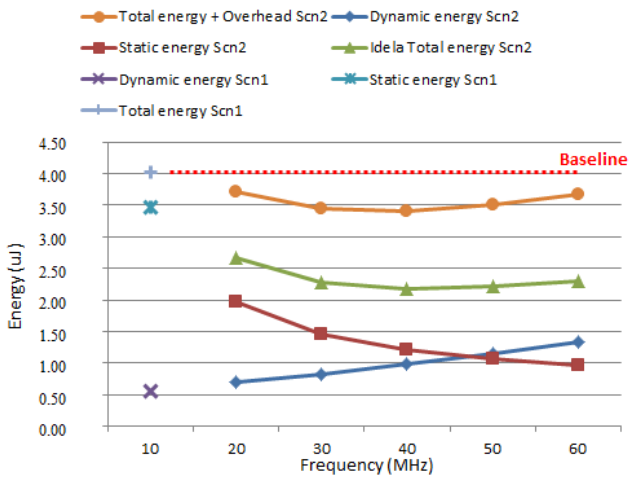
Fig. 11 Total energy consumption including energy transition. Scenario 1 vs. scenario 2. Sweep across several frequencies and VBNs. Deadline = 3 ms.

measurements from our evaluation. Figure 11 shows the results of this evaluation. It describes the change in the energy consumption with various VBNs for such a deadline. The horizontal line is the optimized energy of scenario 1, which works at a 10 MHz clock frequency. For a large frequency corresponding to a short active state, a strong RBB is advantageous. However, as we have a tradeoff between switching power and operational frequency, 60 MHz of operational frequency cannot be the optimal point. In this figure, the best reduction ratio was achieved with −500 mV VBN at a 40 MHz clock frequency in the active state. To show the tradeoff in simple terms, the energy efficiency breakdown of the second scenario with a 3 ms deadline is shown in Fig. 12 (a).

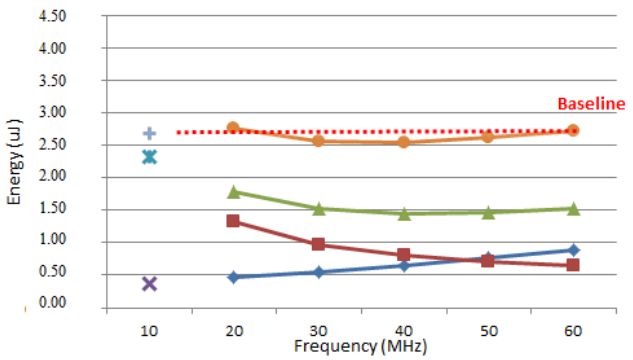
The optimal VBN = −500 mV was used. For a large frequency corresponding to a short active state, the dynamic energy in the active state increased, while the total static energy decreased thanks to the energy reduction in the idle state.

Moreover, the energy breakdown proves that we cannot ignore the energy overhead when designing a system, especially RTSs. In fact, the total energy is almost doubled by the overhead of dynamic BB scaling. However, the dynamic BB is still useful for lowering system energy. In this case, we achieved 15.31% energy reduction when using a 40 MHz clock frequency. The energy saving by dynamic RBB scaling is efficient only when the deadline is long enough since shorter deadlines reduce idle duration. In fact, at a 2 ms deadline, we achieved only 5% energy saving, as shown in Fig. 12 (b).

To determine the optimal operating region for VDD



(a) Deadline = 3 ms



(b) Deadline = 2 ms

Fig. 12 Total energy consumption. Comparison between 1st scenario (Baseline at 10 MHz) and 2nd scenario (20 MHz–60 MHz) including overhead conditions. Optimal BB −500 mV.

and BB control, we applied brute force in the same fashion as described earlier to find the optimal point for a 3 ms deadline (Fig. 11). Our brute-force approach involves calculating with granularity of 1 ms and −100 mV increments for the deadline and BB control, respectively. The outcome is that 40 MHz remains the optimal frequency, regardless of the deadline length. However, for short deadlines, the optimal BB point is −500 mV. As the deadline increases, the optimal point moves to a stronger RBB. As we can see in Fig. 13, the decreasing energy rate is not linear, e.g., at around 4 ms, the −700 mV, −600 mV and −500 mV reach a similar value, from this point −500 mV is no longer optimal. Hence, the next RBB step becomes the optimal value of the region. Increasing the deadline decreases the energy consumed across strong RBBs. Though simple, this method can be practical as a quick reference for design.

For further analysis, energy reduction with various deadlines (2 ms, 3 ms, 4 ms, and 12 ms) is shown in Fig. 14. Since the idle time is stretched when a longer deadline is given, stronger RBB can reduce further leakage. At the 12 ms deadline, a stronger VBN (−700 mV) achieved better energy reduction than VBN = −500 mV, which we previously considered as the optimal voltage setting at the 3 ms

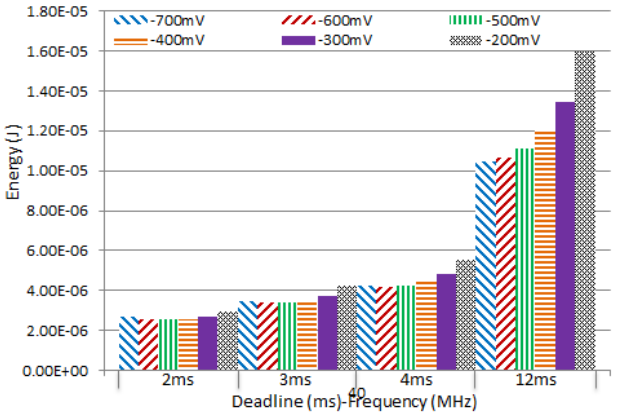


Fig. 13 Brute-force results to find optimal VDD-BB control optimal point. For illustrative purposes, we leap from 4 ms to 12 ms to show trend in energy behavior.

deadline. About 35% of energy reduction was obtained at the 12 ms deadline.

6.3 Accuracy of the Model

Models proposed here are based on the timing model in Sect. 3.1 and the energy model in Sects. 3.2 and 3.3. The following errors are considerable.

- We expressed the execution time T_{exe} as a simple expression (2). Since a micro processor includes the overhead of pipeline stall caused by the cache misses and various kind of hazards, it is too optimistic in general. However, V850E-star used in this evaluation is a simple micro-controller which provides local memory modules instead of the cache. All instructions and data are preloaded the memory before execution. Also, V850E-star can execute most of instructions without pipeline stall, that is one clock cycle. So, we can ignore the error from this part. When more sophisticated processors are treated this part of model must be elaborated.
- The base energy E shown in Expression (10) and the maximum frequency f_{max} are based on the model proposed in [5], [23]. According to the paper [23], error of the model under room temperature is about 2.7%, yet it can be increased by the temperature variation, process variation and the GIDL (Gate Induced Drain Leakage) effect. Although the GIDL effect was appeared to be less than 1%, the process variation and temperature variation must be compensated to adjust the power supply voltage. The supply voltage adjustment method proposed in [23] can be also applicable to the model used here.

All other values used in the paper come from the evaluation results from the real chip.

7. Conclusions

We presented the first investigation into analyzing BB con-

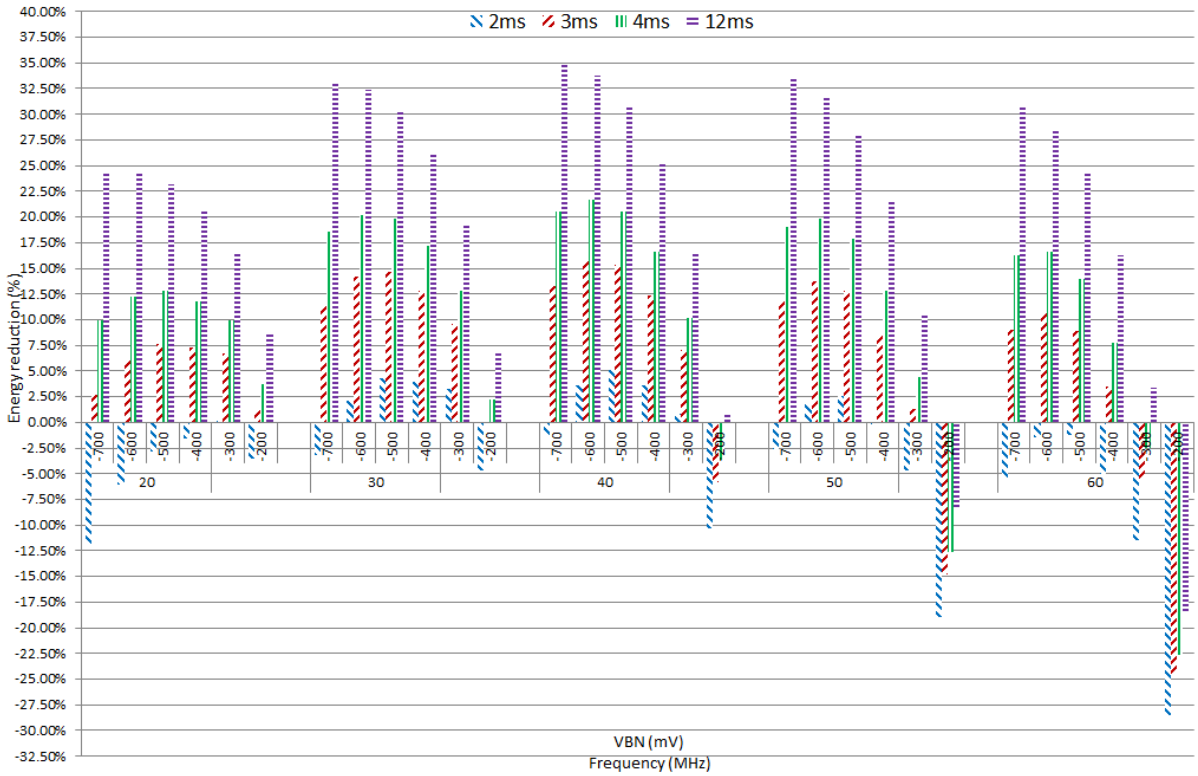


Fig. 14 Energy-reduction ratio considering leakage current at idle state across 2 ms, 3 ms, 4 ms and 12 ms deadlines. Each column represents each VBN voltage grouped by frequency.

trol with a practical approach to improve the energy efficiency for RTSs. We proposed a mathematical model, for which accurate coefficients were measured from a real chip, as well as overhead parameters used in this model. We also optimized VDD for a given frequency. We analyzed how these overhead conditions affect energy saving with a trade-off between energy consumption and execution time. By manipulating VDD and VBN to boost the frequency and execute a given task in a shorter time, we can significantly reduce energy consumption. The evaluation results indicate that the energy reduction can be 15.31% at 40 MHz and −500 mV VBN with a 3 ms deadline and can increase up to 35% at 40 MHz and −700 mV VBN with a 12 ms deadline. Although there are complex tradeoffs among the energy overhead, deadline, and dynamic power, our evaluation provided insight into these combinations.

We also found that the energy overhead contributes to the total energy consumed. This can be from 20% up to 40% of the dynamic and static energy. We presented a brute-force algorithm for finding the optimal region of VDD, BB, and deadline tradeoff. Nevertheless, the parameters applied in this brute-force analysis are coarse; hence, there is room for improvement, e.g., granularity can be adjusted to find a finer RBB control for deadlines.

We analyzed and controlled the VBN outside the chip under the assumption that external control can be equivalent to an internal control since the inputs and outputs have only metal parts; thus, there is no capacitance or diodes. However, on-chip BB generators (under development) [15], [24] should be used.

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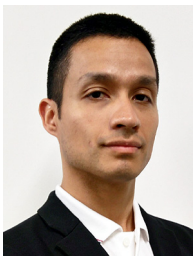

Carlos Cesar Cortes Torres received the M.Sc. degree from Keio University, Japan in 2016, currently is pursuing a Ph.D. degree at Keio University. His research interests include low power, VLSI and SoC design and computer micro-architecture.

Hayate Okuhara received the B.S. degree from Chuo University, in 2014, and the M.S. degree from Keio University, in 2016, currently is a Ph.D. candidate at Keio University. His research interests include low power LSI design and low power computer architecture.

Nobuyuki Yamasaki received a Ph.D. in engineering from Keio University in 1996. He is a professor in the Department of Information and Computer Science at Keio University. His research interests include real-time processing and communication, parallel and distributed processing, computer architecture, operating systems, embedded systems, and SoC design. He is a member of IEICE, IPSJ, RSJ, and IEEE.

Hideharu Amano received a Ph.D. in electric engineering from Keio University in Japan in 1986. He is a professor in the Department of Information and Computer Science at Keio University. His research interests include parallel architecture and reconfigurable computing.