## **FOREWORD**

## **Special Section on Parallel and Distributed Computing and Networking**

Welcome to the Special Section on Parallel and Distributed Computing and Networking. This special section was planned to publish high quality papers reflecting the recent research activities in the fields of parallel/distributed computing and networking, such as parallel/distributed algorithms and their applications, innovative hardware and parallel/distributed architectures, distributed systems and networking, and software systems and fundamental technology. This special section brings together high-quality and timely papers on the recent progress in the interdisciplinary area of parallel and distributed computing and networking. These papers include the extended versions of conference papers presented at the International Symposium on Computing and Networking (CANDAR'16), in addition to bland-new contributions from our IEICE members.

The submitted papers to this section were 27 papers and 6 letters, which were from five countries: 18 from Japan, 5 from China, 3 from Korea, 1 from India, and 2 from Taiwan. Through the fair and strict reviewing process by expert reviewers, 11 papers and 2 letters were finally accepted for publication. It was an extremely difficult task to select papers to be published because there were so many excellent and interesting submissions.

It is my honor to serve as the guest editors-in-chief of this special section. It is the result of hard and excellent work of the guest associate editors. Especially, we could not reach our goal without a hard work of two Guest Editors, Dr. Akihiro Fujiwara and Dr. Michihiro Koibuchi. We would also like to express our sincere appreciation to all authors for their valuable contributions, and to all external reviewers for their cooperation and contributions.

Special Section Editorial Committee Members

Guest Editors: Akihiro Fujiwara (Kyushu Institute of Technology), Michihiro Koibuchi (NII)

Guest Associate Editors: Ryusuke Egawa (Tohoku Univ.), Ikki Fujiwara (NII), Hiroaki Inoue (NEC), Yasuaki Ito (Hiroshima Univ.), Kenji Kawahara (Kyushu Institute of Technology), Kenji Kise (Tokyo Tech), Hiroki Matsutani (Keio Univ.), Takashi Miyoshi (FUJITSU Lab.), Hironori Nakajo (Tokyo Univ. of Agriculture and Technology), Akira Naruse (NVIDIA), Masakatsu Ogawa (Sophia Univ.), Fukuhito Ooshita (Nara Institute of Science and Technology), Yoshinori Sato (Tokyo Tech), Ryota Shioya (Nagoya Univ.), Shigeaki Tagashira (Kansai Univ.), Hirozumi Yamaguchi (Osaka Univ.), Toshihiro Yamauchi (Okayama Univ.)

Satoshi Fujita (Hiroshima University), Guest Editor-in-Chief

**Satoshi Fujita** (Member) is a professor of Department of Information Engineering, Faculty of Engineering, Hiroshima University. He received the B.E. degree in electrical engineering, M.E. degree in systems engineering, and Dr. E. degree in information engineering from Hiroshima University in 1985, 1987, and 1990, respectively. He has served as program committee or organizing committee chairs of many international conferences, and served on the editorial board of the IEICE Transactions on Information and Systems. His research interests include communication algorithms, graph algorithms, and parallel computer systems. He is a member of IEEE Computer Society, SIAM, IEICE, IPS, and SIAM Japan.

