FOREWORD

Special Section on Reconfigurable Systems

Reconfigurable Systems are the processing system that can flexibly exploit the parallelism of the algorithm, and run it directly on the processing device. By using the parallelism of the parallel algorithm, Reconfigurable Systems are possible to balance computing performance, processing device size and power consumption, on various positions. With such flexibility, Reconfigurable Systems are adaptable for implementing various systems such as "small embedded systems" to "large-scale supercomputers" efficiently. In addition, the flexibility of Reconfigurable Systems lets us program the internal structure of processing device. With the flexibility in the internal structure of the device, various fault-tolerant designs and also power saving designs are possible in logic-gate level and system level.

However, because of the various aspects of the Reconfigurable Systems the design framework for it requires a wider and a different set of knowledge than on the traditional systems, in the area of application, system software, computer architecture, and device technology. To make the Reconfigurable Systems become a more practical technology in the industry, advanced researches and developments in this area are needed to be presented widely to show what can be done.

So we planned a special section in order to sum up the recent advanced researches and developments of various areas on reconfigurable systems. In response to the call for papers for this special section, 15 regular papers were submitted. Through the same review and editorial process as the regular section, 10 papers were accepted for publication. The selected papers will give readers the latest results of researches in various fields of Reconfigurable Systems.

The special section editorial committee members listed below wish to thank all of those who submitted papers, as well as the reviewers for their thoughtful comments and suggestions. As the guest editor, I would wish to convey my earnest thanks to the editorial committee members for their endeavors to preserve the quality of the selected papers high.

The Special Section Editorial Committee Members:
Guest Editors:

Hiroki Matsutani (Keio University), Yukinori Sato (Tokyo Institute of Technology), Hideharu Amano (Keio University), Yohei Hori (National Institute of Advanced Industrial Science and Technology), Masahiro Iida (Kumamoto University), Yasushi Inoguchi (Japan Advanced Institute of Science and Technology), Hiroaki Inoue (NEC Corporation), Tomonori Izumi (Ritsumeikan University), Shorin Kyo (Huawei Technologies Japan), Yukio Mitsuyama (Kochi University of Technology), Akira Nagoya (Okayama University), Hiroki Nakahara (Tokyo Institute of Technology), Yasunori Osana (University of the Ryukyus), Kentaro Sano (Tohoku University) Yuichiro Shibata (Nagasaki University), Kazuya Tanigawa (Hiroshima City University), Takao Toi (Renesas Electronics), Yutaka Yamada (Toshiba Corporation)

Minoru Watanabe, Guest Editor-in-Chief

Minoru Watanabe *(Member)* received B.S. and M.S. degrees in Opto-Electronic and Mechanical Engineering from Shizuoka University, Hamamatsu, Japan, in 1992 and 1994, respectively, and a Ph. D. degree in Computer Science and Systems Engineering from the Kyushu Institute of Technology, Iizuka, Japan, in 2005. He joined Nissan Motor Co. Ltd., Zama, Japan, in 1994, where he was a development engineer of embedded systems until December 1999. He was a Research Associate at the Department of Control Engineering and Science during January 2000-2003, and in the Department of Systems Innovation and Informatics during 2004-2006, Kyushu Institute of Technology, Iizuka, Japan. He is currently an Associate Professor of the Department of Electrical and Electronic Engineering, Shizuoka University, Hamamatsu, Japan. His current research interests are reconfigurable devices and optoelectronic devices.