LETTER

Wideband Radar Frequency Measurement Receiver Based on FPGA without Mixer

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SUMMARY In this letter, a flexible and compatible with fine resolution radar frequency measurement receiver is designed. The receiver is implemented on the platform of Virtex-5 Field Programmable Grid Array (FPGA) from Xilinx. The Digital Down Conversion (DDC) without mixer based on polyphase filter has been successfully introduced in this receiver to obtain lower speed data flow and better resolution. This receiver can adapt to more modulation types and higher density of pulse flow, up to 200000 pulses per second. The measurement results indicate that the receiver is capable of detecting radar pulse signal of 0.2us to 2.5ms width with a major frequency root mean square error (RMSE) within 0.44MHz. Moreover, the wider pulse width and the higher decimation rate of DDC result in better performance. This frequency measurement receiver has been successfully used in a spaceborne radar system.

key words: *radar frequency measurement, DDC without mixer, FPGA*

1. Introduction

In modern electronic warfare and reconnaissance, band width (BW) and carrier frequency (CF) are two major parameters of pulse frequency measurement. In general, conventional receivers usually utilize analog components to transform the input signal into a video signal [1]–[3]. However, analog components may include mixer, crystal oscillator, and low pass filter (LPF), which makes the receivers difficult to do maintenance and not very flexible in practice. Besides, in the real battlefield, the width of radar pulses varies greatly, but the transform length of Fast Fourier Transform (FFT) IP core in Field Programmable Grid Array (FPGA) is always limited. Some pulses are too large to be transformed by FFT IP core directly.

To solve above problems, Digital Down Conversion (DDC) without mixer is introduced in this paper. The new structure has two advantages over the conventional structures. Firstly, it can reduce the working clock to half of the data rate without losing data. Secondly, it can reduce the order of the filter by half, which is very meaningful for hardware implementation. In the structure of quadrature DDC based on polyphase filter, finite impulse response (FIR) filter plays an important role. The processing speed of FIR filter determines the real-time of the whole structure. In addition, thanks to the high development of analog to digital converter (ADC) and FPGA [4], wideband and the fine frequency resolution can be implemented easily.

The remainder of the letter is organized as follows. We present the functional block diagram breakdown of the receiver in Sect. 2 and focus on the implementation structure of high-speed DDC based on polyphase filter and principle of multi-length FFT frequency measurement method. In Sect. 3, we demonstrate the effectiveness of the proposed method with a linear frequency modulation (LFM) pulse signal and present an in-depth analysis. And in the end of Sect. 3, we introduce the packet format of the frequency results downlink transmission briefly. A summary of our work will conclude the paper in Sect. 4.

2. Principle of Operation

The flow diagram of the designed receiver is depicted in Fig. 1. As we can see, the structure is very simple, only containing three parts, i.e., the clock generator, the high-speed ADC, and the FPGA where the high-speed DDC and frequency calculation are implemented. The interaction between ADC and FPGA is via LVDS, and that between clock generator and ADC is through LVPECL. The incoming signal is firstly applied to a balun where the single-ended signal is transformed into differential signal. Then the differential signals are sent to the ADC, where the data flow is generated and sent to FPGA. 1.2GHz clock is generated by PLL circuits from 50MHz crystal oscillator. The area breakdown of the three modules in FPGA is given in the corresponding block diagrams. The structure of parallel FIR filter for Q channel in Fig. 1 is the same as I channel, so only the brief structure of I is given. The design is fully implemented in FPGA by RTL and IP core.

2.1 DDC without Mixer Based on Polyphase Filter

For direct RF sampling, the band-pass sampling theorem can be applied to select the sampling frequency. According to the band-pass sampling theory, the bandpass signal can be sampled at a low rate compared to Nyquist sampling theorem, and the signal can be reconstructed uniquely. When the relationship of the center frequency of signal f_0 and sampling frequency f_s satisfies [5]:

$$f_s = \frac{4f_0}{2m_0 + 1} \ (m_0 = 0, 1, 2, 3 \cdots) \tag{1}$$

where m_0 is the natural number and if the initial phase of the

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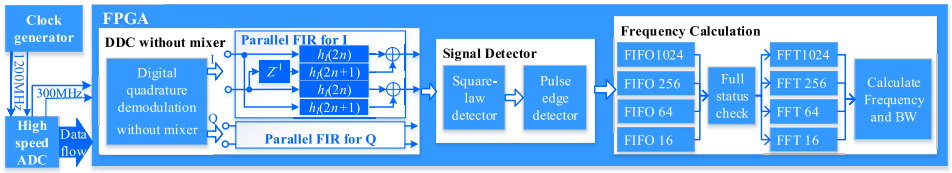

Fig. 1 The receiver functional block diagram

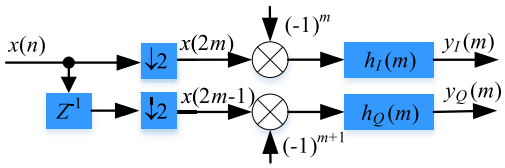

Fig. 2 The structure of mixer-free digital quadrature demodulation

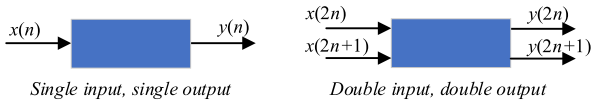

Fig. 3 The parallel structure of the FIR

local oscillator is 0 degree, then the output of the digital controlled oscillator is only 1, 0, −1. As a result, the multiplier can be removed.

Based on the theory of multi-rate signal processing, the input sequence can be extracted in odd-even order and then filtered. The extracted sequence $x_I(n)$ and $x_Q(n)$ can be given by:

$$\begin{aligned} x_I(n) &= x(2n)(-1)^n \\ x_Q(n) &= x(2n+1)(-1)^n \end{aligned} \quad n = 0, 1, 2, \cdots \tag{2}$$

where $x(n)$ is original signal sequence, $x_I(n)$ and $x_Q(n)$ differ by half a sample point in the time domain, which is caused by the extraction in odd-even order and can be revised through two phase-shifting filters whose frequency response satisfies:

$$\frac{H_I(e^{j\omega})}{H_Q(e^{j\omega})} = e^{-j\omega/2}, \ and \ |H_I(e^{j\omega})| = |H_Q(e^{j\omega})| = 1 \tag{3}$$

$H_I(e^{j\omega})$ is the frequency response of $h_I(n)$, while $H_Q(e^{j\omega})$ is the frequency response of $h_Q(n)$, $|\cdot|$ is modulo operation. $h_I(n)$ and $h_Q(n)$ can be obtained by extracting $h(n)$ in odd-even order, and $h(n)$ is an M order FIR filter, which can be obtained through Filter design & Analysis Tool (FDATool) in Matlab.

$$\begin{aligned} h_I(n) &= h(2n) \\ h_Q(n) &= h(2n+1) \end{aligned} \quad n = 0, 1, 2 \cdots \frac{M}{2} - 1 \tag{4}$$

Figure 2 shows the structure of the mixer-free digital quadrature demodulation based on poly-phase filter. $x(n)$ represents the input signal, Z^{-1} represents the inverse Z-transformation, $\downarrow 2$ represents double decimation, $h_I(m)$, $h_Q(m)$ represent time domain response of LPF, m is the natural numbers and $y_I(m)$, $y_Q(m)$ represent inphase and quadrature (IQ) outputs.

In this paper, the center frequency f_0 is 900MHz, f_s is 1.2GHz, if $m_0 = 1$, Eq. (1) is satisfied. Therefore, the processing bandwidth of the receiver can be up to 600MHz in theory, which makes the clock of the filter up to 600MHz; however, the current hardware level cannot meet such high processing speed. Therefore, a parallel structure of FIR filter is introduced. Since the parallel FIR filters of IQ channels are of the same structure, take I channel as an example. The processing framework is depicted in Fig. 3. Assume $x(n)$ is the input of FIR filter for I channel, $y(n)$ is the output of FIR filter and the coefficient of the FIR filter is $h(n)$, which is designed by FDATool in Matlab. The relationship of the three terms is given by:

$$y(n) = \sum_{k=0}^{M} x(n-k)h(k) \tag{5}$$

where M is the order of the FIR filter.

In Fig. 3, the single input and output of the data are divided into two parallel channels, so that the processing speed in the blue box can be reduced to half of that in a single channel. Supposing M is even, $M = 2T$ and T is a positive integer, and then Eq. (5) can be described as:

$$\begin{aligned} y(2n) &= \sum_{k=0}^{2T-1} h(k)x(2n-k) \\ &= \sum_{k=0}^{T-1} h(2k)x[2(n-k)] \\ &\quad + \sum_{k=0}^{T-1} h(2k+1)x[2(n-k)-1] \end{aligned} \tag{6}$$

$$\begin{aligned} y(2n+1) &= \sum_{k=0}^{2T-1} h(k)x(2n+1-k) \\ &= \sum_{k=0}^{T-1} h(2k)x[2(n-k)+1] \\ &\quad + \sum_{k=0}^{T-1} h(2k+1)x[2(n-k)] \end{aligned} \tag{7}$$

The detailed implementation structure of the parallel FIR for I channel is depicted in Fig. 4. The upper half part is corresponding to Eq. (6), while the lower half corresponds to Eq. (7). At work, data are entered in parallel, the inputs of the whole part are $x(2n)$ and $x(2n+1)$, both the upper and lower parts run simultaneously, the inputs of the upper part are $x(2n)$ and $x(2n+1)$, while the inputs of the lower part

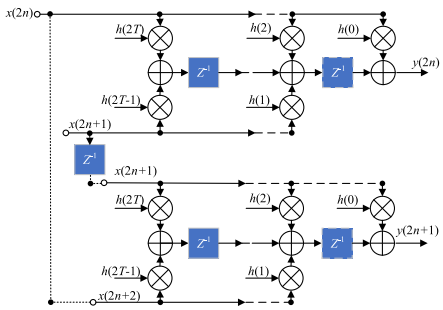

Fig. 4 The implementation structure of parallel FIR filter for I channel

Table 1 Data flow of the parallel FIR in Fig. 4.

	Time n	0	1	2		T-1	T
Inputs	$x(2n)$	$x(0)$	$x(2)$	$x(4)$		$x(2T-2)$	$x(2T)$
	$x(2n+1)$	$x(1)$	$x(3)$	$x(5)$		$x(2T-1)$	$x(2T+1)$
		\	$x(1)$	$x(3)$	...	$x(2T-3)$	$x(2T-1)$
		\	$x(2)$	$x(4)$		$x(2T-2)$	$x(2T)$
Outputs	$y(2n)$	\	\	\		\	$y(2T)$
	$y(2n+1)$	\	\	\		$y(2T-1)$	$y(2T+1)$

are $x(2n+1)$ and $x(2n+2)$. Suppose the calculation starts at time n, $x(2n)$ and $x(2n+1)$ reach the input ports at the same time. At this time, the output of the upper is valid, while the lower half is invalid because of $x(2n+2)$. In the next clock period, the inputs of the lower are valid. Therefore, there is one clock delay between the upper and lower parts. Taking no account of pipeline delay, the data flow is shown in Table 1.

As can be seen from the analysis and structure, multiplier resources required for the dual parallel processing structure are twice of the single way. In essence, it consumes more resources to get higher processing speed. Because the sampling rate of the ADC is 1.2 GHz in this paper, through parallel extracting and filtering, data rate can be dropped to 300 MHz, so FIR filter can work on a 300 MHz clock. However, 300 MHz is still a little fast for Virtex-5 devices. Therefore, we choose a device with a speed grade of -2, and through multistage pipeline design and timing constraints optimization, the real-time processing in 300 MHz is realized successfully.

2.2 Multi-Length FFT Frequency Measurement

As is known to all, the width of the pulse covers a large range, and the transform length of FFT core in the FPGA is limited. The maximum transform length of Virtex-5 FPGA is 65536. In this design, the clock is 300MHz, the maximum FFT length covers 218.453us in time domain. As a consequence, for a pulse wider than 218.453us, one frame FFT will not cover the whole pulse. Therefore, multi-frame FFT is required. In actual implementation of FPGA, the transform length of 65536 is rarely used because of its 262304 clock cycles latency [6] and the timing constraints.

Herein, the maximum length 1024 points FFT and Pipelined, Streaming I/O architecture are selected, which

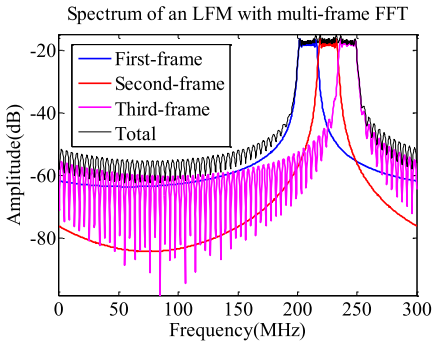

Fig. 5 Results of the frequency spectrum of LFM with multi-FFT

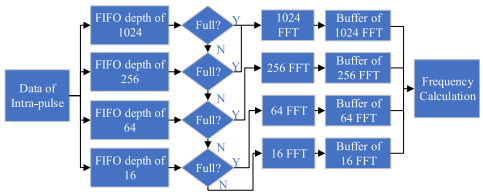

Fig. 6 Diagram of multi-length FFT frequency measurement

pipelines several Radix-2 butterfly processing engines to offer continuous data processing. The user can continuously stream in data and unload the results after the calculation latency. For a chirp signal with a pulse width of 10 us, the summation of 3 frames FFT can generate the spectrum of signal, as depicted in Fig. 5.

As the signal includes noise and there are fewer points in the narrow pulse, one length FFT will only provide a very rough estimation of the frequency so that the precision requirement for a frequency measurement receiver cannot be met. As a consequence, we picked different transform lengths of FFT to adapt varieties of pulse and different decimation rates of DDC. In this paper, 16 points, 64 points, 256 points, and 1024 points FFT are selected, which cover 48 ns, 192 ns, 768 ns, and 3072 ns in time domain, respectively. The frequency measurement work flow diagram is shown in Fig. 6.

The specified steps of frequency measurement mainly focus on the relationship between pulse width and the FFT length. The final step of the frequency measurement is frequency calculation. For convenience, all transform lengths are united into 1024. The center frequency is calculated based on the Eq. (8):

$$f_c = \frac{(Id_{left} + Id_{right})/2}{1024} \times f_{s\_dec} \tag{8}$$

The band width can be calculated by:

$$BW_{3dB} = \frac{Id_{right} - Id_{left}}{1024} \times f_{s\_dec} \tag{9}$$

where f_c is the mapped center frequency, BW_{3dB} is the 3dB band width, Id_{left} is the left-most index of signal spectrum, Id_{right} is the right-most index of signal spectrum and f_{s_dec} is the sampling frequency based on decimation rate.

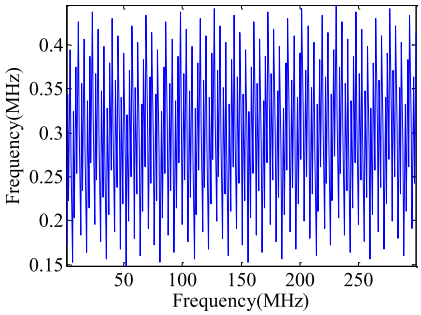

Fig. 7 RMS error of the results when f_{s_dec} = 300MHz

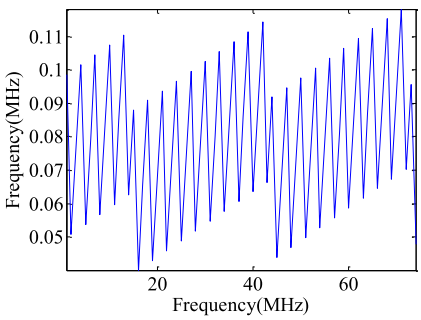

Fig. 8 RMS error of the results when f_{s_dec} = 75MHz

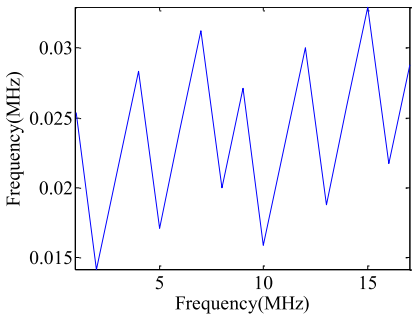

Fig. 9 RMS error of the results when f_{s_dec} = 18.75MHz

3. Result

In this design, DDC has 3 decimation rates, i.e., 300MHz, 75MHz, and 18.75MHz, respectively. 1000 tests were carried out using an LFM signal in each frequency point over the frequencies 0~300MHz with a 1MHz step for every f_{s_dec}. The RMS error of the results is depicted in Fig. 7~Fig. 9. The X axis represents the frequency of input signal; the Y axis represents the RMS error. As we can see, the max RMS error is 0.44MHz when f_{s_dec} = 300MHz, the max RMS error is 0.12MHz when f_{s_dec} = 75MHz, and RMS error is 0.033MHz when f_{s_dec} = 18.75MHz. Due to the Picket Fence Effect of the FFT, the RMS error is turned to be periodic and can hardly be removed totally.

Figure 10 shows the results of the measured data and filtered result. The magenta line is the measured data captured with ChipScope, and the blue line is the result after median filter.

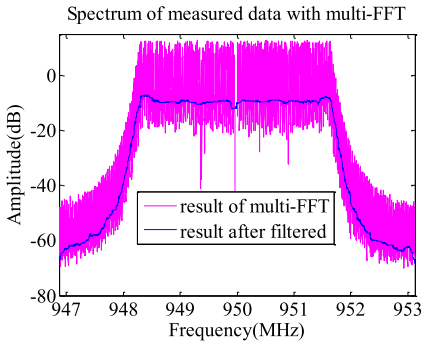

Fig. 10 The spectrum of an LFM based on measured data

Table 2 The package format of downstream data

Sync header	Header information	Results area	Cyclic Redundancy Check (CRC)

The frequency measurement results are transmitted down to the ground equipment in the form of packets via an 8-bit LVDS. The packet is formatted as follows. Then the packets are analyzed through specific analysis software.

4. Conclusion

The designed radar frequency measurement receiver is a compatible, reliable and practical device for wideband radars. Especially the RF sampling simplifies the complexity of the system extremely. The non-mixing structure and polyphase filtering of DDC make the implementation on FPGA more convenient and lower down the arithmetic speed. With a 300MHz frequency bandwidth and a major error within 0.15 MHz to 0.44MHz, the pipelined frequency measurement method has been successfully applied in wideband radar systems. On the platform consisting of the Xilinx XC5VFX130T with speed grade -2 and TI ADC12D1600, with the help of Xilinx ISE Project Navigator, Matlab and ChipScope, both the simulation and measurement results demonstrate the effectiveness of our design.

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