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FOREWORD

Special Section on Reconfigurable Systems

Reconfigurable Systems are the processing systems that can flexibly exploit the parallelism of target algorithms, and run them directly on processing devices. By extending the algorithm-level parallelism to hardware-level parallel execution in sophisticated manners, Reconfigurable Systems are possible to balance computing performance, processing device size and power consumption, on various positions. With such flexibility, Reconfigurable Systems are adaptable for implementing various systems such as "small embedded systems" to "large-scale supercomputers" efficiently. In addition, the flexibility of Reconfigurable Systems let us program the internal structure of processing devices. With this additional flexibility, various fault-tolerant designs as well as power saving designs are possible in logic-gate and system levels.

Because of the various aspects of the Reconfigurable Systems, however, their design frameworks require a wider and different set of knowledge than those for the traditional systems, in the areas of application, system software, computer architecture, and device technology. To make the Reconfigurable Systems more practical and mature technology in the industry, advanced researches and developments in those areas need to be shared widely among the community for facilitating common understanding on the state of art.

Hence, we planned a special section in order to sum up the recent advanced researches and developments of various areas on Reconfigurable Systems. In response to the call for papers for this special section, 12 regular papers and 3 letters were submitted. Through the same review and editorial process as the regular section, 5 papers were accepted for publication. The selected papers will give readers the latest results of researches in various fields of Reconfigurable Systems.

The special section editorial committee members listed below wish to thank all of those who submitted papers, as well as the reviewers for their thoughtful comments and suggestions. As the guest editor, I would wish to convey my earnest thanks to the editorial committee members for their endeavors to preserve the quality of the selected papers high.

The Special Section Editorial Committee Members:
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Masato Motomura, Guest Editor-in-Chief

Masato Motomura *(Member)* received B.S. and M.S. in 1985 and 1987, respectively, and Ph.D. of Electrical Engineering in 1996, all from Kyoto University. He joined NEC in 1987, where he worked on various hardware architectures including memory-based processors and reconfigurable systems. He also led research and business development of dynamically reconfigurable processor (DRP) that he invented. He was a visiting researcher at MIT from 1991 to 1992. Now being a professor at Hokkaido University since 2011, his current research interests include reconfigurable and parallel architectures for deep neural networks, machine learning, annealing machines, and intelligent computing in general. He won the IEEE JSSC Annual Best Paper Award in 1992, IPSJ Annual Best Paper Award in 1999, and IEICE Achievement Award in 2011, ISSCC Silkroad Award as the corresponding author in 2018, respectively. He is a member of IEEE, IEICE, IPSJ, and EAJ.