PAPER

Universal Testing for Linear Feed-Forward/Feedback Shift Registers

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SUMMARY *Linear feed-forward/feedback shift registers* are used as an effective tool of testing circuits in various fields including built-in self-test and secure scan design. In this paper, we consider the issue of testing linear feed-forward/feedback shift registers themselves. To test linear feed-forward/feedback shift registers, it is necessary to generate a test sequence for each register. We first present an experimental result such that a commercial ATPG (automatic test pattern generator) cannot always generate a test sequence with high fault coverage even for 64-stage linear feed-forward/feedback shift registers. We then show that there exists a *universal* test sequence with 100% of fault coverage for the class of linear feed-forward/feedback shift registers so that no test generation is required, i.e., the cost of test generation is zero. We prove the existence theorem of universal test sequences for the class of linear feed-forward/feedback shift registers.

key words: *linear feed-forward shift registers, linear feedback shift registers, test generation, sequential logic, universal test, built-in self-test, secure scan design*

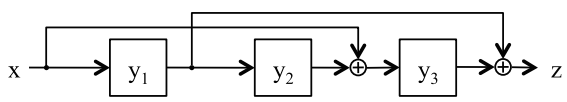
1. Introduction

Linear feed-forward/feedback shift registers are used as an effective tool of testing circuits in various fields including built-in self-test [1]–[4] and secure scan design [5]–[8]. Many works on built-in self-test using linear feedback shift registers have been reported [1]–[4], and it is well-known that linear feedback shift registers can be used as a test pattern generator or as a test response compactor. In scan design, we reported a secure scan design approach by using *extended shift registers* called "*SR-equivalents*" that are functionally equivalent but not structurally equivalent to shift registers [6]–[8]. Among the class of extended shift registers, there are linear feed-forward shift registers and linear feedback shift registers.

As stated above, linear feed-forward/feedback shift registers are used to test circuits. Then, our next concern is how to test linear feed-forward/feedback shift registers themselves. To test those circuits, we need to generate a test sequence for each linear feed-forward/feedback shift register. However, the test generation for those circuits does not seem to be so easy because of sequential logic circuits. In this paper, we first present an experimental result such that a commercial ATPG (automatic test pattern generator) cannot always generate a test sequence with high fault coverage even for 64-stage linear feed-forward/feedback shift registers. To resolve this issue, we consider *universal testability* for linear feed-forward/feedback shift registers. *Universal testing* [1] is performed with a test sequence that is independent of the function realized by the circuit under test. Usually, such a universal test sequence depends only on the size of the circuit. If there exists a universal test sequence for a class of circuits, test generation for the class is not required, i.e., the cost of test generation is zero. In this paper, we show that there exists a *universal* test sequence with 100% of fault coverage for the class of *linear feed-forward shift registers* and *linear feedback shift registers* so that no test generation is required, i.e., the cost of test generation is zero. We prove the existence theorem of universal test sequences for linear feed-forward shift registers and linear feedback shift registers. Experimental results show that universal test sequences are much superior to the test sequences generated by a commercial ATPG with respect to both fault coverage and test sequence length.

2. Linear Feed-Forward/Feedback Shift Registers

In our previous works [6]–[8], we introduced *extended shift registers* (*ESRs*, for short) to organize secure and testable scan design. Among the class of ESRs, there are *linear feed-forward shift registers* (*LF*^{2}*SRs*, for short) and *linear feedback shift registers* (*LFSR*, for short).



(a) LF^{2}SR, R_1.

x	y_1	y_2	y_3	z
$x(t)$	$y_1(t)$	$y_2(t)$	$y_3(t)$	$z(t) = y_1(t) \oplus y_3(t)$
$x(t+1)$	$x(t)$	$y_1(t)$	$x(t) \oplus y_2(t)$	$z(t+1) = y_2(t)$
$x(t+2)$	$x(t+1)$	$x(t)$	$x(t+1) \oplus y_1(t)$	$z(t+2) = y_1(t)$
$x(t+3)$	$x(t+2)$	$x(t+1)$	$x(t+2) \oplus x(t)$	$z(t+3) = x(t)$

(b) Symbolic simulation of R_1.

Fig. 1 Example of linear feed-forward shift register.

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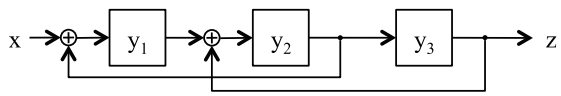
Table 1 Test generation with TetraMAX.

Circuit	Number of flip-flops	Number of feed lines	Number of target faults	Number of detected faults	Fault coverage (%)	Length of test sequence	CPU time (second)
LF^{2}SR32a	32	4	284	284	100.00	317	16.80
LF^{2}SR32b	32	6	296	296	100.00	163	0.29
LF^{2}SR32c	32	10	320	319	99.69	73	5.02
LF^{2}SR64a	64	4	540	244	45.19	55	118.52
LF^{2}SR64b	64	6	552	307	55.62	149	181.86
LF^{2}SR64c	64	10	576	296	51.39	141	451.07
LFSR32a	32	4	284	282	99.30	162	2.14
LFSR32b	32	6	296	294	99.32	191	13.50
LFSR32c	32	10	320	317	99.06	234	23.89
LFSR64a	64	4	540	258	47.78	143	488.94
LFSR64b	64	6	552	258	46.74	126	936.93
LFSR64c	64	10	576	560	97.22	248	1906.95



(a) LFSR, R_2.

x	y_1	y_2	y_3	z
x(t)	y_1(t)	y_2(t)	y_3(t)	z(t) = y_3(t)
x(t+1)	x(t)⊕y_2(t)	y_1(t)⊕y_3(t)	y_2(t)	z(t+1) = y_2(t)
x(t+2)	x(t+1)⊕y_1(t)⊕y_3(t)	x(t)	y_1(t)⊕y_3(t)	z(t+2) = y_1(t)⊕y_3(t)
x(t+3)	x(t+2)⊕x(t)	x(t+1)	x(t)	z(t+3) = x(t)

(b) Symbolic simulation of R_2.

Fig. 2 Example of linear feedback shift register.

Figure 1 illustrates an example of LF^{2}SR. Figure 1 (a) is a 3-stage LF^{2}SR, R_1, with three flip-flops, two XOR gates, and two *feed-forward* lines. Figure 1 (b) illustrates the symbolic simulation of R_1. Figure 2 illustrates an example of LFSR. Figure 2 (a) is a 3-stage LFSR, R_2, with three flip-flops, two XOR gates, and two *feedback* lines. Figure 2 (b) illustrates the symbolic simulation of R_2. Symbolic simulation is useful to analyze the behavior of linear feed-forward/feedback shift registers. In the figures, an input sequence $(x(t), x(t+1), x(t+2)), x(t+3))$ is applied to the circuit from the initial state $(y_1(t), y_2(t), y_3(t))$ at time t, and the output sequence $(z(t), z(t+1), z(t+2)), z(t+3))$ is obtained.

LF^{2}SRs and LFSRs are used to realize secure and testable scan design. The security level of the secure scan architecture is determined by the probability that an attacker can guess right the structure of the LF^{2}SR/LFSR used in the scan design, and hence the attack probability approximates to the reciprocal of the cardinality of the class of LF^{2}SRs/LFSRs. In [6], we clarified the cardinality of each class of ESRs. The cardinality of the class of k-stage LF^{2}SRs is $2^{k(k+1)/2} - 1$, and the cardinality of the class of k-stage LFSRs is also $2^{k(k+1)/2} - 1$. Hence, the cardinality of the class of k-stage LF^{2}SRs and LFSRs is $2(2^{k(k+1)/2} - 1)$.

3. Test Generation vs. Universal Testing

The types of faults considered here are *single stuck-at faults* on signal lines of a circuit under test. Signal lines of LF^{2}SRs and LFSRs are classified into two types; *basic signal lines* and *feed signal lines*. *Basic signal lines* are signal lines on the path from x to z thru all flip-flops once, i.e., signal lines on the path of $(x, y_1, y_2, \ldots, y_k, z)$. Hence basic signal lines include the primary input/output of the register, inputs/outputs of flip-flops, and signal lines from fanout point to XOR gate that are on the path $(x, y_1, y_2, \ldots, y_k, z)$. *Feed signal lines* are feed-forward/feedback lines from fanout-point to XOR gate that are not on the path $(x, y_1, y_2, \ldots, y_k, z)$. The faults on *basic signal lines* are single stuck-at-0 and stuck-at-1 faults on the primary input/output of the register, inputs/outputs of flip-flops, and basic signal lines from fanout point to XOR gate. The faults on *feed signal lines* are single stuck-at-0 and stuck-at-1 faults on feed-forward and feedback lines from fanout point to XOR gate.

We also consider *resettable* LF^{2}SRs and LFSRs, i.e., LF^{2}SRs and LFSRs *with reset*. The stuck-at fault on the reset signal line may fail to initialize the circuit under test. One way to resolve this issue is to make the reset signal line observable, i.e., to make it a primary output of the circuits. Then, the stuck-at-0 and stuck-at-1 faults on the reset signal line are easily tested. In the following discussion, we therefore focus on single stuck-at faults only on basic signal lines and feed signal lines.

In general, a test sequence varies with the circuit to be tested, and hence test generation is required for every circuit. The test generation for sequential circuits is usually very hard and expensive. Since LF^{2}SRs and LFSRs are sequential circuits, it would be very hard to generate a test sequence with high fault coverage. To check it, we did an experiment using a commercial ATPG, TetraMAX. TetraMAX was executed on RHEp Linux workstation 7.3 (Intel Xeon CPU ES-1660 v4, 16 Core 3.2GHz, 32GB Memory). Table 1 shows the experimental result for six LF^{2}SRs and six LFSRs, where all circuits have reset signal lines. The limit of backtracking was set to 1000 for each fault. From Table 1, we can see that TetraMAX cannot always generate a test sequence with high fault coverage even for 64-stage LF^{2}SRs and LFSRs.

To resolve this issue, we consider the possibility of *universal testing* for LF^{2}SRs and LFSRs. First, we define a

Table 2 Fault simulation with universal test sequence.

Circuit	Fault coverage of reset+$0^{k+1}1\,0^{2k}$	Length of universal test sequence
LF^{2}SR32a	100 %	99
LF^{2}SR32b	100 %	99
LF^{2}SR32c	100 %	99
LF^{2}SR64a	100 %	195
LF^{2}SR64b	100 %	195
LF^{2}SR64c	100 %	195
LFSR32a	100 %	99
LFSR32b	100 %	99
LFSR32c	100 %	99
LFSR64a	100 %	195
LFSR64b	100 %	195
LFSR64c	100 %	195

universal test sequence as follows.

Definition 1: Let S be a set of circuits. If a test sequence T can detect all faults of any circuit in S, T is called a *universal test sequence* of S.

From this definition, we can see that if there exists a universal test sequence for a class of circuits and we know the universal test sequence, then no test generation is necessary for any circuit in the class, and the cost of test generation is zero. Universal testing is performed with a test sequence that is independent of the function realized by the circuit. Usually, such a universal test sequence depends only on the size of the circuit.

LF^{2}SRs and LFSRs consist of only flip-flops and XOR gates. Since the combinational logic parts in LF^{2}SRs and LFSRs realize linear logic functions consisting only of XOR gates, we can expect that there might exist a universal test sequence for LF^{2}SRs and LFSRs.

We did another experiment for the same circuits as shown in Table 1. Table 2 shows the result of fault simulation with a test sequence reset+$0^{k+1}1\,0^{2k}$ such that reset is applied, followed by $k+1$ consecutive 0's, followed by 1, and followed by 2k consecutive 0's where k is the number of flip-flops. From Table 2, we can see 100% of fault coverage is achieved by reset+$0^{33}1\,0^{64}$ for 32-stage LF^{2}SRs and LFSRs with reset, and by reset+$0^{65}1\,0^{128}$ for 64-stage LF^{2}SRs and LFSRs with reset, respectively. Hence this test sequence reset+$0^{k+1}1\,0^{2k}$ seems to be a universal test sequence. Here, let us compare the fault coverage and the length of test sequence in Table 1 with those in Table 2. Obviously, the results in Table 2 are much superior to the results in Table 1 with respect to both fault coverage and test sequence length.

As mentioned in the previous section, the cardinality of the class of k-stage LF^{2}SRs and LFSRs is $2(2^{k(k+1)/2}-1)$, which is a huge number. Hence, it is not obvious whether there exists a universal test sequence for the class of k-stage LF^{2}SRs and LFSRs. In the following sections, we show that there exists a universal test sequence for both classes of k-stage LF^{2}SRs and LFSRs.

For test generation, a sequential circuit can be modeled as an iterative combinational circuit or a *time expansion model*. For example, Fig. 3 illustrates an iterative combinational circuit with p time frames expanded from R_1 of Fig. 1 (a). Figure 4 illustrates an iterative combinational circuit with p time frames expanded from R_2 of Fig. 2 (a). By observing Fig. 3 and Fig. 4, we can see the structural characteristics of LF^{2}SRs and LFSRs, as shown in Fig. 5 and Fig. 6, respectively.

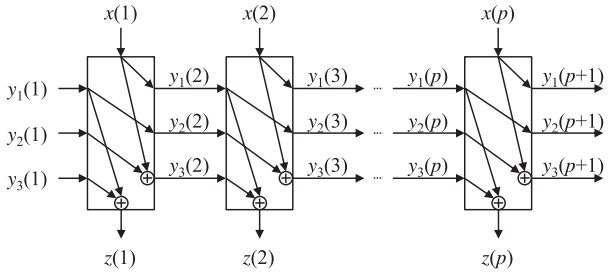


Fig. 3 Time expansion model of R_1.

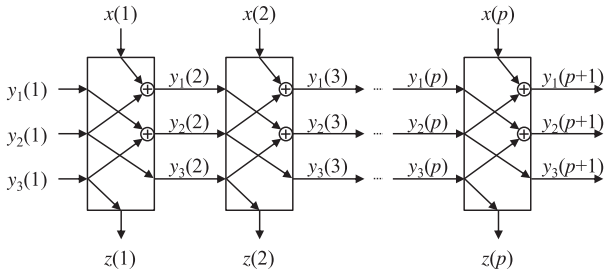


Fig. 4 Time expansion model of R_2.

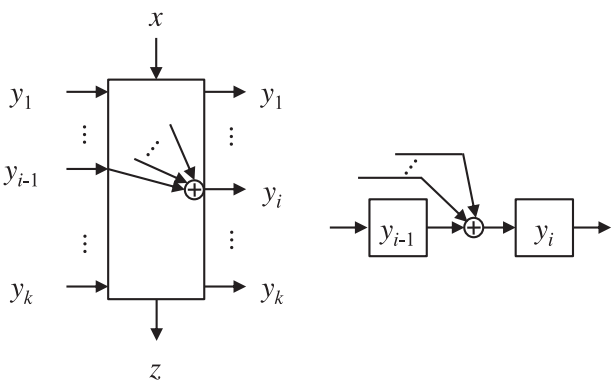


Fig. 5 Structural characteristics of LF^{2}SRs.

A single stuck-at fault f in a sequential circuit is modeled as a multiple stuck-at fault in the corresponding iterative combinational circuit such that f exists in every time frame.

Using a time expansion model, we can prove the theorems for universal testing of LF^{2}SRs and LFSRs. First, we consider the theorem for LF^{2}SRs in the following.

4. Theorem for LF^{2}SRs

In this section, we consider the theorem for universal testing of LF^{2}SRs. First, we consider stuck-at faults on basic signal lines, i.e., stuck-at faults on the primary input/output, in-

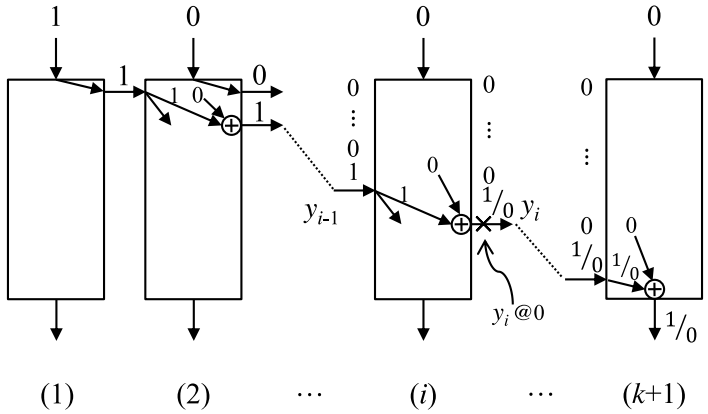


Fig. 7 LF^{2}SR testing for y_i s-a-0 fault.

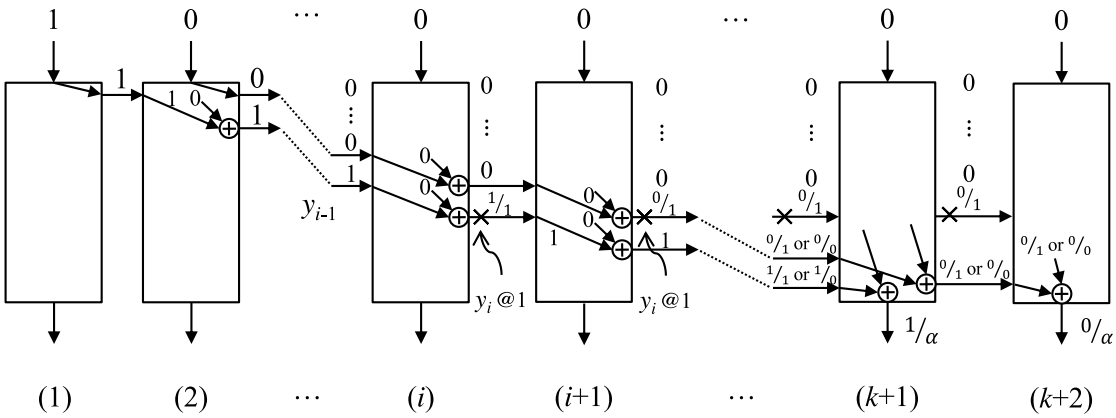


Fig. 8 LF^{2}SR testing for y_i s-a-1 fault.

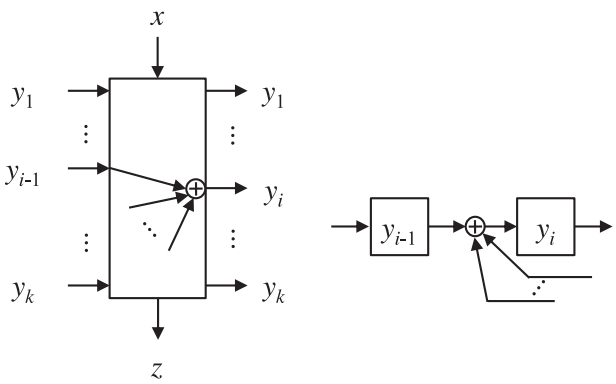


Fig. 6 Structural characteristics of LFSRs.

puts/outputs of flip-flops, and basic signal lines from fanout point to XOR gate. The test sequence $1\,0^{k+1}$ represents one followed by k+1 zeros.

Lemma 1: For the class of k-stage LF^{2}SRs, $1\,0^{k+1}$ is a universal test sequence that detects any single stuck-at fault on basic signal lines.

Proof: Let C be any k-stage LF^{2}SR. First suppose a stuck-at-0 fault on the output of flip-flop y_i. The behavior of C to which the test sequence $1\,0^{k+1}$ is applied can be illustrated by the time expansion model of C as shown in Fig. 7. As shown in Fig. 7, the stuck-at-0 fault is activated at time frame i, and the resulting error is $1/0$ where fault-free value of $y_i(i)$ is 1 and faulty value of $y_i(i)$ is 0. Since the fault is stuck-at-0, both fault-free and faulty values of y_i are the same after time frame i. Therefore, the error $1/0$ activated at time frame i is propagated to the primary output along a single path as shown in the figure.

Similarly stuck-at-0 faults on the primary input/output, inputs of flip-flops, and basic signal lines from fanout point to XOR gate are also detected by the test sequence $1\,0^{k+1}$.

Next, suppose a stuck-at-1 fault on the output of flip-flop y_i. The behavior of C to which the test sequence $1\,0^{k+1}$ is applied can be illustrated by the time expansion model of C as shown in Fig. 8. In this case, as different from the case of stuck-at-0 fault, the stuck-at-1 fault is not activated at time frame i because both fault-free and faulty values of $y_i(i)$ are the same, i.e., $1/1$.

However, the activation occurs at time frame $i+1$, i.e., fault-free value of $y_i(i)$ is 0 and faulty value of $y_i(i)$ is 1, and the resulting error is $0/1$. For the fault-free circuit, the values 1 and 0 are propagated to the primary output at time frame $k+1$ and $k+2$, respectively. On the other hand, for the faulty circuit, the values propagated to the primary output at time $k+1$ and $k+2$ are the same, because the internal

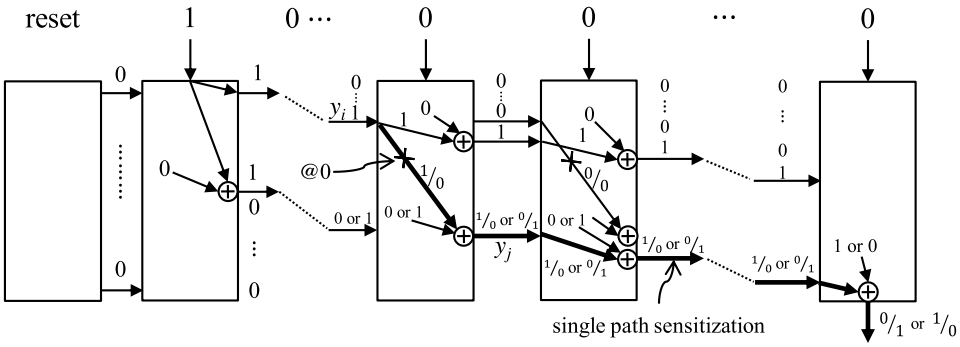


Fig. 9 LF^{2}SR testing for feed-forward line $(y_i - y_j)$ s-a-0 fault.

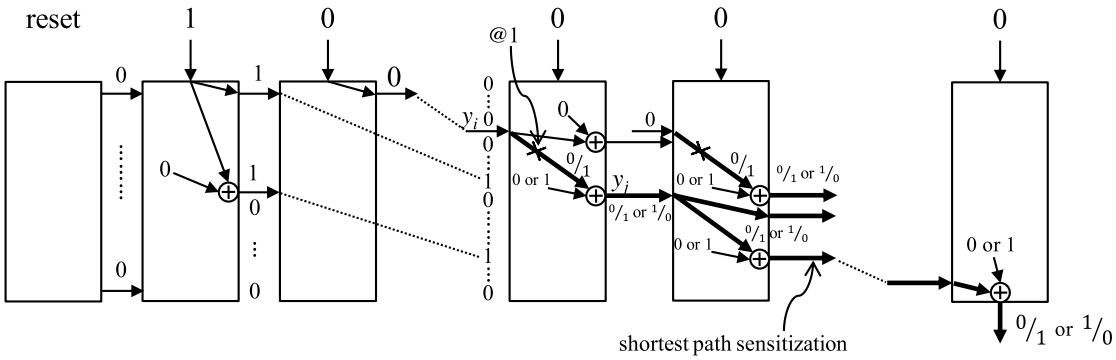


Fig. 10 LF^{2}SR testing for feed-forward line $(y_i - y_j)$ s-a-1 fault.

states of $(y_1, y_2, \ldots, y_i)$ at time i and $i+1$ are the same, i.e., $(0, 0, \ldots, 0, 1)$, and the input sequences after time i and i+1 are the same. Therefore, the error caused by the fault can be detected at the primary output either at time $k+1$ or $k+2$.

Similarly, stuck-at-1 faults on the primary input/output, inputs of flip-flops, and basic signal lines from fanout point to XOR gate are also detected by the test sequence $1\,0^{k+1}$.

□

Next, we consider universal testing for stuck-at faults on feed signal lines. To guarantee the detection of stuck-at faults on feed signal lines, we consider *resettable* LF^{2}SRs. The test sequence reset+1 0^{k+1} represents reset followed by input sequence $1\,0^{k+1}$.

Lemma 2: For the class of k-stage resettable LF^{2}SRs, reset+1 0^{k+1} is a universal test sequence that detects any single stuck-at fault on feed signal lines.

Proof: Let C be any k-stage LF^{2}SR. The behavior of C to which the test sequence reset+1 0^{k+1} is applied can be illustrated by the time expansion model of C as shown in Fig. 9. As shown in Fig. 9, suppose a path from the output of flip-flop y_i to the input of flip-flop y_j. On this path, suppose a line which starts from the fanout point of the output of y_i and ends at the XOR gate of the input of y_j. Let us call this line the feed-forward line from y_i to y_j, and denote it as $(y_i - y_j)$.

First suppose a stuck-at-0 fault on the feed-forward line $(y_i - y_j)$. As shown in Fig. 9, the stuck-at-0 fault on the feed-forward line is activated at the time frame when value 1 appears at y_i, and the resulting error $1/0$ propagates to y_j. After this time frame, the faulty feed-forward line is not activated, i.e., $0/0$. Therefore, the error caused by the fault is propagated to the primary output along a single path as shown in the figure.

Next suppose a stuck-at-1 fault on the feed-forward line $(y_i - y_j)$. The behavior of C to which the test sequence reset+1 0^{k+1} is applied can be illustrated by the time expansion model of C as shown in Fig. 10. As shown in the figure, the stuck-at-1 fault on the feed-forward line is activated at the time frame when value 0 appears at y_i, and the resulting error $0/1$ propagates to y_j. The error propagated to y_j becomes $0/1$ or $1/0$ depending on the internal state of the time frame. The error then continues to propagate along the shortest path to the primary output. Other errors which occur after the first error never catch up with the first error, and hence never violate sensitization on the shortest path. Therefore, the error caused by the fault is propagated to the primary output as shown in the figure.

□

From Lemma 1 and Lemma 2, we have the following Theorem 1.

Theorem 1: For the class of resettable k-stage LF^{2}SRs, reset+1 0^{k+1} is a universal test sequence that detects any single stuck-at fault on basic signal lines and feed signal lines.

5. Theorem for LFSRs

In this section, we consider the theorem for universal testing of LFSRs. First, we consider stuck-at-0 faults on basic signal lines, i.e., stuck-at-0 faults on the primary in-

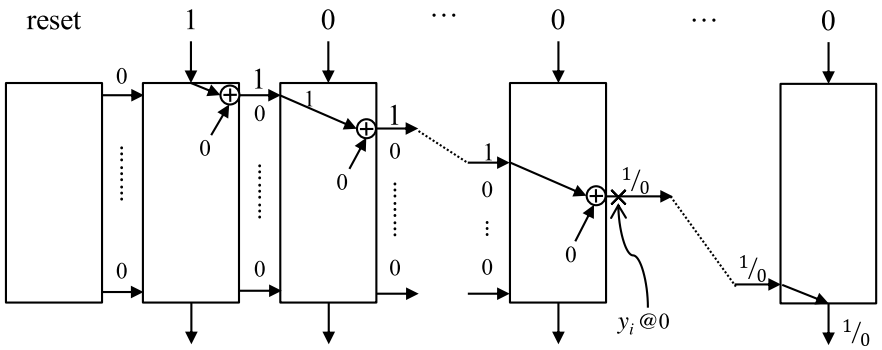


Fig. 11 LFSR testing for y_i s-a-0 fault.

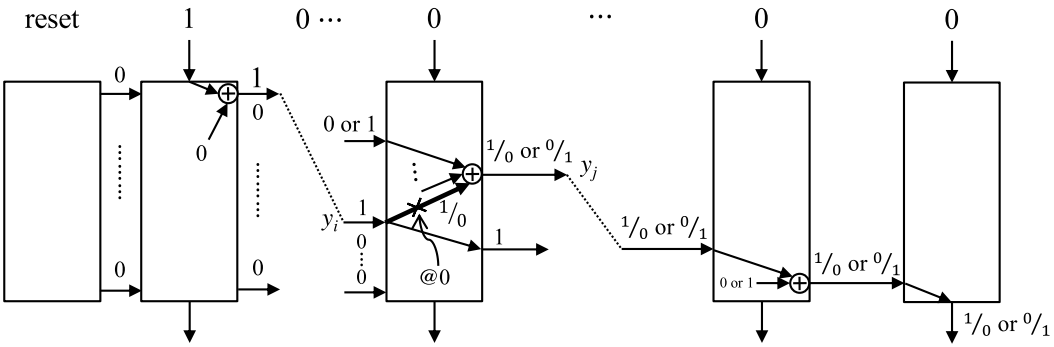


Fig. 12 LFSR testing for feedback line $(y_i - y_j)$ s-a-0 fault.

put/output, inputs/outputs of flip-flops, and basic signal lines from fanout point to XOR gate.

Lemma 3: For the class of resettable k-stage LFSRs, reset+1 0^k is a universal test sequence that detects any single stuck-at-0 fault on basic signal lines.

Proof: Let C be any k-stage LFSR. First suppose a stuck-at-0 fault on the output of flip-flop y_i. The behavior of C to which the test sequence reset+1 0^k is applied can be illustrated by the time expansion model of C as shown in Fig. 11. As shown in Fig. 11, the stuck-at-0 fault is activated at the time frame when value 1 appears at y_i, and the resulting error is $1/0$ where fault-free value of $y_i(i)$ is 1 and faulty value of $y_i(i)$ is 0. The error $1/0$ is propagated to the primary output along a single path as shown in the figure.

Similarly stuck-at-0 faults on the primary input/output, inputs of flip-flops, and basic signal lines from fanout point to XOR gate are also detected by the test sequence reset+1 0^k.

□

Next, we consider stuck-at-0 faults on feed signal lines. We have the following lemma.

Lemma 4: For the class of resettable k-stage LFSRs, reset+1 0^{2k} is a universal test sequence that detects any single stuck-at-0 fault on feed signal lines.

Proof: Let C be any k-stage LFSR. First suppose a stuck-at-0 fault on the feedback line $(y_i - y_j)$. The behavior of C to which the test sequence reset+1 0^{2k} is applied can be illustrated by the time expansion model of C as shown in Fig. 12. As shown in Fig. 12, the stuck-at-0 fault on the feedback line $(y_i - y_j)$ is activated at the time frame when value 1 appears at y_i, and the resulting error $1/0$ propagates to y_j. After this time frame, the error caused by the fault is propagated to the primary output along a single path as shown in the figure. The longest test sequence reset+1 0^{2k} is necessary when the feedback line $(y_k - y_1)$ is tested.

□

Next, we consider stuck-at-1 faults on basic signal lines and feed signal lines, i.e., stuck-at-1 faults on the primary input/output, inputs/outputs of flip-flops, basic signal lines from fanout point to XOR gate, and feedback lines. We have the following lemma.

Lemma 5: For the class of resettable k-stage LFSRs, reset+0^{k+1} is a universal test sequence that detects any single stuck-at-1 fault on basic signal lines and feed signal lines.

Proof: Let C be any k-stage LFSR. First suppose a stuck-at-1 fault on the output of flip-flop y_i. The behavior of C to which the test sequence reset+0^{k+1} is applied can be illustrated by the time expansion model of C as shown in Fig. 13. As shown in the figure, the stuck-at-1 fault is activated at the first time frame after reset, and the resulting error $0/1$ is propagated to the primary output along a single path as shown in the figure.

Similarly stuck-at-1 faults on the primary input/output, inputs of flip-flops, and basic signal lines from fanout point to XOR gate are also detected by the test sequence reset+0^{k+1}.

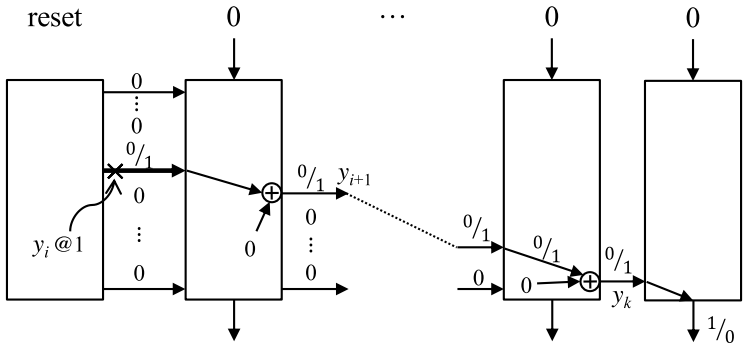


Fig. 13 LFSR testing for y_i s-a-1 fault.

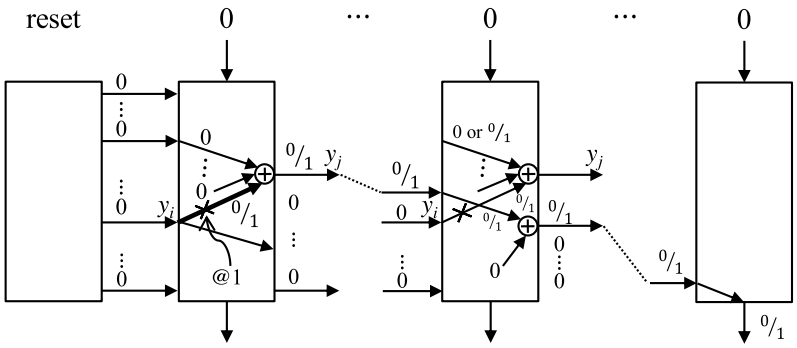


Fig. 14 LFSR testing for feedback line $(y_i - y_j)$ s-a-1 fault.

Next suppose a stuck-at-1 fault on the feedback line $(y_i - y_j)$. The behavior of C to which the test sequence reset+0^{k+1} is applied can be illustrated by the time expansion model of C as shown in Fig. 14. As shown in the figure, the stuck-at-1 fault on the feedback line $(y_i - y_j)$ is activated at the first time frame after reset, and the resulting error $0/1$ propagates to y_j. The error propagated to y_j becomes $0/1$ or $1/0$ depending on the internal state of the time frame. Other errors which occur after the first error never catch up with the first error, and hence never violate sensitization of the first error. Therefore, the error caused by the fault is propagated to the primary output as shown in the figure.

□

From Lemmas 3, 4 and 5, we have the following theorem.

Theorem 2: For the class of resettable k-stage LFSRs, reset+$0^{k+1}1\,0^{2k}$ is a universal test sequence that detects any single stuck-at fault on basic signal lines and feed signal lines.

Proof: First, consider stuck-at-0 faults on basic signal lines. From Lemma 3, reset+$1\,0^k$ detects those faults. Since reset+$0^{k+1}1\,0^{2k}$ covers reset+$1\,0^{k+1}$, reset+$0^{k+1}1\,0^{2k}$ also detects any stuck-at-0 fault on basic signal lines.

Next, consider stuck-at-0 faults on feed signal lines. From Lemma 4, reset+$1\,0^{2k}$ detects those faults. Since reset+$0^{k+1}1\,0^{2k}$ covers reset+$1\,0^{2k}$, reset+$0^{k+1}1\,0^{2k}$ also detects any stuck-at-0 fault on feed signal lines.

Finally, consider stuck-at-1 faults on basic signal lines and feed signal lines. From Lemma 5, reset+0^{k+1} detects those faults. Since reset+$0^{k+1}1\,0^{2k}$ covers reset+0^{k+1}, reset+$0^{k+1}1\,0^{2k}$ also detects any stuck-at-1 fault on basic signal lines and feed signal lines.

Therefore, reset+$0^{k+1}1\,0^{2k}$ detects any single stuck-at fault on basic signal lines and feed signal lines.

□

6. Theorem for LF^{2}SRs and LFSRs

Theorem 1 shows that reset+$1\,0^{k+1}$ is a universal test sequence for the class of resettable k-stage LF^{2}SRs. Since reset+$0^{k+1}1\,0^{2k}$ covers reset+$1\,0^{k+1}$, reset+$0^{k+1}1\,0^{2k}$ is also a universal test sequence for the class of resettable k-stage LF^{2}SRs. From Theorem 2, reset+$0^{k+1}1\,0^{2k}$ is a universal test sequence for resettable k-stage LFSRs. Therefore, reset+$0^{k+1}1\,0^{2k}$ is a universal test sequence for both resettable k-stage LF^{2}SRs and LFSRs. Then, we have the following Theorem 3.

Theorem 3: For the class of resettable k-stage LF^{2}SRs and LFSRs, reset+$0^{k+1}1\,0^{2k}$ is a universal test sequence that detects any single stuck-at fault on basic signal lines and feed signal lines.

7. Conclusion

In this paper, we considered universal testability for linear feed-forward shift registers (LF^{2}SRs) and linear feedback shift registers (LFSRs). As an experimental result, we

showed that the test generation of LF^{2}SRs and LFSRs is very hard and a high fault coverage cannot be obtained by a commercial ATPG. To resolve this issue, we considered universal testability for the class of LF^{2}SRs and LFSRs. We showed that there exists a universal test sequence with 100% of fault coverage for the class of LF^{2}SRs and LFSRs. We proved the existence theorem of universal test sequences for the class of LF^{2}SRs and LFSRs. We showed that universal test sequences are much superior to the test sequences generated by a commercial ATPG with respect to both fault coverage and test sequence length.

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