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Reduction of Test Data Volume and Improvement of Diagnosability Using Hybrid Compression

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SUMMARY This paper describes a simple means to enable direct diagnosis by bypassing MISRs on a small set of tests (MISR-bypass test mode) while achieving ultimate output compression using MISRs for the majority of tests (MISR-enabled test mode.) By combining two compression schemes, XOR and MISRs in the same device, it becomes possible to have high compression and still support compression mode volume diagnostics. In our experiment, the MISR-bypass test was first executed and at 10% of the total test set the MISR-enabled test was performed. The results show that compared with MISR+XOR-based compression the proposed technique provides better volume diagnosis with slightly small (0.71 X to 0.97 X) compaction ratio. The scan cycles are about the same as the MISR-enabled mode. A possible application to partial good chips is also shown.

key words: *test compression, hybrid compression, volume diagnosis, ATPG, partial good chip*

1. Introduction

Advanced test methodologies for digital circuits have evolved with technology over the years [1]. Due to the large test data volume in recent test process, non-compression mode test data is difficult to be supported on traditional ATEs although the traditional test data can ensure the best diagnosability. In order to reduce ever-growing pattern sizes, logic built-in self test (LBIST) showed much promise in the 1980 s [2], as an improvement to existing automatic test pattern generation (ATPG) methodologies. The benefit of LBIST was to compress both stimulus and response data dramatically, although usually with a drop in fault coverage in spite of a huge increase in the number of test cycles applied [3], [4]. Recently, compression techniques obtain much of the stimulus and response compression of LBIST while yielding the high coverage expected from ATPG. Some of them have decompressor and multiple input signature registers (MISRs) [5]–[9] and others utilizes a linear feedback shift registers (LFSRs) and MISRs [10], [11].

Response compression schemes in use today primarily rely on a linear compactor that is either combinatorial or sequential. The combinatorial compactors are typically just a set of XOR trees of various complexities [8]. The sequential compactors are of either finite or infinite memory (in terms of their sequential depth). A finite memory compactor holds onto compacted data for some finite number of cycles. Because it does not hold the (compressed) response data for an infinite number of cycles, finite memory compactors must have their outputs observed during the compaction process so as not to lose any of the possibly captured errors.

MISR is an example of an infinite memory compactor since it can continue to re-circulate compressed responses until it is reset. A disadvantage of MISR based compression is that the source of a defective response cannot generally be located using only a small set of failing signatures [12]. More recent results indicate that diagnosing from failing signatures may sometimes be possible [13], but while results may look promising for diagnosing defects that mimic simple fault models, real defects often do not match the fault model behavior and may make such analysis more error prone.

To get around that problem, compression schemes that use MISRs typically require a failing test to be applied twice: once to detect a failure via a bad signature; and a second time to scan the test response off chip either dumped to the automatic test equipment (ATE) or compared with expected response streams on the ATE [14]. As long as most tests pass, the penalty for applying failing tests twice is relatively small. Also, many testers have limited fail buffer space that typically limits fail data collection just to a few failing tests, further mitigating the costs of using a MISR; however, not everyone has (ATE) software capable of conditionally applying a test twice.

Due to the diagnosis issue with MISR based compression technology, the industry has leaned towards using the space expander and compactor based compression technology which is much simpler to diagnose. Space expander and space compactor based compression technology came up as an alternative solution where the users no longer need to apply the test vectors on the ATE twice; however the compression ratio of this compression technology was still smaller comparing to the MISR based technology. The question becomes whether it is possible to use a MISR to obtain its benefits and still be able to diagnose failures without a cumbersome approach to applying the tests on the ATE.

In 2005, two of the authors [15] proposed use of streaming MISR outputs (observe the MISRs on each scan cycle) as a means to allow diagnostics to be performed on tests that produced the MISR output streams. In this paper we propose an alternative scheme that allows the infinite memory of MISRs to be bypassed for a limited number of

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tests, useful for performing volume diagnostics.

This paper is organized as follows. In Sect. 2, we show the diagnosis technique for MISR-base test. In Sect. 3 we propose a hybrid test compression scheme along with ATPG method, followed in Sect. 4 by three experimental results in the real circuits. In Sect. 5 the proposed technique is applied to partial good chips. Section 6 concludes the paper.

2. MISR Signature-Based Diagnosis

For LBIST, diagnostics has always been a somewhat complicated process. Generally, LBIST tests apply many scan cycles between checking of signatures. An LBIST signature is typically accumulated across many thousands of scan cycles before it is checked. A mismatching signature simply indicates that a failure has occurred, but cannot precisely identify where the failure occurred. Once a failure is detected, the sequence of LBIST cycles is re-applied and the intermediate signatures are compared in an attempt to locate a small range of LBIST cycles where a defective response is first seen. Given that small range of cycles, those cycles are applied again, but the responses are scanned out to the tester instead of into the MISR so that the complete internal responses can be compared for diagnostic processing [14].

Anyone currently performing diagnostics of LBIST is likely to have experience in applying tests multiple times in order to collect the diagnostic fail data. The fail data collection is further complicated by the fact that LBIST signatures accumulate across tests, making it difficult to restart LBIST past the first failing pattern so as to locate the next failing pattern.

Some of the complexity of LBIST diagnostics is avoided when using a MISR to compress stored pattern response data. First, the signatures are typically compared at the end of each test, so there is no searching to locate the failing test. Second, the MISRs are usually reset between tests, so there is no sequential propagation of failure responses from one test to the next via the signature - if a signature is bad, the last test applied is the culprit.

Checking the signature at the end of each test provides a simple means to detect which test produced the error response, but there is still the need to collect more data to drive the diagnostic process. This is traditionally done the same as for LBIST: by re-applying the failing test and then scanning the internal responses out to the ATE instead of into the MISR. An alternative approach sometimes used: create a new tester program that contains just the failing tests for a set of chips and apply all of those tests by scanning out to the tester instead of into the MISR.

3. Hybrid Compression Approach

3.1 Streaming Outputs

One reason that a MISR is good for detecting errors is that it captures the fact that it saw an erroneous response and continues to recirculate the error bits within it until the signature is read out. In the case of LBIST, the MISR is read out for comparison infrequently, but in the case of compression schemes such as OPMISR+ [5], the MISR states are usually observed after each test. Shown in Fig. 1 is a more generalized compression scheme, including masking logic, that allows use of MISRs or bypassing of them. Without the MUXes between MISRs and Space Compactor the configuration is a standard OPMISR+ scheme. In a stand alone Space Compactor compression technology, as can be seen in Fig. 1, there is a Space Expander (Spreader Network) on the input side which takes the original chip scan inputs as its input and expands them out to multiple scan chains. Actually scan chains in regular scan mode are broken down into multiple smaller scan chains in between the spreader and compactor to match the compression ratio that the user wants to achieve. These scan chains are the compacted together using a space compactor on the output side to match the number of the scan outputs available. From a hardware structure point of view, the Space Expander+Space compactor based compression technology is lot simpler comparing to the MISR based OPMISR+ compression technology. This space compactor based compression approach is able to resolve the diagnosability issue, but is unable to achieve as high compression ratio as the MISR based OPMISR+ approach can. This is the reason why the dual compression approach has been proposed in this thesis not only to enable the users to achieve higher test data volume compression ratio, but also to achieve diagnosability. Here, the Mask Registers are used to mask out unpredictable (X) response values before they enter the MISRs, which would cause their final signatures to become unpredictable [16].

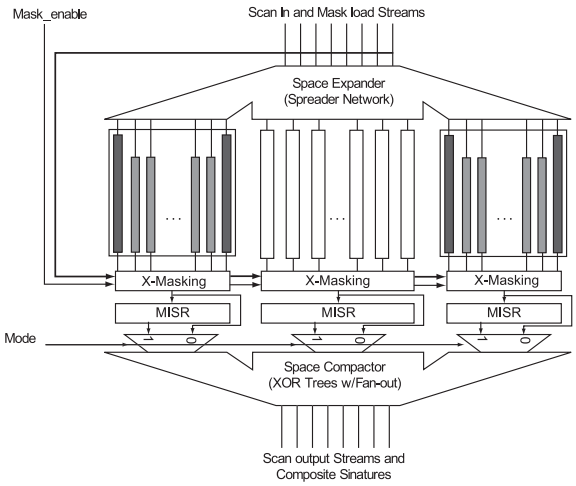

Fig. 1 MISR-based hybrid compression structure.

It was shown in [15] that the space compactor signatures could be observed every scan cycle, producing a stream of compressed output data that can be utilized to perform diagnostics. This stream of values at the output of the space compactor pins looks very similar to standard scan-out streams.

3.2 MISR MUXing

An alternative to observing the MISR outputs on each scan cycle is to bypass the MISRs observing the internal chain outputs through the space compactor directly. Diagnosing fails that propagate through the space compactor is somewhat simpler to do without concern for the feedback aspects of the MISRs. The MISRs may be in the design just for use compressing stored pattern responses or may exist for Logic BIST. The point is that it is reasonable to consider application of some tests that bypass the MISRs and additional tests that utilize the MISRs for additional response compression.

As shown in Fig. 1, adding a layer of MUXes between the MISRs and Space Compactor allows use of MISRs or bypassing of them. A similar effect can be obtained by switching the MISRs into a single pipeline stage.

When the bypass signal Mode=1, the chain outputs (after masking) go into the MISRs and the final MISR signatures are read out through the space compactor that consists of XOR trees with fan-outs.

When Mode=0, the chain outputs are observed via the space compactor directly, allowing for direct diagnosis of fail data. The scan input streams are decompressed using the combinatorial form of SmartBIST [17], but would also work with regular fan-out.

Since volume diagnostics for manufacturing test can be performed with data collected from just a few failing tests and since test fails predominantly occur within the first 10% of the test patterns, it is reasonable to consider use of compression that bypasses the MISRs for the first 10% of the tests so that full manufacturing diagnostics can be performed for the vast majority of tester fails and then use the MISR based compression for the final 90% of the tests to obtain the higher compression rate provided by MISRs.

Compared to an OPMISR+ structure, there is certain overhead added for the hybrid compression structure. For each channel, one MUX is added to bypass the channel response from the MISRs. Compared to a purely combinatorial XOR compactor network, the overhead is a little bit more in the sense that there are MISRs in between the channels and compactor. For each channel, MISR based approach needs one additional register bit and a MUX for bypassing compared to XOR compactor based approach. This register bit loops the channel value anti-clockwise with other register bits inside the MISR and generates & keeps the final value during the measure event. Since the basic structure is about the same as XOR or OPMISR+ compression, the chip overhead is very limited. If the bypass signal can be shared as noted above, there is no additional control primary input needed.

3.3 ATPG Methodology

The ATPG methodology for using this hybrid compression strategy can be described using the flow chart shown in Fig. 2. In the first step, we run ATPG to full coverage using

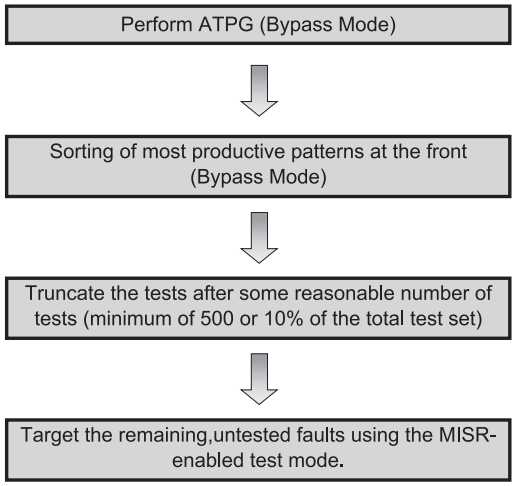

Fig. 2 ATPG flow methodology.

the MISR bypass test mode. The total fault set is targeted in this mode and then a certain amount of ATPG patterns are generated. The test generator calls the simulator internally to simulate the generated test patterns and check each fault is detected or not by the generated pattern.

In this mode the test data is not compressed by the MISR but by the space compactor only. As the test data is compressed by the XOR based space compactor, the test data volume compression ratio is not as big as the MISR based approach. However, it does provide the flexibility to be able to diagnose without any additional ATE time in case of failure. In this process, these test vectors are sorted according to the number of faults they can detect. And then, we truncate the test vectors to keep approximately the best 10% of the sorted tests.

In the final step, ATPG in the MISR-enabled mode targets the remaining untested faults left over by the bypass mode. In this stage, these remaining faults become the targets of the ATPG engine. So, it is the simulator that keeps track of the "Tested" and "Untested" faults in the fault list. The combined set of tests collectively covers all faults and consumes less data volume.

The steps of running ATPG, sorting, truncating and running ATPG again to target remaining faults is often used today as a means to reduce the number of tests applied to the circuit. The only real change is that the follow-up ATPG is performed using a different test mode in order to obtain a higher rate of compression for the response data. So, in the final step, we need to switch to a MISR-enabled test mode from the MISR-bypass mode and then run ATPG on the remainder of the faults.

3.4 Dealing with Unknown Responses

When bypassing MISRs and using only the space compactor, it is not critical that unknown responses are removed before entering the compression logic. We remove them only when not doing so would result in the loss of a tar-

geted fault's detection. This can greatly reduce the amount of masking used and can thus result in an overall improvement in the compression rate. For tests that use the MISRs, it is imperative that any unknown values be removed before they get into a MISR; use of masking may be higher for tests that use the MISR.

3.5 Diagnosis of Fails

As reported in [15], we attempt to solve the linear equations that can explain tester fails. When it is not possible to solve the equations (to point to less than a few fail source chains), all scan bits that could potentially be the fail bit capture points are included as "possible fail" locations. We depend on the simulation of the faults in the back cones of the fail bits and possible fail bits (for both failing and passing patterns) to weed out the incorrect fail locations from the true ones. Our results for this scheme turned out to be pretty effective and logical.

Occasionally there will be cases where the fails occur during tests that use the MISRs. In most cases it will be correct to simply avoid diagnosing such fails; however, in the case where these fails occur such that they are yield limiting, they must be diagnosed. When this happens there are three approaches that can be utilized:

(1) Apply the failing tests a second time and before scanning out the results, switch to a full scan mode to dump the full content of the scan bits. This is the traditional approach.
(2) Apply the failing tests a second time and before scanning out the results, switch to the MISR bypass mode to scan out compressed responses.
(3) Apply the failing tests a second time and observe the composite MISR signatures on each scan cycle to permit collecting enough fail data to permit diagnostics [15].

4. Experimental Results

4.1 ATPG Results

We have applied the compression technique shown in Fig. 1 to the modest sized designs shown in Table 1. The first column is the name of designs. The number of gates and the number of scan-in/out are shown in the second and third column. From the forth to seventh column chain data is provided for full scan and compression test modes.

We ran ATPG in the Full scan test mode (non-compression mode) first to get an idea about the test coverage, the number of total test patterns and the test data volume. The data in Table 2 shows the test coverage, data volume, number of tests and scan cycle information in different test modes. This table compares the above mentioned parameters among non-compression (Fullscan), MISR+XOR, MISR-bypass and Hybrid Compression modes.

The total data volume and test time for this hybrid methodology is obtained by adding the values for the 10% MISR bypass to those for the MISR add-on. For example, for design A, the final hybrid compression data volume is 0.14 M scan bits compared with the 0.29 M for space compactor (MISR bypassed) only vectors. The test time is 12.6 K scan cycles as compared with the MISR-bypass' 12 K cycles. The first 10% of test pattern achieves 90.92% of fault coverage, while the final fault coverage is 95.09% for this ATPG test set. In other words, 90.92% of the target faults can be detected and hopefully diagnosed by the first 10% of test vectors. Similarly, for designs B and C 93.53% and 92.46% of faults are detected by the first 10% of test set.

In practice, more than 90% of device fails will occur

Table 1 Designs used for experiments.

Design	# gates	# si/so	Chain data for test modes			
			Full scan		Compression	
			# chains	longest	# chains	longest
A	90 K	8/8	8	243	48	40
B	1.2 M	16/16	16	2206	320	108
C	1.6 M	16/16	16	2881	320	142

Table 2 ATPG experimental results for three designs.

Design	Test Coverage (%)	Full scan			MISR-enabled (MISR+XOR)			MISR-bypass			Hybrid Compression						
											10% MISR Bypass				Overall Stats		
											MISR Add-ON						
		Number of Tests	Data Volume (M)	Scan Cycle (K)	Number of Tests	Data Volume (M)	Scan Cycle (K)	Number of Tests	Data Volume (M)	Scan Cycle (K)	Test Coverage (%)	Number of Tests	Data Volume (M)	Scan Cycle (K)	Number of Tests	Data Volume (M)	Scan Cycle (K)
A	95.12	295	1.7	72	300	0.1	12	300	0.29	12	90.92	47	0.05	1.9	314	0.14	12.6
											95.09	267	0.09	10.7			
B	98.52	2549	269	5623	2719	4.7	295	2728	14.1	295	93.53	264	1.4	29	2267	4.9	245
											98.62	2003	3.5	216			
C	98.64	3844	532	11074	4160	9.5	590	5726	39	813	92.46	572	3.9	81	4020	11.8	571
											98.65	3450	7.9	490			

Table 3 Comparison of savings on data volume and scan cycle time.

Design	MISR-enabled (MISR+XOR)		MISR-bypass		Hybrid-Compression	
	Data Volume	Scan Cycles	Data Volume	Scan Cycles	Data Volume	Scan Cycles
A	17 X (1.0)	6 X (1.0)	6 X (0.35)	6 X (1.0)	12 X (0.71)	6 X (1.0)
B	57 X (1.0)	19 X (1.0)	19 X (0.33)	23 X (1.21)	55 X (0.97)	23 X (1.21)
C	56 X (1.0)	19 X (1.0)	14 X (0.25)	14 X (0.74)	45 X (0.8)	19 X (1.0)

within these first 10% of tests. This shows it is practical to do volume diagnosis on fails within the first 10% of tests (using the MISR-bypass test patterns). Note that data volume is about the same or less than just using the MISR yet we gain the benefit of being able to directly diagnose most failures.

Here each experiment has been optimized based on pattern count to do a fair comparison. It is thought that because the designs are different hardwarewise in between the non-compression mode and the compression mode and the target fault locations are slightly different in every individual mode, for Design B for some reason more faults could be tested with smaller set of test patterns in the hybrid methodology.

Table 3 compares the test data volume and test application time reduction for all three schemes. The values in the parenthesis of each cell mean the relative one for MISR-enabled (MISR+XOR) test. For example, the MISR-enabled (MISR+XOR) test achieves 17 X test volume reduction and 6 X scan cycles for design A. Similarly, the MISR-bypass (XOR) test shows 6 X data volume, resulting in 0.35 times compression ratio. The scan cycles for the MISR-bypass test mode are 6 X, resulting in the same value for the MISR-enabled test mode. For the hybrid test mode, the data volume is 12 X (0.71 times) and the number of scan cycles is 6 x (1.0 time.) Compared with MISR-enabled compaction the proposed technique provides better volume diagnosis with slightly small (0.71 to 0.97) compaction ratio. The scan cycles are about the same.

It shows how our recommended hybrid compression approach reduces test data volume and test cycle time comparing to the MISR-bypass only approach and still enables direct diagnostics.

Although not shown here, it has been shown [5] that by using run-length encoding compression and repeat-fill, the input scan stimulus in the MISR mode can be further compressed by a factor of about 5 X when using a tester repeat capability. This is possible because the scan data often repeats for several contiguous cycles. This is the case as there is no scan-out data to consider.

4.2 Test Mode Migration

In general, since the decompressor is the same for both test modes, a test from one mode can easily be migrated to the other mode and all that may be required is some change to the masking data. Migration of a test from the MISR-enabled mode to the MISR bypass mode would need no modification since if that test's masking eliminates all unknown values, it will work fine in the MISR-bypass mode. If some MISR-enabled mode test happens to catch a lot of failures even after all of the bypass mode tests have be applied, migrating that test to the bypass mode to allow diagnosing those fails is trivial.

The first 10% of the MISR-bypass mode's tests detect more than 90% of the total fault population. It's reasonable to do most of the diagnostic process using fails on those first patterns so that a one pass volume diagnostic approach can use this hybrid compression structure. The data volume reductions using the hybrid compression scheme are nearly equivalent or even better than using MISRs or XOR only.

5. Application to Partial Good Chips

Many complex chips being designed today contain multiple copies of identical cores. Often these chips can be useful even if one or a few of these cores turn out to be defective. This is called a partially good device. The developers of such chips find it extremely beneficial if there is some way for them to avoid throwing away a defective chip if it could still be sold for a reduced price for reduced functionality.

One simple means for identifying when a specific core is defective is to ensure the core's scan chains feed out through pins dedicated for its scan out data. Without compression this would be very difficult to do, but with compression, it is possible to use a space compactor to compress all of a core's scan streams down to just a few scan outputs. It is important in such a scheme not to merge the outputs of several cores within the compression logic. This allows a chip with one or a few known defective cores to simply ignore the scan output and signature data for the pins associated with those cores. It is a reasonably simple responsibility for module manufacturing test to expect X on those outputs associated with the bad cores that are being allowed.

For example, suppose a chip has four cores and can be sold at a reduced price if at least two of the cores are working. If the device can support 32 scan outputs, each core can have its compressed outputs go to six chip outputs; this will consume 24 chip outputs for all four cores, leaving 8 for the compressed output of other chip logic. Then, if the chip fails during wafer test, but only at the outputs associated with core 2, the chip is designated as partially good with a

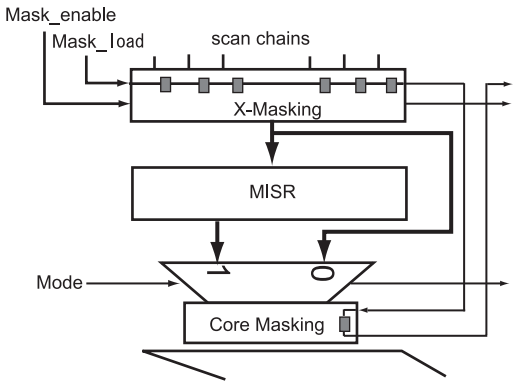

Fig. 3 Compression supporting partial good die.

bad core 2. This chip may then have fuses burned to make it work functionally with only 3 good cores. When the chip is processed at module test, the outputs associated with core 2 should be ignored.

This approach will work fine as long as you do not have too many cores such that you do not have enough chip pins to dedicate some for each core. When this happens, it may be best to use a core-level masking approach as shown in Fig. 3. This uses a mask inserted prior to the space compactor and allows each independent core's MISR (and bypass) to be forced to all zeros (or some constant value). Core-Masking logic includes only one register bit common to all MISR output and AND gates for individual MISR outputs. Core-Masking register bit is serially connected to the X-Masking registers (The number of X-Masking register bit is same as the number of scan channels) [16]. There is one mask bit for each MISR, so not much mask data is required. This allows all of the cores' chains to merge within the space compactor so that it is not a requirement to dedicate some chip output pins to each core.

Although this avoids having chip pins dedicated to each core, it does require a separate set of (compressed) output streams and signatures for each unique good core combination that legally defines a partially good chip. If only the MISR-enabled mode is used for module test, then the masking can be used to check each core's signature separately rather than in composite, with the signatures for known defective cores expected as X; this is a minor amount of additional data to have to push around with a partially good device. Alternatively, it may be possible for tester software to dynamically compute a corrected signature for each test by knowing how to subtract out a particular core's portion of the composite signature. A similar technology has been explained by Arabi in Ref. [18]. The proposed technique can be used either in conjunction with ATE or as a stand-alone BIST technique to test multiple identical blocks on the same chip whereas our approach is fully a scan based approach and do not directly rely on BIST technique or ATE for deployment/implementation.

6. Conclusions

We have described a means of using two different test modes to further improve compression results. By using MISR signatures on the majority of tests we get nearly the full advantage of having MISRs on-chip. Being able to perform diagnostics on the fails from the first 10% or so of the whole test vector set is reasonable and supports a single pass volume diagnostic approach while providing a data volume reduction that is typically 3 x better than without the MISR. The experimental results show that compared with MISR+EOX-based compaction the proposed technique provides better volume diagnosis with slightly small (0.71 X to 0.97 X) compaction ratio. The scan cycles are about the same as the MISR-enabled mode. It is shown the proposed scheme can possibly applied to partial good chips by inserting core-masking circuits.

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