PAPER *Special Section on Dependable Computing*

A Method for Minimizing Clock Skew Fluctuations Caused by Interconnect Process Variations

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SUMMARY As the LSI process technology advances and the gate size becomes smaller, the signal delay on interconnect becomes a significant factor in the signal path delay. Also, as the size of interconnect structure becomes smaller, the interconnect process variations have become one of the dominant factors which influence the signal delay and thus clock skew. Therefore, controlling the influence of interconnect process variations on clock skew is a crucial issue in the advanced process technologies. In this paper, we propose a method for minimizing clock skew fluctuations caused by interconnect process variations. The proposed method identifies the suitable balance of clock buffer size and wire length in order to minimize the clock skew fluctuations caused by the interconnect process variations. Experimental results on test circuits of 28 nm process technology show that the proposed method reduces the clock skew fluctuations by 30–92% compared to the conventional method.
key words: *clock skew, interconnect, process variation, signal delay*

1. Introduction

The clock skew is defined as the delay difference between two clock paths in an LSI chip, as shown in Fig. 1. In the high-speed LSI designs of advanced process technologies, controlling the clock skew is one of the most important issues because, if the clock skew is large, the designers have to specify a long clock period and thus the clock frequency (LSI performance) becomes lower.

The size of interconnect structure (wire width, wire thickness, and inter-layer dielectric thickness, which are shown in Fig. 2) varies among chips depending on the interconnect process, and this variation is referred to as interconnect process variation (Fig. 3). As the LSI process technology advances, the size of interconnect structure becomes smaller, whereas the amount of variation in each interconnect parameter (wire width, wire thickness, and inter-layer dielectric thickness) does not change much. Accordingly, the ratio of variation to the nominal value in each interconnect parameter has become larger, and thus the influence of interconnect process variations on the signal delay has become crucial.

If the signal delay on a circuit varies significantly depending on the interconnect process variations among chips, the clock skew fluctuations among chips are large, which makes the timing convergence difficult and also leads to lower yield. Therefore, we focus on minimizing the clock skew fluctuations which are caused by the interconnect process variations among chips.

Conventionally, there have been some researches which address the impact of process variations on clock skew. Reference [1] investigates the impact of process variations on clock skew and shows that the ratio of clock skew to clock period increases as the LSI process technology scaling. Reference [2] proposed a method for constructing *non-tree* clock networks for reducing clock skew fluctuations caused by wire width variations. But, in real LSI designs,

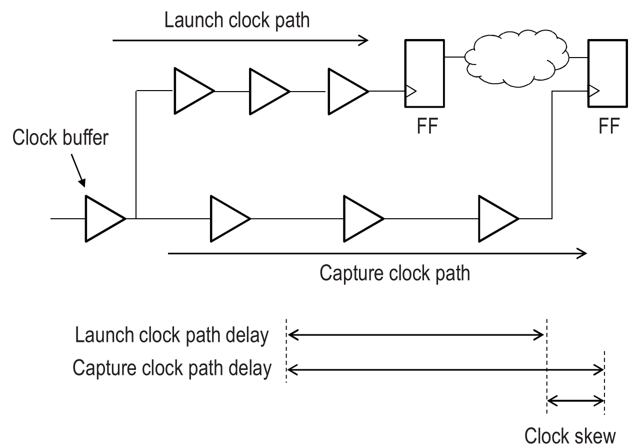

Fig. 1 Clock skew.

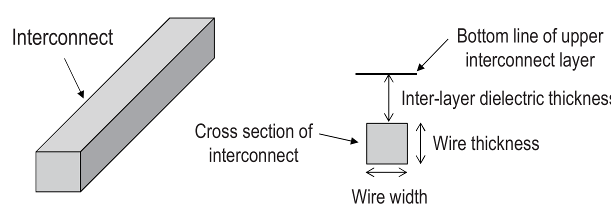

Fig. 2 Interconnect structure.

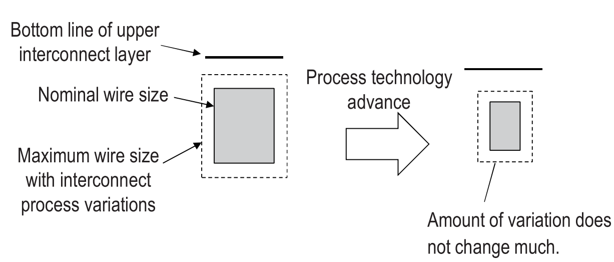

Fig. 3 Interconnect process variations.

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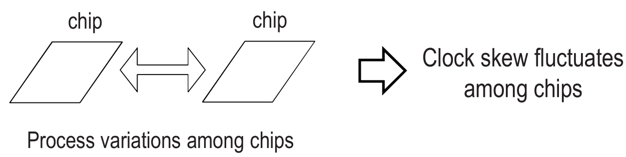

Fig. 4 Clock skew fluctuations.

tree clock network is usually used and therefore methods of reducing the clock skew fluctuations for tree clock structures are desired. References [3] and [4] proposed clock tree routing methods for minimizing clock skew within a chip considering interconnect process variations.

In this paper, we propose a method for minimizing the clock skew fluctuations (for clock tree) caused by interconnect process variations among chips (Fig. 4). The proposed method minimizes the influence of interconnect process variations on the signal delay, and considers the impact of interconnect process variations on both the gate delay and the interconnect delay.

This paper is organized as follows. In Sect. 2 the problem of minimizing clock skew fluctuations is defined and the proposed method is described. Section 3 shows the experimental results by using test circuits of 28 nm process technology to validate the effectiveness of the proposed method. Finally, conclusions and future works are presented in Sect. 4.

2. Proposed Method

2.1 Problem Definition

We define the signal delay as the delay time for a stage of a clock path on a clock tree. Here, the stage is the path from an input pin of a gate to the input pin of the next gate on the clock path, as shown in Fig. 5. The signal delay can be approximately calculated by Elmore delay model [5], which is a widely used delay model, as shown in (1).

$$D(L) = D_0 + R_{on}(c_w L + nC_{pin}) + \frac{r_w L}{n}\left(\frac{c_w L}{2n} + C_{pin}\right) \tag{1}$$

Here, D is the signal delay, D_0 is the signal delay without load, R_{on} is the on-resistance of the transistor, c_w is the wire capacitance per unit length, r_w is the wire resistance per unit length, L is the net wire length on the output of the transistor, n is the number of fan-outs on the output of the transistor, and C_{pin} is the input capacitance of the transistor.

The clock skew is the delay difference between two clock paths in a chip. Generally, the main reason of clock skew is the difference in wire length between two clock paths. Let L_1 and L_2 denote the wire lengths of the two clock paths (Fig. 6). Based on (1), the clock skew ΔD in a stage is calculated as follows:

$$\Delta D = \left(R_{on}c_w + \frac{r_w C_{pin}}{n}\right)(L_1 - L_2) + \frac{r_w c_w}{2n^2}(L_1^2 - L_2^2). \tag{2}$$

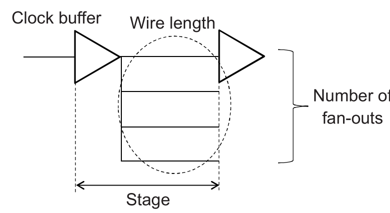

Fig. 5 A stage in a clock path.

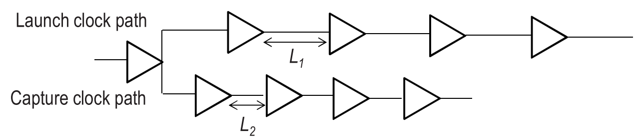

Fig. 6 Wire length in a clock path.

Table 1 Interconnect process corners.

Corner name	Description
Cmin	Interconnect process corner where the wire capacitance is minimum.
Cmax	Interconnect process corner where the wire capacitance is maximum.
RCmin	Interconnect process corner where the product of wire resistance and wire capacitance is minimum.
RCmax	Interconnect process corner where the product of wire resistance and wire capacitance is maximum.

Let us assume that the maximum and minimum wire lengths are l and zero, respectively. Then, the clock skew in the worst case (ΔD_{worst}) is calculated as follows:

$$\Delta D_{worst} = R_{on}c_w l + \frac{r_w C_{pin}}{n} l + \frac{r_w c_w}{2n^2} l^2. \tag{3}$$

The values of r_w and c_w fluctuate by the interconnect process variations among chips, and thus the clock skew ΔD_{worst} also fluctuate. In this paper, we focus on the clock skew fluctuations caused by interconnect process variations among chips, because interconnect process variations affect seriously on the signal delay in the advanced process technologies.

We define the clock skew fluctuation Δd between interconnect process corners c_1 and c_2 as the difference in ΔD_{worst} between interconnect process corners c_1 and c_2, as follows:

$$\Delta d(c_1, c_2) = |\Delta D_{worst}(c_1) - \Delta D_{worst}(c_2)|. \tag{4}$$

Here, we use the four interconnect process corners as shown in Table 1, which are generally used in the LSI designs [6], [7]. These four corners (Cmin, Cmax, RCmin, and RCmax) denote corner conditions in terms of the wire capacitance or the product of wire resistance and wire capacitance, and consider the variations of wire width, wire thickness, and inter-layer dielectric thickness.

Note that ΔD_{worst} corresponds to the portion in the signal delay D (with respect to wire length l) which is affected by the interconnect process variations. Therefore,

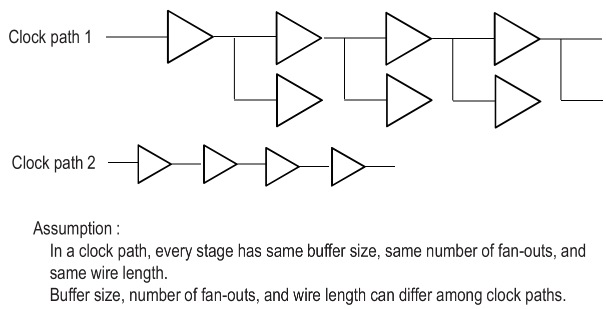

Fig. 7 Clock paths.

the clock skew fluctuation equals to the signal delay difference (among all the combinations of interconnect process corners) in a stage with wire length l. Thus, by calculating the difference in signal delays between two corners, Δd can be obtained.

For simplicity, we assume that, in a clock path, every stage has the same buffer size, the same number of fan-outs, and the same wire length. Note that different clock paths can have different buffer sizes, different numbers of fan-outs, and different wire lengths (Fig. 7). With this assumption, we define the problem of minimizing clock skew fluctuations as follows:

> Determine the wire length for each combination of clock buffer size and number of fan-outs, so as to minimize the maximum clock skew fluctuations among interconnect process corners (Cmin, Cmax, RCmin, and RCmax).

2.2 Clock Skew Fluctuations among Corners

Figure 8 shows the clock skew fluctuations (signal delay difference) between all the combinations of interconnect process corners for a buffer with four times the size of the normal buffer size (referred to as X4-size) in 28 nm process technology. (The clock skew fluctuations is normalized by the delay on the typical interconnect process condition.) Here, $\Delta d(corner1, corner2)$ denotes the clock skew fluctuation between *corner1* and *corner2*, and this is the absolute value of the signal delay difference between *corner1* and *corner2*. In this figure, it is observed that the clock skew fluctuation between Cmax and Cmin corners (referred to as Δd_C) is mostly maximum when the wire length is relatively short, and the clock skew fluctuation between RCmax and RCmin corners (referred to as Δd_{RC}) is mostly maximum when the wire length is relatively long. It is also observed that, at the wire length where Δd_C equals to Δd_{RC}, the maximum clock skew fluctuation among all the combinations of interconnect process corners becomes approximately minimum. This wire length is referred to as the *suitable wire length*. (Note that the suitable wire length is measured by net wire length and not by pin-to-pin wire length.) This suitable wire length differs depending on the clock buffer size and the number of fan-outs. By constructing the clock tree with the suitable wire length for each combination of clock buffer size and number of fan-outs, the clock skew fluctuations caused by interconnect process variations are thought to be approximately minimized.

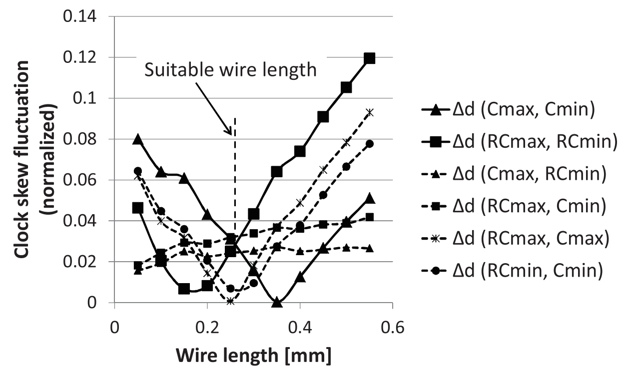

Fig. 8 Relation between wire length and clock skew fluctuation among interconnect process corners for a clock buffer.

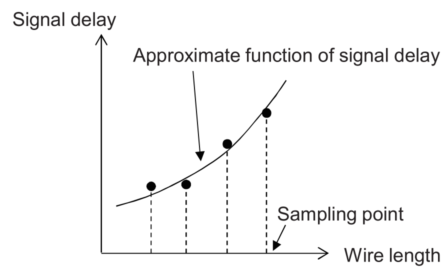

Fig. 9 Approximate function of signal delay.

2.3 Method for Minimizing Clock Skew Fluctuations

Based on the above observations, we propose a method for minimizing clock skew fluctuations as follows:

First, STA (static timing analysis) is performed for each interconnect process corner. Here, STA is performed for each combination of clock buffer size and number of fan-outs used in the clock tree of the target technology or the target designs. Also, the wire length sampling points are determined to obtain an approximate function of signal delay with respect to wire length (Fig. 9).

Next, the suitable wire length L_s for each combination of clock buffer size and number of fan-outs is obtained by using the approximate functions of signal delay (with respect to wire length) on the four corners (Cmin, Cmax, RCmin, and RCmax).

Then, the clock tree synthesis is performed such that the suitable wire length is used for each combination of clock buffer size and number of fan-outs. Note that how to implement the wire length for each clock buffer depends on EDA tool and design style, and it is out of the scope of this paper.

3. Experimental Results

In order to validate the effectiveness of the proposed method, we have performed STA on test circuits of 28 nm

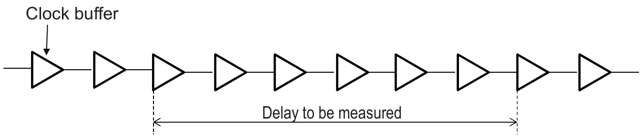

Fig. 10 Test circuit (clock path) used in the experiments.

process technology. Each test circuit is assumed to be a clock path, and composed of ten clock buffers with uniform size, uniform number of fan-outs, and uniform wire length, as shown in Fig. 10. The signal delay was measured as the delay time from the input pin of the third buffer to the input pin of the ninth buffer in the buffer chain, in order to stabilize the slew of each stage. The STA was performed for various sizes of clock buffer and various numbers of fan-outs.

The experimental conditions are as follows:

- Process technology: 28 nm.
- Clock buffer: X4, X8, X12, X16-size.
- Number of fan-outs: 1, 2, 4.
- Transistor process, power-supply voltage, and temperature are on the typical conditions.
- The fan-out configuration is symmetric, i.e., each pin-to-pin interconnect has a uniform length in a net.
- The clock paths go through specified interconnect layers for clock tree, which has a uniform nominal value for wire width, wire thickness, sheet resistance, and dielectric constant.

In the conventional clock tree synthesis, the clock tree is usually constructed based on the target transition time for suppressing the crosstalk noise. In the experiments, the wire length (for each combination of clock buffer size and number of fan-outs) was derived by using the conventional method based on the target transition time, which was specified as 50 ps. Also, the suitable wire length (for each combination of clock buffer size and number of fan-outs) was derived by using the proposed method. The wire lengths where the numbers of fan-outs is one, two, and four are shown in Figs. 11, 12, and 13, respectively. As shown in these figures, the suitable wire length L_s obtained by the proposed method decreases with an increase in buffer size, whereas the wire length obtained by the conventional method increases with an increase in buffer size. The average net wire lengths for all combinations of buffer size and number of fan-outs used in the experiments are 0.89 mm and 0.69 mm for the proposed method and the conventional method, respectively.

For each combination of clock buffer size and number of fan-outs, two test circuits (clock paths) were constructed, where one uses the wire length obtained by the proposed method and the other uses the wire length obtained by the conventional method.

For each combination of clock buffer size and number of fan-outs, the STA was performed on the test circuit and the maximum clock skew fluctuation among interconnect process corners (Cmin, Cmax, RCmin, and RCmax) was calculated for each of the proposed method and the conventional method, respectively.

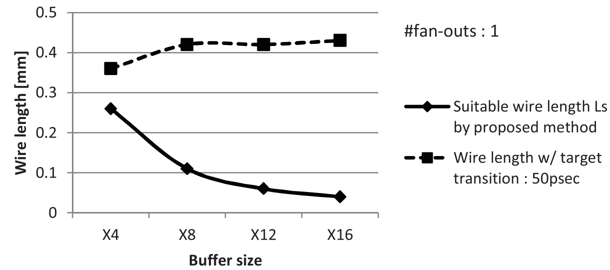

Fig. 11 Wire lengths derived by the proposed method and the conventional method. (#fan-outs: 1)

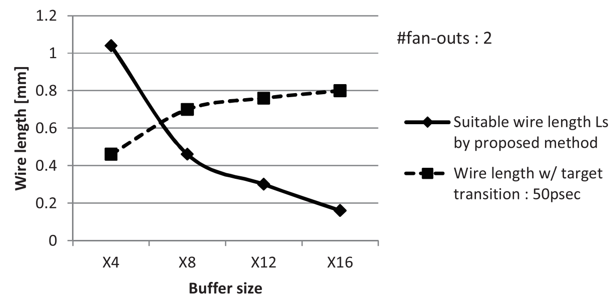

Fig. 12 Wire lengths derived by the proposed method and the conventional method. (#fan-outs: 2)

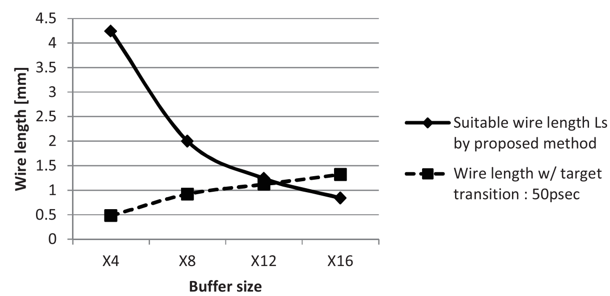

Fig. 13 Wire lengths derived by the proposed method and the conventional method. (#fan-outs: 4)

Figures 14, 15, and 16 show the maximum clock skew fluctuations (normalized by the delays on the typical condition) among interconnect process corners Cmin, Cmax, RCmin, and RCmax for each clock buffer size, for the numbers of fan-outs one, two, and four, respectively. The maximum clock skew fluctuations by the proposed method were at most 4.3% (in the case where the buffer size is X4 and the number of fan-outs is four) of the path delay on the typical condition. On the other hand, the maximum clock skew fluctuations by the conventional method were up to 21.7% (in the case where the buffer size is X16 and the number of fan-outs is one) of the path delay on the typical condition. In every combination of buffer size and number of fan-outs, the proposed method reduced the clock skew fluctuation compared to the conventional method, although the average net wire length by the proposed method was longer than that by the conventional method. For reference, the maximum clock skew fluctuations which are not normalized (i.e., the actual values) among interconnect process corners Cmin, Cmax,

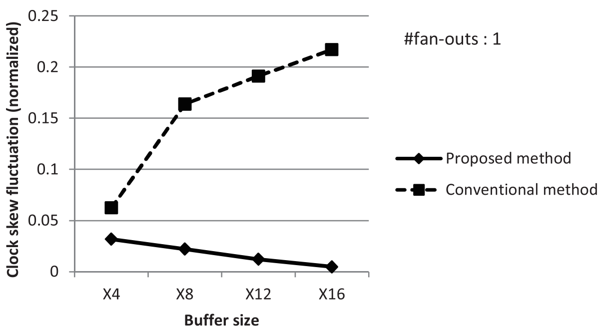

Fig. 14 Clock skew fluctuations caused by interconnect process variations. (#fan-outs: 1)

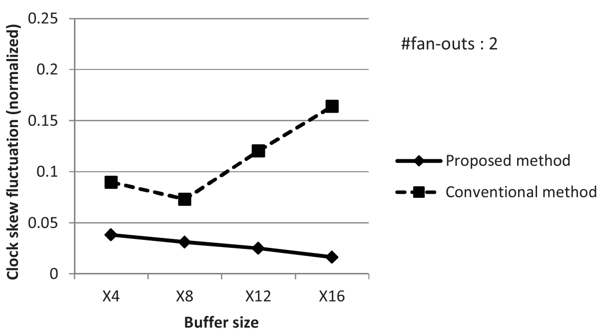

Fig. 15 Clock skew fluctuations caused by interconnect process variations. (#fan-outs: 2)

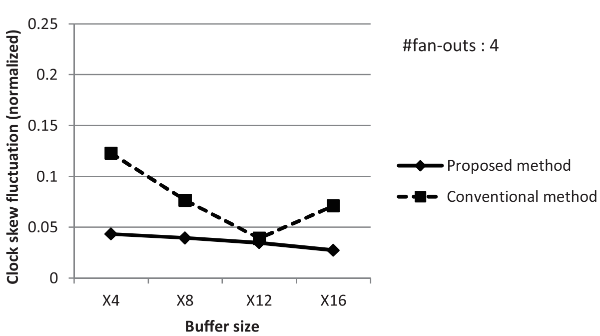

Fig. 16 Clock skew fluctuations caused by interconnect process variations. (#fan-outs: 4)

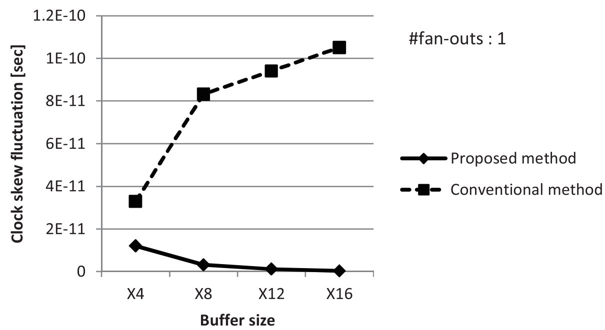

Fig. 17 Actual clock skew fluctuations caused by interconnect process variations. (#fan-outs: 1)

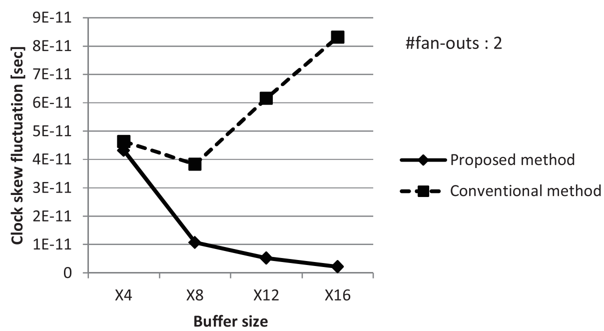

Fig. 18 Actual clock skew fluctuations caused by interconnect process variations. (#fan-outs: 2)

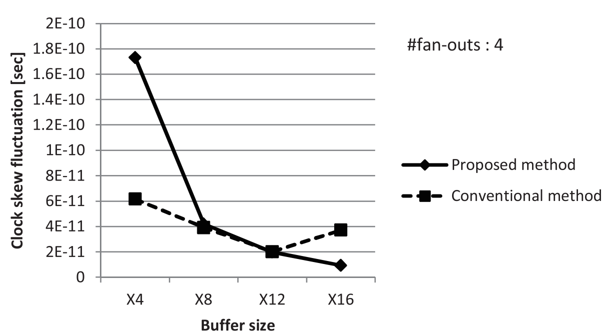

Fig. 19 Actual clock skew fluctuations caused by interconnect process variations. (#fan-outs: 4)

RCmin, and RCmax for each clock buffer size, for the numbers of fan-outs one, two, and four, are shown in Figs. 17, 18, and 19, respectively.

Note that, the wire lengths derived by the proposed method could be too long from the viewpoint of transition time. Therefore, we derived the best cases under constraint of the maximum transition time, which was specified as 50 ps, for each of the proposed method and the conventional method. Here, the best case means the combination of clock buffer size and wire length where the clock skew fluctuation is minimum for each number of fan-outs.

The clock buffer size and the wire length in the best case for each number of fan-outs, for each of the proposed method and the conventional method, are shown in Table 2. The clock skew fluctuations at the best cases are shown in

Table 2 Buffer sizes and wire lengths [mm] in the best cases.

#FOs	Proposed method		Conventional method	
	Buffer size	Wire length	Buffer size	Wire length
1	X16	0.02	X4	0.36
2	X16	0.16	X8	0.70
4	X16	0.84	X12	1.12

Table 3. In these tables, the first column shows the number of fan-outs (#FOs). In Table 3, each clock skew fluctuation is normalized by the signal delay on the typical condition. As shown in Table 3, the proposed method reduced the

Table 3 Clock skew fluctuations (Normalized) in the best cases.

#FOs	Proposed method	Conventional method	Reduction rate
1	0.0048	0.0624	92%
2	0.0164	0.0731	78%
4	0.0273	0.0390	30%

clock skew fluctuations by 30–92% compared to the conventional method, which shows the effectiveness of the proposed method.

4. Conclusions

We have proposed a method for minimizing clock skew fluctuations caused by interconnect process variations. The proposed method identifies the wire length at which the clock skew fluctuation among interconnect process corners is minimized for each combination of clock buffer size and number of fan-outs. The experimental results on test circuits of 28 nm process technology show that the proposed method reduces the clock skew fluctuations by 30–92% compared to the conventional method based on the target transition time.

Possible future works include integrating the proposed method into the existing clock tree synthesis system and validating the effectiveness of the proposed method by using real designs.

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