PAPER

Study of Reducing Circuit Scale Associated with Bit Depth Expansion Using Predictive Gradation Detection Algorithm

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SUMMARY The authors have evaluated a method of expanding the bit depth of image signals called SGRAD, which requires fewer calculations, while degrading the sharpness of images less. Where noise is superimposed on image signals, the conventional method for obtaining high bit depth sometimes incorrectly detects the contours of images, making it unable to sufficiently correct the gradation. Requiring many line memories is also an issue with the conventional method when applying the process to vertical gradation. As a solution to this particular issue, SGRAD improves the method of detecting contours with transiting gradation to effectively correct the gradation of image signals which noise is superimposed on. In addition, the use of a prediction algorithm for detecting gradation reduces the scale of the circuit with less correction of the vertical gradation.

key words: *bit depth expansion, circuit size, IIR filter, gradation pridiction algorithm*

1. Introduction

Recently, display devices have been gaining ever higher brightness and a wider color gamut. The brightness of liquid crystal displays was about 200 cd/m^2 around the year 2000. Now, however, it is not unusual to see liquid crystal displays with brightnesses of more than 500 cd/m^2. It is also commonplace that large screen liquid crystal televisions which wider than 30 inch diagonal, produce brightnesses that exceed 300 cd/m^2 [1]. In terms of color reproducibility, for example, a liquid crystal television using three primary color LEDs for its light sources produces 133% [2] of wide color gamut in comparison with BT.709 [3] while yet another television using solid lasers with short wavelength light sources reaches a color gamut as wide as 208% in comparison with BT.709 [4].

A display device aimed at higher dynamic range (HDR) has a problem of false contouring when it displays low bit depth image signals. More particularly, when displaying conventional digital image data of 8 bits/channel or lower on a HDR display device without any corrective processing, the change in the brightness and the change in the chromaticity for each digit of the image signal become relatively large. As a result, each digit change is inevitably recognized visually as false contouring when reproducing images of the sky and human skin in particular, which are composed of gradual gradation changes. In addition, applying the process for gaining high image quality, which currently contains complicated product-sum operations, or applying the coding process to low bit depth signals, generates round-off errors during the operation. This in turn causes discontinuities in the gradation. It is obvious that these discontinuities are very likely to be recognized visually as false contouring.

A few studies report that it is necessary to process image signals at an accuracy of 12 bits/channel or better to reproduce smooth images with less false contouring and noise effects on a HDR display device [5], [6]. In fact, the digital image signal transmission systems of HDMI [7] and DisplayPort [8], for instance, are capable of transmitting up to 16 bits for each RGB color. The next generation broadcast standard of BT.2020 [9] considers the quantization of up to 12 bits/channel. Considering, however, that the current high definition (HD) television broadcast standard of BT.709 deals with the quantization of 8 bits/channel, it is expected that many digital contents recorded at the quantization of 8 bits/channel or lower and image transmission system devices designed to the norm of around 8 bits/channel will remain for some time. This reality requires the development of a method that reduces artifacts such as gradation discontinuities to reproduce images of 12 bits/channel or better from low bit depth image signals so that a HDR display device can reproduce smooth images when it processes image signals that have been quantized at a low bit depth.

As for the input of analog image signals, increasing the quantized bit number through A/D conversion can obtain high bit depth signals conveniently. When inputting low bit depth digital signals, however, it is necessary to restore the image signals that have been lost during the quantization.

A number of studies have reported on methods of increasing the quantized bit number of digital image signals. The simplest of all is zero padding over the least significant bit of the input signals. This particular method affects the circuit scales less. Ulichney proposed a method called 'Bit Replication' that adds the high order bits of the input signals corresponding to the number of bits to be extended to the low order bits of the input signals [10]. Further, Dely proposed a method of applied dithering that utilizes the vi-

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sual characteristics of human beings [11]. These methods have less impact in terms of circuit scale. However, they are unable to efficiently correct artifacts such as gradation discontinuities attributable to the round-off errors during image processing operations.

A technique using smoothing filters is available that can expand the bit depth while efficiently correcting artifacts including gradation discontinuities. This particular technique, however, requires some attention so that the filtering does not degrade the sharpness of the image contours. To cope with this problem, Au's group proposed a method that combines a spatially varying filter, which takes into account the amount of gradation changes to vary its filter strength based on the flat region and the edge region, with a low path filter (LPF) [12], [13]. Kubo is doing research on expanding the bit depth by employing an edge preserving ε filter and a bilateral filter [14]. The use of an edge preserving filter does not have to divide images into the flat and edge regions. Since the smoothing filter has to become long depending on the amount of bit extension, however, it is disadvantageous from the viewpoint of circuit scale when expanding the bit depth. However, Okuno proposes a technique which controls the smoothing by identifying the texture region and the gradation region based on the frequencies of small gradation changes [15]. Nevertheless, this technique poses the risk of incorrect identification of these regions if noise is superimposed on the image signals.

These techniques of using smoothing filters have the common issue of making circuits large when it comes to devising hardware because of the product-sum operation between pieces of high bit data and of the necessary data delay depending on the filter length. Filtering images in the vertical direction, in particular, requires line memories to delay the data. Recently, thanks to the fine tuning of semiconductor processes, it is not uncommon to see application specific integrated circuits (ASIC) having a few mega gates and field programmable gate arrays (FPGA) having similar magnitude of logic. Nevertheless, it is preferable not to raise costs by using a large-scale circuit only for expanding the bit depth.

Under these circumstances, the authors of this study have been researching a method of improving the expression of gradation (referred to as super gradation or SGRAD) that requires fewer calculations and degrades the sharpness of images less than the conventional techniques while targeting the hardware development of SGRAD [16]–[18]. Like the algorithm proposed by Cheng [19], SGRAD basically uses the logic that determines the gradient of correction based on the width of the flat region of the images and the amount of gradation change in the transition part. The advantage is that SGRAD can easily be realized by hardware because the circuit comprises simple logics such as counters, addition and subtraction, and the bit expansion does not significantly affect the circuit scale. In addition, SGRAD's other function of detecting acnodes does not degrade the image sharpness because it does not exercise the smoothing process over the noise. Furthermore, use of the prediction algorithm for calculating the gradient of correction does not require a lot of line memory when expanding the bit depth of the images in the vertical direction.

2. Process of Expanding Bit Depth

2.1 Basic Configuration

Figure 1 is a basic block diagram of SGRAD. The diagram consists of a comparison section, a flat region counting section, an added value generating section and a delay compensation section, while $I(n)$ and $O(n)$ are input signals and output signals, respectively. Here, Z indicates a z transformation while Z^{-S} shows the total sum of delay in the sections for comparison, counting the flat region and generating added values. Also, Z^{-F} indicates the amount of delay in the flat region counting section. The comparison section calculates the amount of gradation change $d(n)$ between the n^{th} input pixel $I(n)$ and the adjacent pixel $I(n-1)$.

$$d(n) = I(n) - I(n-1) \tag{1}$$

Comparing the amount of gradation change $d(n)$ with the threshold value d_{lmt}, the flat region counting section determines it is a transition part if the amount of gradation change $d(n)$ is larger than the threshold value d_{lmt} or a flat region if otherwise. Thereafter, the counter counts the continuities in the flat region to calculate the pixel width of the flat region W.

$$W = \begin{cases} W+1 & \text{, when} \quad d(n) \le d_{lmt} \\ 0 & \text{, else} \end{cases} \tag{2}$$

If comparison with the gradation change $d(n)$ finds the pixel in question to be a transition part, the added value generating section generates an added value based on the pixel width of the flat region W having been counted in the flat region counting section and on the amount of gradation change $d(n)$ in the transition part and adds the added value to the input signal $I(n)$ to make the gradation change gradual.

$$O(n-a) = \frac{d(n)}{W}(W-a) + I(n-a) \tag{3}$$

where $\quad a \in \{1, 2, \ldots, W-1\}$

Figure 2 conceptually shows this system with an example that the pixel width of the detected flat region W is narrower than the delay width Z^{-F} of the image signal. While

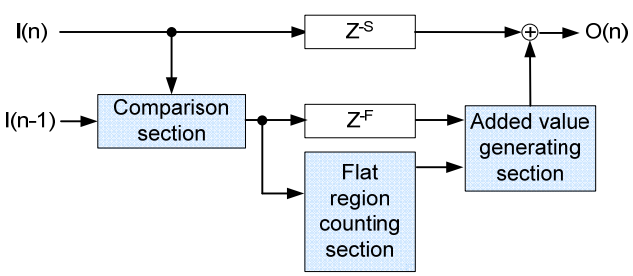


Fig. 1 Basic block diagram of SGRAD.

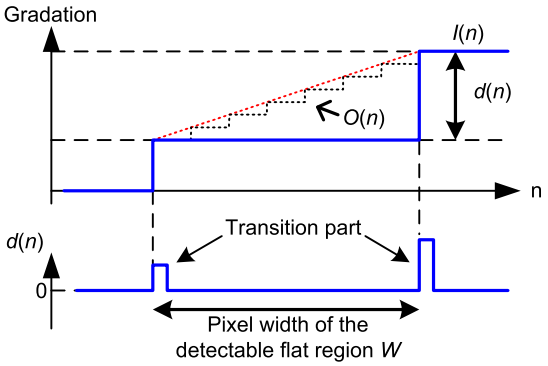


Fig. 2 Conceptual diagram representing two-gradation expansion process.

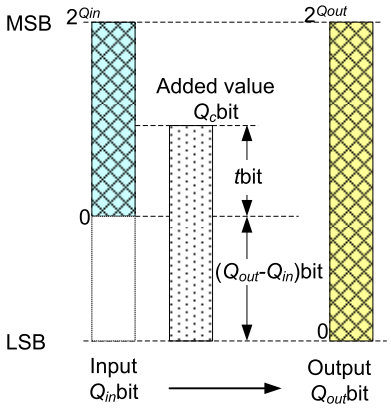


Fig. 3 Relationships among the bit depth of input signal, output signal and added value.

it is obvious that the wider the pixel width of the detectable flat region W becomes the more gradual gradation changes the system can deal with, the system needs more data delay. While the pixel width of the detectable flat region W depends on the quality of input signals, the pixel width of the detectable flat region W being about 256 pixels has a sufficient effect if the resolution of the HD image is about 1920×1080. Because of the use of an algorithm of fewer calculations consisting mainly of counters, even if the delay increases to some extent, SGRAD still can manage the expansion in the scale of the circuit compared with other techniques that use complicated product-sum operations.

2.2 Process Threshold Values

As shown in Eq. (3), SGRAD adds the added value, which is generated based on the amount of gradation change $d(n)$ in the detected transition part and the pixel width of the flat region W, to the flat region of the input signal $I(n)$. At this stage, the system adds the added value, which includes a decimal fraction generated by the division for generating the added value, to the signal level in the flat region. Thus, the system expands the bit depth of the input signals.

Figure 3 shows the relationships between the input and output signals where SGRAD expands the bit depth Q_{in} of

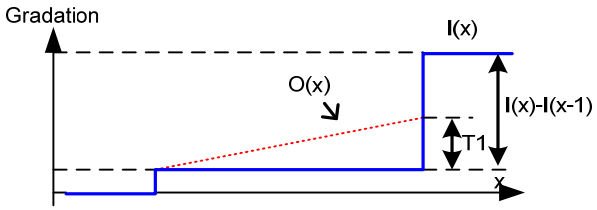


Fig. 4 Conceptual diagram of threshold value process.

the input signal $I(n)$ to obtain the output signal $O(n)$ with the bit depth of Q_{out}. Assuming the number of gradations to be t bits for carrying out smoothing correction over the input signals, the number of quantizations Q_c of the added value to be added to the input signal $I(n)$ is expressed by the following equation.

$$Q_c = (Q_{out} - Q_{in}) + t \tag{4}$$

It is considered that a gradation of about 2 bits is good enough to carry out the correction if the number of quantizations of the input signal $I(n)$ is about 8 bits. For a general circuit that expands the bit depth, however, the number t should be larger to some extent in consideration of retaining freedom. It should be noted that too large a gradation number t causes a steep gradation change, that is, it could smooth out the contours only to reduce the sharpness of the input images. To cope with this issue, if the amount of gradation change $d(n)$ is larger than the preset threshold value $T1$, the comparison section generates an output equal to $T1$ as the amount of gradation change $d(n)$. The proposed system also introduces a threshold processing where, if the amount of gradation change $d(n)$ is smaller than the threshold value $T1$, the comparison section generates an output equal to the amount of gradation change $d(n)$ as it is as a difference.

$$d(n) = \begin{cases} I(n)-I(n-1) & \text{, when } \quad I(n)-I(n-1) \le T1 \\ T1 & \text{, else} \end{cases} \tag{5}$$

Figure 4 is a conceptual diagram showing the gradation correction at the contours by the algorithm with the threshold processing. If the amount of gradation change $I(n)-I(n-1)$ at the transition part is larger than the threshold $T1$, the added value generating section generates an added value based on the pixel width W and the threshold value $T1$ and adds the generated value to the input signals.

Expanding the bit depth of only the low gradation part of the signals in a selective fashion, the threshold processing algorithm can make the number of quantizations of the added value small. Although this results in the merit of making the circuit scale smaller, it also increases the nonlinear characteristics of quantization. Nonetheless, as the γ characteristics of a liquid crystal display [20] and Weber's Law expressed by Eq. (6) show, it is well known that the darker the signals are, the larger the recognizable gradation difference ΔV_I of the human perception V_I is. This means that, even limited to the low gradation areas, the proposed system has a sufficient effect of improving artifacts including gradation discontinuities.

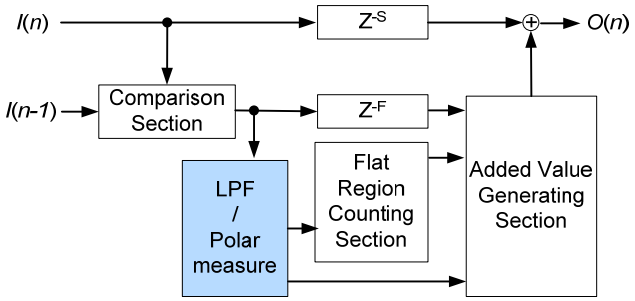


Fig. 5 Block diagram for removing acnodes.

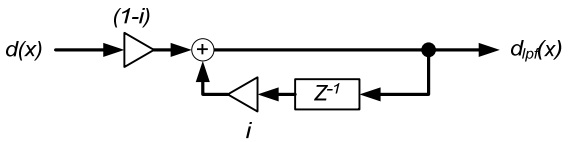


Fig. 6 Configuration of IIR filter.

$$\frac{\Delta V_I}{V_I} = \text{const.} \tag{6}$$

2.3 Eliminating Acnodes in Detecting Flat Regions

SGRAD generates an added value based on the pixel width of the flat region W and the amount of gradation change $d(n)$ in the transition part. Therefore, if noise is superimposed on the input signals $I(n)$, as is sometimes seen in analog signals, the system would not detect the pixel width of the flat region W. This could possibly make the system unable to generate the added value correctly. The system carries out the gradation processing for the noise in a similar manner where the system desires to correct the transition part contained in the input images, possibly degrading the sharpness of the entire images.

Most image processing systems are equipped with various noise reduction process functions. Even if noise is superimposed on the source signals, it will not create a big problem as long as SGRAD is applied after these noise reduction processes. If SGRAD is laid out in the front row of the image processing flow before the noise reduction processing, it is desired that, as shown in Fig. 5, an LPF carries out smoothing in a simplified manner on the difference $d(n)$ coming out from the comparison section to reduce incorrect detection in the process of detecting the transition part.

The authors in this study used a primary infinite impulse response (IIR) filter as an LPF to reduce the number of taps in the filtering process while anticipating its use in the vertical direction. Figure 6 shows the configuration of the IIR filter. Here, Z^{-1} indicates a one pixel delay. Equation (7) shows the filter function where $d_{lpf}(x)$ is the amount of difference after the LPF.

$$d_{lpf}(x) = i \cdot d_{lpf}(x-1) + (1-i) \cdot d(x) \tag{7}$$

$$= (1-i)\left[d(x) + \sum_{n=1}^{\infty} i^n d(x-n)\right] \tag{8}$$

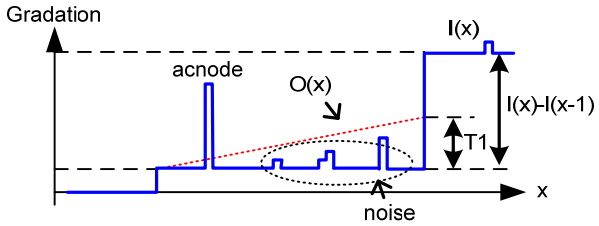


Fig. 7 Conceptual diagram of removing acnodes.

where $0 \le i < 1$

While noise causes the incorrect detection of the pixel width of the flat region W, it is also a necessary artifact to maintain the image sharpness. More particularly, the impulse noise of a relatively large gradation change, which the LPF is unable to remove, can degrade the image sharpness if it is present at the contours, but it has the effect of increasing the image sharpness if it is present at the texture part [21]. Considering this, rather than applying the smoothing process indifferently to the entire noise, a sequence for eliminating acnodes is used in conjunction with a simple LPF to prevent the image degradation when expanding the bit depth.

Figure 7 shows the concept of eliminating acnodes. As for transition parts with a large change (which is the noise components that the LPF cannot smooth out), the system does not carry out contour correction if it judges they are acnodes. Here, using the polarity of the difference $d(x)$ calculated by the comparison section, if the following equation is satisfied, the $I(x)$ is defined as an acnode.

$$d(x) \cdot d(x+1) < 0 \tag{9}$$

If the detected transition part is judged to be an acnode, the flat region counting section continues to count the pixel width of the flat region. In other words, the added value generating section does not apply the gradation correction process to the acnode.

2.4 Results of Image Simulation

Now the authors are conducting image simulations on the improvements in the quality of images that contain false contours and on the presence or absence of defects in high definition images to evaluate the effects of the bit depth expansion by the SGRAD process.

Figure 8 shows the original picture used for the image simulation to see the improvements against the false contours. It is a grayscale image of 760×480 pixels and 6 bits with random noise of up to five gradations superimposed.

Figure 9 (a) shows an enlarged view of the section enclosed by the rectangle in the uppermost row in Fig. 8. It shows a step of one digit for every 32 pixels in the horizontal direction. One digit on a 6-bit image, which corresponds to the gradation number of four on an 8-bit image of a conventional printer, appears to be a false contour to the authors.

Figure 9 (b) shows the result of expanding the number of bits to 8 bits with the image in Fig. 9 (a) having gone

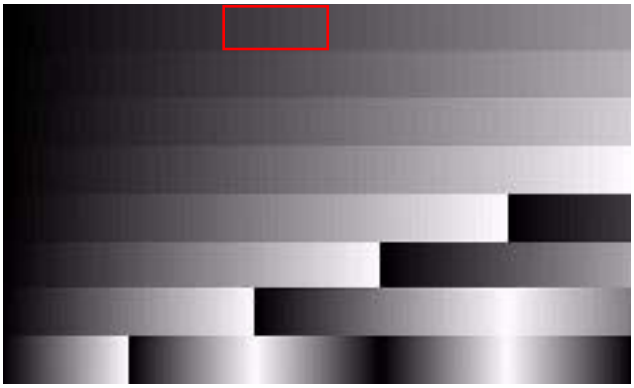


Fig. 8 Original 6bit Picture with randam noise.

(a) Enlarged input image

(b) Enlarged image after SGRAD process

Fig. 9 Results of image simulation 1.

through the SGRAD process. Here, the SGRAD process takes place in the horizontal direction only while the maximum detection width is 256 pixels and the process threshold value $T1$ is 2 bits. The results show that the false contours are gone from the image where noise is superimposed on the input signals, proving the improvement in the image expression.

One of the most concerned side effects of the bit number expansion is that this particular process smoothens out an image to an extent not desired only to deteriorate the feeling of fineness. The authors expanded the number of bits on a high definition image to see how the bit number expansion would deteriorate the image quality. Figure 10 shows an example where the above processes apply to an image extracted from the CMYK standard colour image data (ISO/DIS 12640). In a similar manner of treating the input image as shown in Fig. 9, the number of bits of the original image that has been degraded to 6 bits is expanded to 8 bits. The authors observed that the bit number expansion by the SGRAD process did not smoothen out the contours so that the image maintained its sharpness.

(a) Input image (6bits/channel)

(b) Image obtained after gradation extension processing (8bits/channel)

Fig. 10 Results of image simulation 2.
ISO/DIS 12640, JIS X9210-1995 N5 (resolution: ISO 400)

3. Developing Hardware for SGRAD and Reducing Circuit Scale

3.1 Necessity for Reducing Circuit Scale

The algorithm discussed in the previous section uses the pixel width of the flat region W in the process of generating added values. The algorithm therefore requires a large counter that detects the pixel width W to cope with the gradation transition of the image, the gradation of which changes gradually in steps. In addition, it also needs a delay register corresponding to the maximum number of detectable pixels. More particularly, it is assumed here that, as an example, the circuit to be installed is capable of correcting images having a gradation gradient of one gradation for every $W = 256$ pixels. As for the circuit discussed in the above sections, since this circuit requires at least 256 clocks from the data entry to the image processing, it is necessary to delay the input signals by good for 256 pixels.

For the purpose of this research, the authors designed a circuit for an FPGA where SGRAD increased the bit depth of 10 bits/channel HD image signals to 16 bits/channel. Because of FPGA's strict limit to the clock frequency, the HD signal of the 150 MHz dot clock cannot be used as it is. Therefore, the circuit is configured to process the input and output signals of 6 channels in parallel operation.

Table 1 Results of FPGA synthesis of bit-depth expansion circuit from 8 bits to 16 bits (the process takes place only in the horizontal direction).

Device	Xilinx 5vlx330ff1760-2
Input signal	60bit (10bit × 6channel)
Output signal	96bit (16bit × 6channel)
Max. horizontal length W	256 pixel
Number of Slice LUTs	7206
Number of DFF	8569

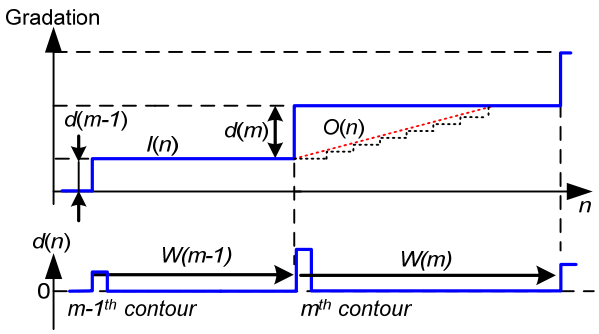


Fig. 11 Conceptual diagram of prediction gradation detection.

After programming the circuit using VHDL [22], which is a hardware description language, the authors used the synthesis tools provided by an FPGA vendor to configure the circuit. Table 1 shows the results. The delay flip-flop (DFF) count of this circuit was 8569. The authors estimate based on past experience that this DFF count is equivalent to an ASIC gate count of about 90 kGates.

Like this circuit, if the process takes place only in the horizontal direction, one line memory (the number of input image channels × bit depth data width) will reduce the flip flops necessary for data delay. Applying the SGRAD process also in the vertical direction requires a 256 line memory for data delay, for instance, making it impractical from the cost viewpoint. The authors therefore studied a prediction process that will make the hardware circuit small.

3.2 Predictive Gradation Detection Algorithm

Figure 11 is a conceptual diagram of the prediction gradation detection algorithm. This algorithm is different in the relationship between the pixel width of the flat region W used for calculation and the gradation change $d(n)$ from the conventional system shown in Fig. 2. The prediction gradation detection algorithm calculates the amount of correction using the width of the flat region W' that is positioned between the $m-1^{th}$ contour and the m^{th} contour but not using the pixel width of the flat region W that starts from the m^{th} contour. It is not necessary to retain the input signal $I(n)$ good for W' pixels at the m^{th} contour. The counter has to retain only the pixel width W' of the detectable flat region. As a result, this enables the circuit scale to be reduced.

$$O(n+b) = I(n+b) - \frac{d(m)}{W(m-1)}(W'-b) \qquad (10)$$

where $\quad b \in \{1, 2, \ldots, W(m-1)\} \leq W(m)$

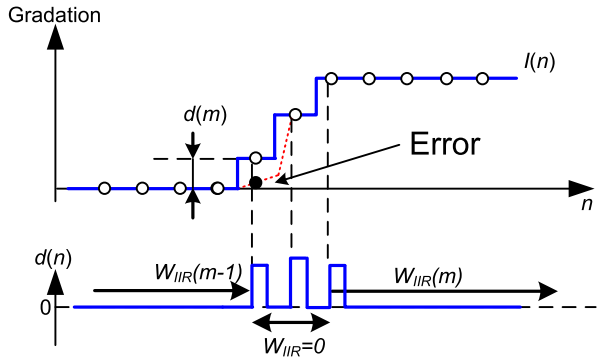


Fig. 12 Correction error over continuously changing contours.

It is prerequisite that the gradation change is uniform for the prediction gradation detection algorithm to function correctly. In an image such as a natural picture where the gradation change is not uniform, the width of the region $W(m)$ desired to be corrected is significantly different from the width of the adjacent flat region $W(m-1)$ used for calculating the amount of correction, possibly making the result of correction unnatural. Thus, the authors used an IIR filter to calculate the amount of correction in a similar manner to the LPF shown in Eq. (7).

$$W_{IIR}(m) = j \cdot W_{IIR}(m-1) + (1-j) \cdot W(m) \qquad (11)$$

$$= (1-j)\left[W(m) + \sum_k j^k W(m-k)\right] \qquad (12)$$

3.3 Added Value Calculating Section

The added value calculating section calculates an added value for correction as expressed by Eq. (10) based on the transition width $d(n)$ shown in Eq. (5) and the flat region width W_{IIR} shown in Eq. (12).

The prediction process, however, encounters a problem in the part where continuous gradation change occurs in Fig. 12. More particularly, a process for smoothing the gradation change takes place at the pixel position where the gradation change starts. From the next pixel onwards, while the process detects the transition width $d(n)$, it judges the width of the flat region W_{IIR} to be zero. This in turn makes the added value generating section unable to generate the added value correctly, causing no gradation correction to occur. As a result, incorrect conversion takes place in that the amount of gradation change between the pixel where the gradation change starts and the second pixel becomes large. In some cases, the portion of this enlarged gradation change is recognized as a false contour.

The added value generating section of the SGRAD therefore does not generate the added value for the region where gradation changes continuously so that correction does not take place.

3.4 Results of Image Simulation

An image such as a human face with a gradual gradation

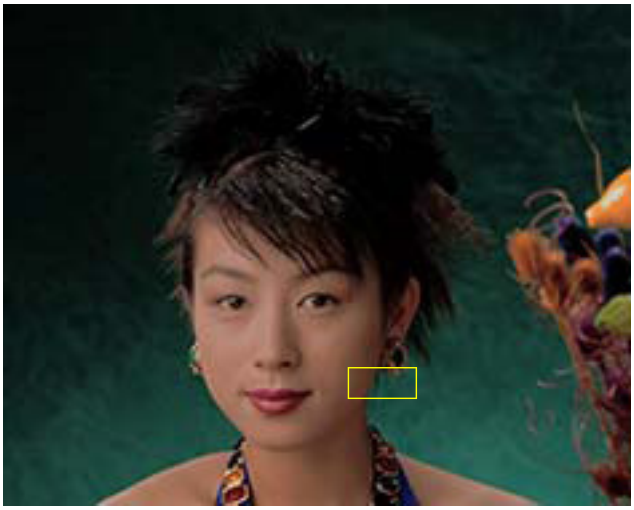


Fig. 13 Original image.
JIS XYZ/SCID (ISO 12640-2):N1 Woman with glass (JIS-sRGB)

change is an image where a false contour is likely to be recognized. The authors selected the standard image human portrait shown in Fig. 13 for image simulation. Figure 14 shows the results of image simulation using SGRAD. These are enlargements of the area enclosed by the rectangle in Fig. 13. Figure 14 (a) shows the input image where the image has been converted to 6 bits/channel to facilitate the effect observation. The fewer number of gradations causes a false contour to be observed in the gradation area. Figure 14 (b) shows where bit depth expansion has taken place in the horizontal direction only while converting the image of 6 bits/channel to an image of 8 bits/channel. Figure 14 (c) shows where bit depth expansion has taken place in both the horizontal and vertical directions while converting to an image of 8 bits/channel. The results show that while the bit depth expansion process in the horizontal direction only is insufficient in correcting the artifacts, the bit depth expansion process in both directions effectively corrects the artifacts. Here, no incorrect conversions, which has been a concern with the prediction algorithm, occur.

3.5 Moving Image Evaluation Equipment and Circuit Scale

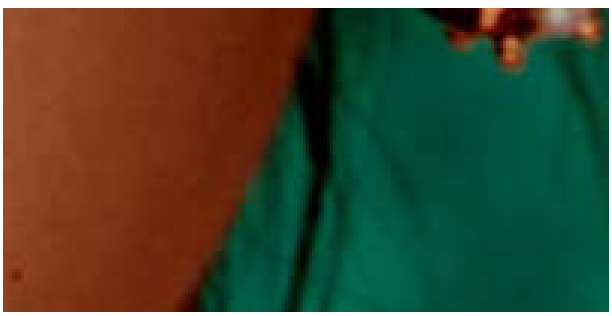
In order to actually verify the SGRAD circuit scale and evaluate the performance of the SGRAD for processing moving images, the authors wrote a program in VHDL, using synthesis tools and configured an FPGA circuit.

Figure 15 is a schematic of the equipment used for the evaluation. The FPGA evaluation circuit board has a 10-bit dual channel digital interface and a DRAM. In addition to SGRAD, the authors also programmed into the FPGA a dither circuit to convert data to a bit depth that is commensurate with the display device.

When the moving image signals enter the evaluation board, the evaluation equipment first uses SGRAD to expand the bit depth of the moving image signals and correct

(a) Input image (6 bits/channel)

(b) Simulated image after SGRAD process only horizontal direction (8 bits/channel)



(c) Simulated image after SGRAD process in both the horizontal and vertical directions (8 bits/channel)

Fig. 14 Results of image simulation 3.

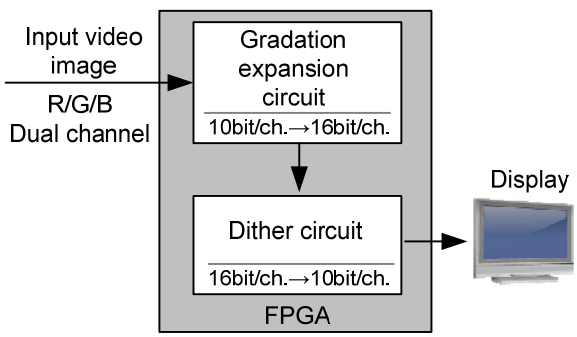


Fig. 15 Evaluation equipment.

the artifacts in those input signals. Considering that present day consumer display devices such as television sets usually have an image processing precision of about 14 bits/channel, the authors determined to process the moving images even higher to 16 bits/channel. This is higher than the bit depth of

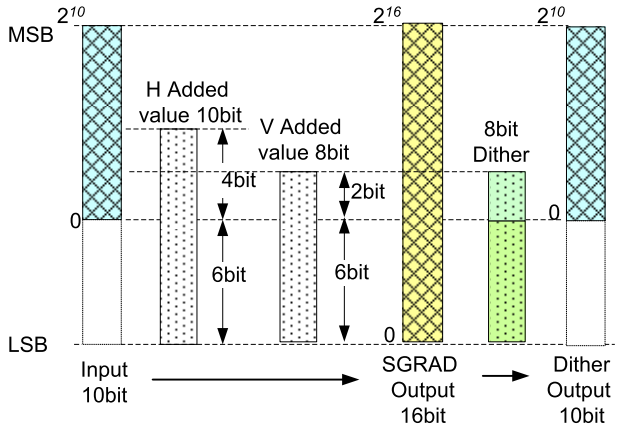


Fig. 16 Relationships between the bit depth of input signal, output signal, added value and range of dither.

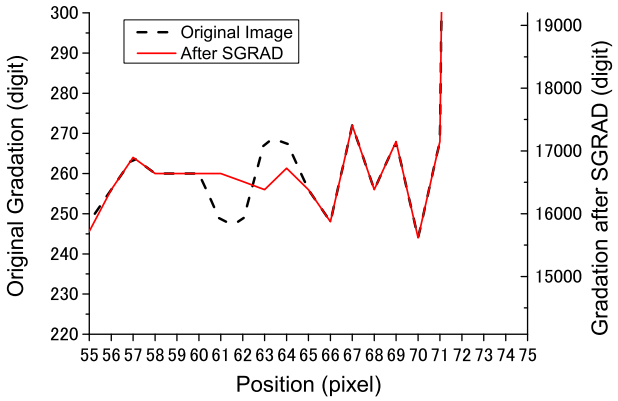


Fig. 17 Result of bit depth expansion using SGRAD.

Table 2 Results of FPGA synthesis of bit depth expansion circuit from 10 bits to 16 bits.

Device	Xilinx 5vlx330ff1760-2
Input signal	60bit (10bit × 6channel)
Output signal	96bit (16bit × 6channel)
Max. horizontal length W_H	1024 pixel
Max. vertical length W_V	256 line
Number of Slice LUTs	12177
Number of DFF	14640
Embedded SRAM	558KB

12 bits/channel required for the HDR display devices. Since general display devices have a gradation number of about 10 bits, they cannot simply display the 16 bits/channel image signals. However, it is significantly beneficial to expand the image signals to a higher bit depth at the stage before the complicated image processing logics where the operation is expected to create many round-off errors.

The dither circuit then compresses the bit depth of the image signals, which have been brought up to 16 bits/channel by SGRAD, down to 10 bits/channel so that the display can generate the images on the screen.

Figure 16 shows the detailed process flow and transition in the bit depths during the process. In addition to the processing in the horizontal direction, the process in the vertical direction also takes place. Upon receiving the 10 bits/channel image signals, SGRAD carries out the process in the horizontal direction with the maximum detectable flat region width of 1,024 pixels while using the added value of 10 bits ($t=4$). This results in the image signal bit depth of 16 bits. Next, SGRAD processes the image signals in the vertical direction with the maximum detectable flat region width of 256 lines while using the added value of 8 bits ($t = 2$). (Note that this process mainly removes the artifacts in the vertical direction. It does not expand the bit depth.) Receiving the output image signals of 16 bits/channel coming from SGRAD, the dither circuit carries out the 8-bits dither process to finally generate image signals of 10 bits/channel.

Figure 17 shows the changes in the gradation of an original 10-bit input image and the changes in the gradation after expanding the original input image to 16 bits using the SGRAD process. The SGRAD process smoothens out the abrupt gradation changes that are present in the original input image between the 60th pixel and the 65th pixel. The diagram also confirms that the SGRAD process expands the original image to 16 bits without smoothening out the continuously changing contours between the 66th pixel and the 70th pixel and the transition section at the 70th pixel onwards.

Table 2 shows the results of FPGA synthesis of this circuit. Despite the vertical process taking place in addition to the horizontal process, the results verify that use of the prediction gradation detection algorithm can contain the system within the circuit scale of 180 kGates and the use of 558 KB of SRAM even with a configuration that expands the 10-bit depths of the image signals by 6 bits for each of the six channels.

3.6 Results of Evaluating Moving Images

The authors used some of the standard moving images and similar data to verify that the SGRAD process was free from side effects such as degradation of image sharpness. The verification also included the intentional use of images containing noise to confirm the effects of SGRAD on reducing the artifacts included in the images.

Figure 18 shows images before and after implementing the SGRAD process for MPEG image signals which most outstandingly demonstrate the effects of SGRAD on reducing artifacts. Since being unable to use images of 10-bit depth because they are printed on paper, the authors converted the 10 bits/channel image captured from the image signals to a 6 bits/channel image as shown in Fig. 18 (a). Figure 18 (b) shows the result of expanding the bit depth of the image in Fig. 18 (a) to an image of 8 bits/channel.

The results of simulation here as well as the verification using the evaluation equipment shown in Fig. 15 verified that SGRAD satisfactorily improved the quality of images containing MPEG noise that a simple filter was unable to remove.

(a) Original image captured for simulation from input signals with bit-depth extended to 6 bits/channel

(b) Simulated image after SGRAD process (8bit/channel)

Fig. 18 Results of simulation on image with superimposed MPEG noise.

4. Conclusions

With the display devices increasingly acquiring HDR, false contouring has become a probrem when displaying low bit depth image signals on HDR display devices. To provide a solution to the probrem of false contouring, the authors have developed SGRAD, which is a bit depth expansion algorithm that is suitable for using hardware with a small circuit scale. With SGRAD installed on an FPGA, the authors verified the circuit scale and evaluated its performance.

Unlike the conventional methods of expanding bit depth that use smoothing filters, SGRAD employs counters effectively to reduce the circuit scale without using product-sum operations extensively. As a result, despite the use of an algorithm to remove acnodes so that SGRAD can effectively carry out the gradation correction against image signals on which noise was superimposed, the authors confirmed that SGRAD can be implemented in a circuit scale of approximately 90 kGates for operations in the horizontal direction only. Also, when equipped with a predictive gradation detection algorithm using IIR filters, when implementing the process in the vertical direction as well, SGRAD demonstrated the effective removal of the artifacts included in the input signals without requiring a lot of line memory.

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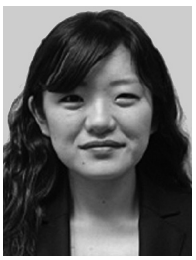

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