

LETTER

RONoC: A Reconfigurable Architecture for Application-Specific Optical Network-on-Chip

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SUMMARY Optical Network-on-Chip (ONoC) is a promising emerging technology, which can solve the bottlenecks faced by electrical on-chip interconnection. However, the existing proposals of ONoC are mostly built on fixed topologies, which are not flexible enough to support various applications. To make full use of the limited resource and provide a more efficient approach for resource allocation, RONO (Reconfigurable Optical Network-on-Chip) is proposed in this letter. The topology can be reconfigured to meet the requirement of different applications. An 8×8 nonblocking router is also designed, together with the communication mechanism. The simulation results show that the saturation load of RONO is 2 times better than mesh, and the energy consumption is 25% lower than mesh.

key words: reconfiguration, optical Network-on-Chip, application-specific, optical router

1. Introduction

Network-on-Chip is a promising way to integrate multi-core system on a single chip [1], [2]. Compared with the conventional electronic interconnect, optical interconnect is capable of providing more bandwidth at a lower power budget. Therefore, photonic technology is becoming an increasingly attractive solution to the various challenges faced by on chip communication. Meanwhile, recent developments in silicon photonics have made it feasible to fabricate all the necessary optical building blocks on a single chip [3], achieving high-bandwidth and energy-efficient intra-chip communications. Various architectures have been proposed, most of which are established on fixed topology [4]–[7]. However, the NoC architecture may face various applications which own different traffic characteristics. Thus, the ONoC proposed in literature often lacks flexibility to meet the different requirements of the applications.

On the other hand, since the technology of optical buffers is not so mature in today's photonic technology, optical packet switching is difficult to implement for on chip networks. Hence, a circuit-switching-like transmission mechanism is often employed for ONoC. However, limited path diversity is one of the main disadvantages, especially for the mesh based ONoC. The high contention probability leads to high latency and degraded throughput. One solution is to employ the concept of reconfiguration to meet different requirement of various applications [8], [9]. It can also help

to increase the success rate of the path establishment. In the electrical domain, some methods to complete reconfiguration have been available. Stensgaard et al. [10] presented a NoC architecture called ReNoC that allows the network topology to be statically reconfigured by using an intelligent switch. Binzhang Fu and Yinhe Han et al. proposed a configurable wormhole routing algorithm [11]. In the optical domain, related researches are relatively few. Artundo et al. propose a reconfigurable optical interconnect and its topology in optical layer is adapted automatically to the evolving traffic situation, allowing a large fraction of the short coherence messages to use the optical links [12]. Gao et al. present the RePNoC architecture which is optional to preset the topology by configuring the connections according to different application patterns [13]. The connections between source and destination IP cores with long links can be set up by bypassing the intermediate routers.

In this letter, a reconfigurable architecture for application-specific optical Network-on-Chip is proposed, the interconnection of which can be reconfigured for different applications, achieving lower latency and power consumption. RONO topology has a simple architecture and is easy to configure the connections just by altering the states of different groups of microring resonators (MRs). A configuration algorithm for different traffic patterns is also developed, which applies universally to diverse applications. The simulation results prove that RONO provides a low-latency and energy-efficient performance.

2. The Architecture of Reconfigurable Optical Network-on-Chip

2.1 Network Architecture

The mesh topology has the advantages of regular shape and simple structure, so it has wide application in the area of NoC. However, it cannot well satisfy specific applications, especially when the traffics among different communication pairs fluctuate dramatically. Therefore, it is necessary to reconfigure the topology to meet the requirement of different applications. Consequently, RONO, a variant of traditional mesh topology, is employed for the ONoC architecture, which inherits the advantages of mesh and achieves better flexibility. Figure 1 illustrates the architecture of RONO. There are two types of nodes in the RONO, i.e. routers and IP cores. The nodes (IP core or router) are placed in rows and columns like mesh topology. Each router has eight

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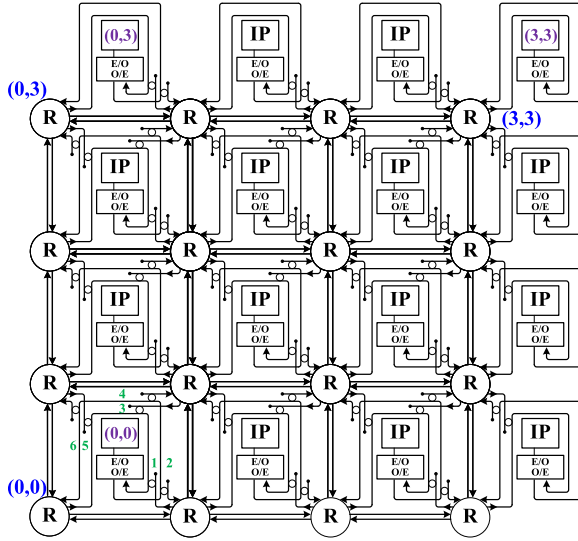


Fig. 1 Architecture of 4×4 RONO.

ports, four of which are used to link up with the four neighboring routers. The other four ports are used to connect the four IP cores around the router. If more IP cores are connected to the router, the number of ports will increase, which leads to higher hardware cost and more power consumption. Each IP core is connected to the router by waveguides and three pairs of MRs. For each pair of MRs, one is used for receiving, and the other is for transmitting. The optical/electronic (O/E) and electronic/optical (E/O) interfaces between the router and IP core take charge of converting optical signal into electronic signal and vice versa.

Compared with some popular topologies used in ONoC, like mesh, the proposed RONO owns some advantages. The diameter and average distance of the RONO are much smaller than that of mesh, which helps to decrease the latency and energy consumption. More link options provide a more flexible choice when configuring the topology.

2.2 Implementation of the Reconfiguration

The RONO needs to be configured to decide which router the IP core will connect to. When the application changes, the RONO should be reconfigured to meet the new requirements. The configuration and reconfiguration of RONO is completed by controlling the three pairs of MRs around the IP core. In default situation, these six MRs are all in the off state. Hence, each IP core is connected to the south-west router. In this situation, the topology of RONO is the same with the mesh topology. If the IP core needs to be connected to other routers, the reconfiguration is carried out by powering on the related MRs. For example, if the IP cores (0, 0) need to be connected to the router (1, 1), the resonators 3 and 4 should be powered on. The rest resonators 1, 2, 5 and 6 are still in the off state. Hence, the optical signal issued by the IP core (0, 0) will be coupled by the resonator 3 to the router (1, 1). The signal from the southwest part of the router (1, 1) will be coupled by the resonator 4 to the IP core

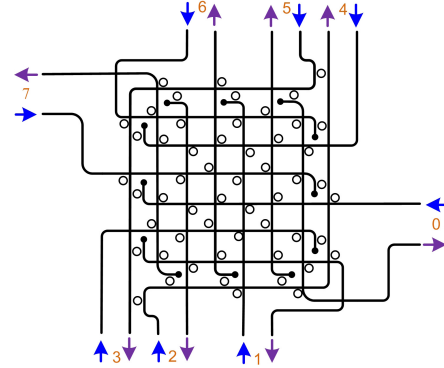


Fig. 2 Layout of 8×8 nonblocking switching fabric.

(0, 0).

After each IP core executes such configuration operation, the reconfiguration of the topology is completed. Certainly, the reconfiguration depends on the specific application, therefore we propose a high-efficiency configuration algorithm for different applications which will be introduced in details in Sect. 3.

2.3 Router Architecture

Optical router is one of the key components of RONO, which implements the function of routing packets. To route packets from and to the eight distinct ports without blocking, an 8×8 optical router architecture is designed. It consists of a switching fabric and a control unit. The switching fabric is the core of the optical router, as is shown in Fig. 2. It switches optical signals from one input port to another output port without blocking. In our design, the switching fabric is assembled by 54 MRs and 14 waveguides. The control unit is built from traditional CMOS transistors. It uses electrical signals to configure the switching fabric by powering on and off each MR according to the routing information. The control units of all the routers in RONO use the electronic network to set up the optical paths.

2.4 Communication Mechanism

To reduce the blocking probability in the circuit-switched network, a hybrid communication mechanism is designed to improve the performance. For the IP cores connected to the same optical router, they can communicate directly if both the input and output are free, thus lowering the latency penalty efficiently. When the output port is granted, the related resonator inside the router will be powered on. Hence, the optical signal from the source IP core pass through the router and arrives at the destination IP core directly. Otherwise, for the source and destination cores not connected to the same router, a physical path should be reserved from the source to the destination before the optical data is transmitted. The path, consisting of several intermediate routers and the waveguides connecting them, is manipulated by three electrical control signals: SETUP, ACK and RELEASE.

The SETUP signal is issued before the transmission of optical data. It progresses toward the destination by using the XY routing algorithm and reserves intermediate links. If the SETUP signal is blocked, it will wait until the required resource is released by the corresponding RELEASE signal. When the SETUP signal reaches its destination, an ACK signal is sent back to the source and powers on the related resonators in the corresponding optical routers along the reserved path. Once receiving the ACK signal, the source sends the optical data. Then the transmission of data begins, after which the source sends a RELEASE signal to tear down the reserved path.

3. Configuration Algorithm for the Reconfigurable Optical Network-on-Chip

To make full use of RONO, a configuration algorithm is proposed aiming at optimized performances for specific applications.

The first step in the proposed algorithm is to determine the number of routers of NoC. The number of the routers for RONO should be large enough to interconnect the IP cores for a certain application. However, the fewer number of routers, the less overhead occurs. Taking the chip shape into account, the gap between the number of routers in x dimension and y dimension should be reduced as small as possible.

The next step is to configure the RONO for the application, i.e. mapping IP cores to the network and connecting IP cores to the appropriate routers. Power consumption is a big concern for NoC design. To save energy, IP cores with large communication traffic should be placed as near as possible. Before mapping, we divide the IP cores into clusters. The size of each cluster is no more than 4, because each router in RONO can connect at most 4 IP cores. Then the clusters are placed onto the network to achieve lowest energy consumption. The algorithm is listed in Fig. 3.

4. Simulation and Results

We build a network simulator for RONO based on OPNET and compare it against optical NoC based on mesh network in terms of latency, energy consumption, and insertion loss. As VOPD is widely employed as a benchmark for application specific NoC [14], [15], we compare RONO with optical NoC based on mesh using this application. The mesh network adopts genetic algorithm (GA) and simulated annealing (SA) to map the VOPD application. Both of the networks employ circuit-switching mechanism. Setup packet is set to be 32-bit and data packet is 1024-bit long. The transmission bandwidth is assumed to be 12.5Gbps, which can be achieved by the current nanophotonic devices [16].

The comparison of ETE (End to End) delay is shown in Fig. 4. RONO has a doubled saturation load than that of mesh topology, no matter GA or SA algorithm is used. The performance improvement of RONO is mainly brought by shorter hops. And the direct connections of adjacent cores

Configuration Algorithm for RONO

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1: initialize  $N \leftarrow$  the number of IP cores,  $Q \leftarrow N$ ;
2: do {
3:   get x and y satisfying  $Q = x \times y$ ;
4:    $Q \leftarrow Q + 1$ ;
5: } while (x, y don't satisfy the constraints of two dimensions)
6: for (all IP cores  $n_i$ ) /*divide IP cores into several clusters*/
7:   if the communication volume from  $n_i$  to  $n_j$  is the highest then
8:     create IP pair( $n_i, n_j$ );
9:   end if
10: end for
11: for (all IP pairs)
12:   if IP pair( $n_i, n_j$ ) and IP pair( $n_k, n_l$ ) exist at the same time then
13:     delete IP pair( $n_i, n_j$ ) and IP pair( $n_k, n_l$ );
14:     create cluster( $n_i, n_j$ );
15:   end if
16: end for
17: put left IP pairs in order as the intra-pair communication volume decreases;
18: for (all left IP pairs( $n_i, n_j$ ))
19:   if  $n_i$  or  $n_j$  is one element in one existed cluster A then
20:     if the number of IP cores in cluster A is less than 4 then
21:       add  $n_i$  or  $n_j$  into cluster A
22:     end if
23:   else then
24:     delete IP pair( $n_i, n_j$ ), construct cluster( $n_i$ ) or ( $n_j$ );
25:   end else
26: end if
27: end for
28: for (all clusters) /*map clusters to RONO*/
29:   calculate intra-cluster communication volume of each cluster
30: end for
31: search for cluster B of which intra-cluster communication volume is the highest;
32: map IP cores in cluster B to RONO with performance optimized;
33: label cluster B mapped;
34: while (there are clusters unmapped) then
35:   search for one unmapped cluster C from which the communication volume
   is the highest to the mapped clusters;
36:   map IP cores in cluster C to RONO with performance optimized;
37: end while

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Fig. 3 The configuration algorithm of RONO.

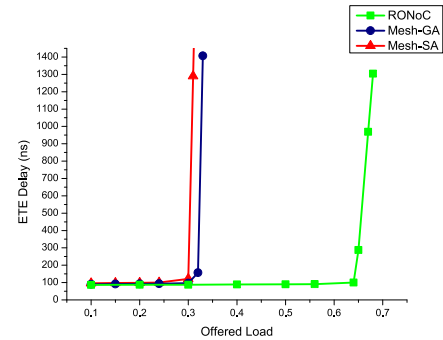


Fig. 4 Latency performance comparison.

also contribute to the performance gain, because these cores can communicate directly without a path reservation phase.

The energy consumption comprises the energy for path reservation in the electrical control network ($E_{Electrical}$) and the energy for control related optical devices in the optical network ($E_{Optical}$). The specific calculation of the energy consumption is determined by (1),

$$\begin{aligned}
 E_{total} &= E_{Electrical} + E_{Optical} \\
 &= (E_{setup} + E_{ack}) + \left(\sum t_{on} \cdot P_{ring} + E_{O/E} + E_{E/O} \right) \quad (1)
 \end{aligned}$$

where E_{setup} and E_{ack} are the energy consumed by the setup packets and ACK packets, P_{ring} is the power for tuning an MR, $E_{E/O}$ and $E_{O/E}$ are the energy needed in transmitter

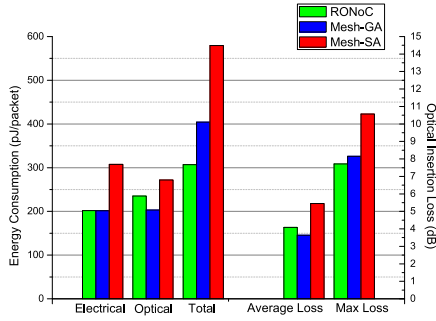


Fig. 5 Comparisons of energy consumption and insertion loss.

and receiver circuits. Figure 5 illustrates the energy comparison of ROnoC and mesh. The electrical energy and optical energy consumed by each packet in these three scenarios hardly have an obvious difference, but the average total energy in ROnoC is only 25% and 47% of that in Mesh-GA and Mesh-SA, respectively. The main reason is that many packets in ROnoC are transmitted by skipping the path reservation phase, therefore they have no energy consumed in the electrical control network.

The power attenuation is dependent on the optical losses, such as waveguide propagation (IL_{travel}), waveguide bendings (IL_{bend}), crossings (IL_{cross}), off and on-resonance of passive or active MRs ($IL_{through}$ and IL_{drop}), modulators ($IL_{modulator}$), detectors ($IL_{detector}$), etc. The analysis of insertion loss is based on the following formula,

$$Loss = L_{wg} \cdot IL_{travel} + \sum IL_{bend} + \sum IL_{cross} + \sum IL_{through} + \sum IL_{drop} + IL_{modulator} + IL_{detector} \quad (2)$$

where L_{wg} is the length of the waveguide. Although much more waveguide crossings and ring drops emerge in the ROnoC, ROnoC can still maintain a similar average optical loss as the Mesh-GA does. As the Fig. 5 shows, the max optical loss of ROnoC is even a bit lower than that of Mesh-GA. The shorter hop of ROnoC amortizes the dense loss penalty of its architecture.

5. Conclusion

The ROnoC architecture is proposed to enable the topology to dynamically match the communication patterns of various applications. The reconfiguration operation is simple, which just needs to power on or off the related resonators. A configuration algorithm for ROnoC is developed to achieve lower power consumption. The simulation results show that ROnoC has a much higher throughput and smaller power consumption. In our future work, some dynamic traffic patterns, like all to all communication, will be considered. New configuration algorithm will be developed.

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