

An FPGA Implementation Method based on Distributed-register Architectures

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Abstract: In order to reduce the effects of interconnection delays in recent FPGA chips, circuit designs based on distributed-register architectures (which we call DR-based circuit designs) are important. Several methods for DR-based circuit designs have been proposed, where high-level synthesis techniques are effectively utilized. However, no methods have been proposed yet to *practically implement* DR-based circuits on FPGA chips. In this paper, we propose an FPGA implementation method based on DR architectures and apply it to a DR-based circuit. The implementation result shows that it operates on an FPGA chip with 21% faster than the circuit based on a traditional architecture.

Keywords: FPGA implementation, interconnection delay, distributed-register architecture, high-level synthesis

1. Introduction

In order to reduce the effects of interconnection delays in recent FPGA chips, circuit designs based on distributed-register architectures (which we call DR-based circuit designs) are important. Since a DR-based circuit has local registers for each functional unit (FU), it can achieve smaller interconnection delays between FUs and registers compared with a traditional shared-register-based (SR-based) circuit.

Several methods for DR-based circuit designs have been proposed [1], [2], where high-level synthesis (HLS) techniques are effectively utilized. These methods introduce, in HLS stage, floorplanning of modules which consist of FUs and local registers, which enables estimation and handling of interconnection delays in HLS. On the other hand, when we utilize these methods for FPGA implementation, we have to appropriately incorporate floorplanning information which is decided in HLS stage into FPGA implementation stage unlike SR-based circuit designs. However, no methods have been proposed yet to *practically implement* DR-based circuits on FPGA chips.

From this reason, we propose, in this paper, an FPGA implementation method based on DR architectures and apply it to a DR-based circuit designed by the approach in Ref. [2]. The contributions of this paper are summarized as follows:

- (1) The method to practically implement DR-based circuits on FPGA chips is presented.
- (2) The operation of an FPGA-implemented DR-based circuit is verified, which achieves 21% faster than the SR-based circuit.

2. FPGA-implemented DR-based Circuit

For FPGA implementation, “Xilinx Virtex-7 (XC7V2000T-2FLG1925)” [5] on the evaluation board “TB-7V-2000T-LSI” is utilized in this paper. The board has off-chip memories realized by DDR3 SDRAM. In our experiments, data communication between PC and the board is performed via USB. The actual evaluation environment with this board is shown in Fig. 1.

Figure 2 illustrates the diagram of an FPGA-implemented DR-based circuit. It consists of a DR-based circuit, interface circuits and Off-chip memories. The interface circuits include USB transmission interface, Write and read memory interface, and Clock/reset generator^{*1}.

Data transmission between PC and Off-chip memories can be realized via USB transmission interface. According to a start instruction from PC, input data are read into the DR-based circuit from Off-chip memories via Write and read memory interface. Similarly, according to a termination instruction from the DR-based circuit, output data are written back to Off-chip memories.



Fig. 1 Evaluation environment.

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^{*1} In this paper, we have utilized the interface circuits whose configurations are similar to Ref. [4].

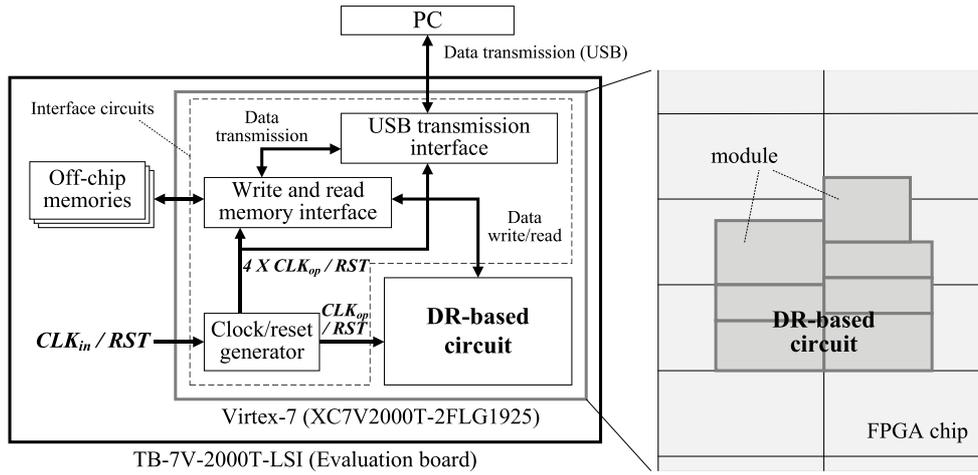


Fig. 2 Diagram of FPGA-implemented DR-based circuit.

Table 1 Implementation results.

	Clock period constraint in HLS [ns]	Parameters (α, β)	Operation clock period CLK_{op} [ns]	#Steps	Latency [ns]	#Slices	#LUTs	#FFs	Total impl. time [s]	Operation time on Xilinx Virtex-7 [ns]
SR-based circuit	6.4	(8, 25)	6.378	10	63.78	1268	2943	3394	1179	65.87
DR-based circuit	5.0	(5, 20)	4.983	10	49.83	1303	2779	3233	710	51.92

In Clock/reset generator, the input clock period CLK_{in} which is provided from the board (= 19.933 ns) is modulated to the operation clock period CLK_{op} which is calculated by:

$$CLK_{op} = CLK_{in} \times \frac{\alpha}{\beta} \text{ [ns]}, \quad (1)$$

where the parameters α and β satisfy the following conditions:

Condition 1 $\alpha \in \mathbb{N}$ and $\beta \in \mathbb{N}$.

Condition 2 $\beta \leq 64^{*2}$.

3. FPGA Implementation Method Based on DR Architectures

3.1 Implementation Flow

We propose an FPGA implementation flow based on DR architectures in Fig. 3. In this paper, we use the method [2] for DR-based circuit designs where HLS techniques are effectively utilized. We also use Xilinx Vivado Design Suite 2014.2 [6] for FPGA implementation.

In this implementation flow, in Step 1, we first design a DR-based circuit for a target application. Step 1 is performed based on a control-data flow graph (CDFG) which represents the application’s behavior, an FU constraint, a clock period constraint, and FPGA information obtained from Ref. [3]. In this step, we obtain *not only* an RTL description of a DR-based circuit *but also* a result of module floorplanning. Next in Step 2, we perform logic synthesis of the RTL description together with three interface circuits and obtain a gate-level circuit. In this step, the operation clock period CLK_{op} is given so that CLK_{op} (calculated by Eq. (1)) is almost equal to the clock period constraint in Step 1. We set the parameters α and β in Eq. (1) as follows:

We first calculate the value of $\frac{\alpha}{\beta}$ so that the operation clock period CLK_{op} is equal to the clock period constraint given in HLS

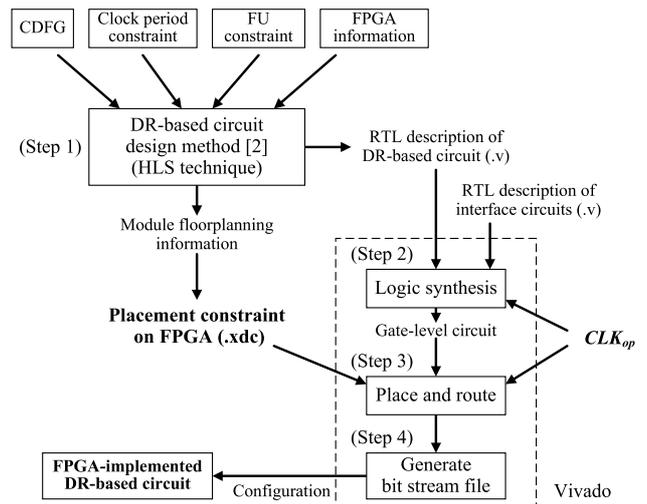


Fig. 3 FPGA implementation flow based on DR architectures.

stage by:

$$\frac{\alpha}{\beta} = CLK_{op} \div CLK_{in}, \quad (2)$$

where CLK_{in} is approximated to 20 ns. Then the parameters α and β are determined so as to satisfy Conditions 1 and 2^{*3,*4}.

Then in Step 3, we perform place and route for the gate-level circuit. It should be noted that, in Step 3, the placement of the DR-based circuit is performed based on the result of module floorplanning in Step 1. Finally a bit stream file is generated in Step 4 and we obtain, through configuration, the FPGA-implemented DR-based circuit.

3.2 Implementation Results and Conclusions

We have implemented a DR-based circuit on the FPGA chip

^{*3} The parameter β was set within a range of 20–30 in our experiment.

^{*4} The parameters α and β are explicitly given to the RTL description of Clock/reset generator.

by applying our proposed implementation flow as in Fig. 3 for a benchmark application DCT (48 operation nodes, not including conditional branches). In this implementation, we have assumed 4 adders and 4 multipliers as the FU constraint [2]. In order to show the validity of DR-based circuits, we have also implemented its SR-based circuit on the FPGA chip^{*5}.

Table 1 shows the implementation results. The 1st column shows the target architecture of the implemented circuit and the 2nd column shows the clock period constraint given in HLS stage. The 3rd column shows the parameters α and β in Eq. (1) which are obtained according to Section 3.1. The 4th column shows the operation clock period CLK_{op} calculated by Eq. (1). The 5th column shows the number of control steps obtained in HLS stage and the 6th column shows the circuit latency calculated by multiplying the 4th and 5th columns. The 7th to 9th columns show the number of slices, the number of look-up tables (LUTs) and the number of flip-flops (FFs) of the implemented circuit, respectively. The 10th column shows the total implementation time and the 11th column shows the measured operation time of the implemented circuit on the FPGA chip^{*6}.

Both DR-based and SR-based circuits have been designed so that they can operate with minimum latency. We have verified the operation of each FPGA-implemented circuit according to the following procedure:

For the FPGA-implemented circuit, we have provided the operation clock period CLK_{op} as shown in the 4th column of Table 1, and operated with a set of input values. We have then obtained a set of output values from the circuit and compared each value with the theoretical one.

We have verified the operations of FPGA-implemented DR-based and SR-based circuits according to the above procedure. The 11th column of Table 1 is 2.09 ns larger than the 6th column of Table 1. It is because the 11th column of Table 1 includes the data transmission delays from PC to the FPGA chip. As demonstrated in the 11th column of Table 1, the DR-based circuit can operate on the FPGA chip 21% faster than the SR-based circuit.

4. Conclusion

In this paper, we have proposed an FPGA implementation method utilizing HLS techniques for DR architectures and applied it to a DR-based circuit of DCT application designed by the approach in Ref. [2]. As the contributions of this paper, we have presented the method to practically implement DR-based circuits including interface circuits on FPGA chips. Then, we have verified the operation of an FPGA-implemented DR-based circuit, which has achieved 21% faster than the SR-based circuit on the FPGA chip.

In the future, we will apply our method to other benchmark applications and compare them with the circuits which are implemented by commercial HLS tools.

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^{*5} Unlike DR-based circuit designs, SR-based circuit designs do not consider floorplanning of modules in HLS stage.

^{*6} We have performed the operation 1,000,000,000 times and calculated the operation time based on the total time.



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