IPSJ Transactions on System LSI Design Methodology Vol. 2 93–102 (Feb. 2009)

Regular Paper

A GIDL-Current Model for Advanced MOSFET Technologies without Binning

Ryosuke Inagaki,[†1,†2] Norio Sadachika,[†3]
Dondee Navarro,[†4] Mitiko Miura-Mattausch[†3]
and Yasuaki Inoue[†1]

A GIDL (Gate Induced Drain Leakage) current model for advanced MOSFETs is proposed and implemented into HiSIM2, complete surface potential based MOSFET model. The model considers two tunneling mechanisms, the band-to-band tunneling and the trap assisted tunneling. Totally 7 model parameters are introduced. Simulation results of NFETs and PFETs reproduce measurements for any device size without binning of model parameters. The influence of the GIDL current is investigated with circuits, which are sensitive to the change of the stored charge due to the GIDL current.

1. Introduction

Advanced MOSFET technologies are drawn by aggressive scaling of device size, where reduction of the gate-oxide thickness is inevitable. It is already well-known that the reduction results in enhanced tunneling currents [1], which are observed as leakage currents flowing into the channel. The gate leakage current is caused by quantum mechanical effects and changes in carrier transport. As one of the leakage currents, the gate induced drain leakage (GIDL) current becomes important especially during accumulation operation. The GIDL current is caused by the tunneling taking place in the narrow-depletion region at the drain underneath the gate oxide. Electron-hole pairs are generated by the tunneling of valance band electrons into the conduction band and collected by the drain and the substrate separately. The electron-hole pair generation is modeled by the direct band-to-band tunneling (BTBT), but also through the trap assisted tunneling (TAT). Thus the GIDL current is written from the BTBT current and TAT current integration of the generation function over the depleted gate drain overlap region [2),3)]. The BTBT mechanism is known to be dominant in the high electric field [4)] whereas TAT current is dominant in the low electric field region [5)]. This trap assisted tunneling effect could be described by the conventional Shockley-Read-Hall (SRH) expression for recombination via traps [2),4)]. Essentially, the GIDL current is generated at the drain junction under the accumulation condition. The drain-to-source voltage (Vds) increase induces a very narrow potential well in the drain just under the gate, causing carrier generation. Therefore, the GIDL current is strongly dependent on Vds. At further reduced the gate-to-source voltage (Vgs) values the direct gate tunneling starts to dominate the GIDL current measurements, resulting in Vds independence [6)].

Existing compact model does not include the GIDL current model. BSIM3 [7)] has no description about GIDL current. On the other hand, BSIM4 [4),8)], PSP102 [9),10)] and HiSIM1 [11)] models include GIDL current models. These descriptions are not enough for the accuracy on the bias dependences when we consider the power consumption and circuit performance in SPICE circuit simulation. The accuracy is still insufficient for advanced technologies. The development of accurate compact model for the GIDL current is not simple due to many complicated mechanisms influencing on the direct tunneling.

For advanced MOSFET circuit simulation, the GIDL model should be derived from the underlying physical mechanism. Alternatively, modeling from the physical mechanism and adding semi-empirical approach for reproducing the measurements are also effective. Several GIDL current models have been reported in the published papers. However, there are very fewer papers about the model accuracy for reproducing measurements of various gate width and gate length, as far as authors know.

In this paper, we propose a new GIDL current model without binning implemented into HiSIM2 (Hiroshima-University STARC IGFET Model) [6),⋆2]. The

†1 Waseda University
†2 Semiconductor Technology Academic Research Center
†3 Hiroshima University
†4 Silvaco Japan Co., Ltd.

⋆1 The real author is the Editorial Board of the Trans. IPSJ.
⋆2 This work was presented at the 2007 IEEE International Conference on Communications, Circuits and Systems, Kokura, Japan, July 2007 [12)].

model of GIDL tunneling current is based on the basic tunneling theory. The accuracy and validity of the model are investigated for measurements with wide variety of device geometries in one model parameter set [6]. Additionally, we investigate the strong influence of GIDL current on the performance of the resistor load inverter circuit and differential amplifier circuit.

2. Former Modeling of the GIDL Current

Advanced MOSFET GIDL current model such as BSIM4, PSP102, and HiSIM1 include different models. The model equations and their performances are summarized.

2.1 BSIM4 Model

BSIM4 model is presently the industry-standard MOSFET model for deep-submicron digital and analog circuit designs developed by the University of California at Berkeley. The GIDL/GISL currents and its body bias effect are modeled as [4),8),13),14)]

$$I_{GIDL} = AGIDL \cdot W_{effcj} \cdot N_f \cdot \frac{V_{ds} - V_{gse} - EGIDL}{3 \cdot T_{oxe}} \cdot exp\left(-\frac{3 \cdot T_{oxe} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL}\right) \cdot \frac{{V_{db}}^3}{CGIDL + {V_{db}}^3}, \quad (1)$$

$$I_{GISL} = AGISL \cdot W_{effcj} \cdot N_f \cdot \frac{-V_{ds} - V_{gde} - EGISL}{3 \cdot T_{oxe}} \cdot exp\left(-\frac{3 \cdot T_{oxe} \cdot BGISL}{-V_{ds} - V_{gde} - EGISL}\right) \cdot \frac{{V_{sb}}^3}{CGISL + {V_{sb}}^3}, \quad (2)$$

where parameters $AGIDL$, $BGIDL$, $CGIDL$ and $EGIDL$ are model parameters for the drain side, and $AGISL$, $BGISL$, $CGISL$ and $EGISL$ are the model parameters for the source side. $CGIDL$ and $CGISL$ account for the body-bias dependence of I_{GIDL} and I_{GISL}, respectively. W_{effcj} and N_f are the effective width of the source/drain diffusions and the number of fingers [8)].

The BSIM4 model includes only 4 model parameters. To reproduce measurements, not only body bias dependence, but also drain bias dependence is not satisfactory without binning [15)]. Moreover, BSIM4 has mathematical method for the continuity of Vdb=0 in the last term. Therefore, improvements on the model are still required.

2.2 PSP102 Model

The PSP model is a compact MOSFET model, recently selected as the next standard model by CMC for digital, analog, and RF-design, which has been jointly developed by the Arizona State University and NXP, originally the merged model of SP by the Pennsylvania State University and MOS Model 11 by Philips Research. PSP is a surface-potential based MOSFET model, containing all relevant physical effects (mobility reduction, velocity saturation, DIBL, gate current, lateral doping gradient effects, STI stress, etc.), relevant for RF applications [9),10)].

In model equations, the GIDL current is calculated

$$I_{gidl} = I_{gixl}(V_{OVL}, V_{DS} + V_{SB}), \quad (3)$$

$$I_{gisl} = I_{gixl}(V_{OV0}, V_{SB}), \quad (4)$$

$$I_{gixl}(V_{OV}, V) = -A_{GIDL} \cdot t \cdot exp\left(-\frac{B_{GIDL}}{V_{tov}}\right) \quad for\ V_{OV} > 0, \quad (5)$$

$$I_{gixl}(V_{OV}, V) = 0 \quad for\ V_{OV} \leq 0, \quad (6)$$

$$t = V \cdot V_{tov} \cdot V_{OV}, \quad (7)$$

$$V_{tov} = \sqrt{{V_{OV}}^2 + {C_{GIDL}}^2 \cdot V^2 + 10^{-6}}, \quad (8)$$

where A_{GIDL}, B_{GIDL} and C_{GIDL} are the GIDL current coefficients and some additional parameters for binning [9),10)].

The quality of the PSP model has issues in continuity of the model equations, because two equations (Eqs. (5) and (6)) are alternatively applied according to the bias condition. Moreover, PSP has local binning method to extract the 9 model parameters. It is well-known that the boundaries of binning areas induce discontinuities among different segmented areas.

2.3 HiSIM1 Model

HiSIM1 is a MOSFET model for circuit simulation based on the drift-diffusion approximation with the surface-potential description, which was originally developed by Pao and Sah [16)]. The most important advantage of the drift-diffusion approximation is the unified description of the device characteristics for all bias

conditions. The physical reliability of the approximation has been proved by 2D device simulations with channel lengths even down to 0.1 um. HiSIM1 is proposed by Hiroshima University together with STARC (Semiconductor Technology Academic Research Center) [11]. In HiSIM1, the GIDL current equation is

$$I_{GIDL} = q \cdot GIDL1 \cdot \frac{E^2}{Eg^{1/2}} \cdot exp\left(-GIDL2 \cdot \frac{Eg^{3/2}}{E}\right) \cdot Weff, \tag{9}$$

$$E = \frac{GIDL3 \cdot V_{ds} - V'_G}{Tox}, \tag{10}$$

$$V'_G = V_{gs} - VFBC + \Delta Vth, \tag{11}$$

where *GIDL*1, *GIDL*2, and *GIDL*3 are the GIDL current coefficients, V_G' is the effective gate voltage, ΔVth is the threshold shift due to short channel effect ($\Delta Vthsc$) and due to reverse short channel effects by the pocket implantation ($\Delta Vthlp$). The GISL current is written without introducing additional model parameters in the following equations assuming the symmetrical source/drain contact [11].

$$I_{GISL} = q \cdot GIDL1 \cdot \frac{E^2}{Eg^{1/2}} \cdot exp\left(-GIDL2 \cdot \frac{Eg^{3/2}}{E}\right) \cdot Weff, \tag{12}$$

$$E = \frac{-GIDL3 \cdot V_{ds} - V''_G}{Tox}, \tag{13}$$

$$V''_G = V_{gd} - VFBC + \Delta Vth. \tag{14}$$

HiSIM1 includes 3 model parameters, describing not only gate bias, but also drain bias dependence like BSIM. The main difference is that HiSIM1 model does not need the binning option to extract model parameters. However, reproduction of the gate bias dependence is not sufficient.

2.4 Summary of the Former Models

It is concluded that none of the existing models, *BSIM4*, *PSP102*, and *HiSIM1* meet all of requirements to be fulfilled for accurate circuit simulations. It consumes significant time to extract the model parameters because the binning process is needed. Moreover, complicated model descriptions result in discontinuity issues. The summary is shown in **Table 1**.

Table 1 Summary of the former models.

Model	*Parameters*	*Difficultiy of the parameter extraction and the handling*
BSIM4	4 (*n bin)	with binning, mathematical term
PSP102	3 (+9 bin)	with binning, discontinuity issue
HiSIM1	3	without binning, no fit to gate bias dependence

*n is the number of binning

3. Proposed Modeling of the GIDL Current

It is known that the GIDL current occurs at the drain as schematically shown in **Fig. 1**. A simulated drain current I_D with a 2D-device simulation [17] is demonstrated in **Fig. 2**. Two different tunneling mechanisms as a function of applied voltages are depicted in Fig. 2.

In general, the BTBT current equation is written as a function of the electric field E with fitting parameters A and B [18].

$$I_{BTBT} = A \cdot E \cdot exp(-B/E). \tag{15}$$

The electric field E is calculated by Eq. (16).

$$E = \frac{Vdg - q \cdot Eg}{3 \cdot Tox}, \tag{16}$$

where Vdg is the drain to gate voltage, q is electron charge, Eg is the band-gap energy, Tox is the gate-oxide thickness. HiSIM1 GIDL model equation is similar to this equation.

On the other hand, the TAT current and recombination current density equation is

$$J_{TAT} = J(TNOM) \cdot exp\left(\frac{-Eg(TNOM)}{k_B T} \cdot X \cdot \left(1 - \frac{T}{TNOM}\right)\right), \tag{17}$$

where J is the saturation junction current density, k_B is Boltzmann constant, T is absolute temperature, $TNOM$ is normalized temperature, X is the exponential temperature coefficient of the junction current [8]. This current is already described in the junction current of HiSIM2 model as the same effect in Eq. (18).

$$I_j = A \cdot js + P \cdot jssw + W_{eff} \cdot NF \cdot jsswg, \tag{18}$$

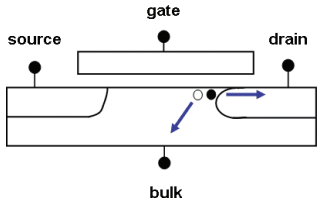

Fig. 1 GIDL current mechanism. The black circle represents an electron and tunnels into the drain. The reminded hole depicted by a white circle flows into the bulk terminal.

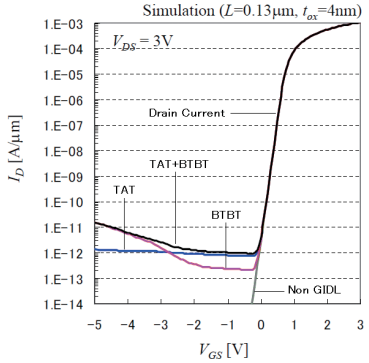

Fig. 2 Simulated GIDL current as a function of the gate voltage Vg. Two tunneling mechanisms (BTBT: band-to-band tunneling, TAT: trap-assisted-tunneling) are added [17].

$$jsswg = JS0SWG \cdot exp\left(\frac{Eg(Tnom)\cdot\beta(Tnom) - Eg\cdot\beta + XTI\cdot log(T/Tnom)}{NJSWG}\right), \quad (19)$$

where A and P are the area and the perimeter parameters of the drain or source region. The instance parameter NF is the number of fingers. The current density js, $jssw$, and $jsswg$ are described the area, the sidewall, and the gate edge of the regions. The $jsswg$ is consisted of the band-gap energy: Eg, the reverse constant of thermal voltage: β, the absolute temperature: T, the normalized temperature: $Tnom$, the model parameter of TAT current coefficient: $JS0SWG$, the model parameter of temperature coefficient of the junction density: XTI, and the model parameter of the gate edge emission coefficient: $NJSWG$ [19].

3.1 GIDL Current Equations

The GIDL current I_{GIDL} is proposed on the basis of the direct tunneling mechanism as Eq. (20).

$$I_{GIDL} = \alpha \cdot Ids \cdot \Delta Y, \quad (20)$$

where ΔY is the length between the narrow potential well at the drain contact (see Fig. 1). The coefficient α is the direct tunneling coefficient, and Ids is the drain current including the generation current [6].

The proposed GIDL current model considers the BTBT current. At first, the electric field E is calculated by Eq. (21).

$$E = \frac{V}{Tox\cdot(1+\frac{1}{\Delta Tox})}, \quad (21)$$

where Tox is the gate-oxide thickness, ΔTox describes the correction due to the gate width variation, and V is the bias voltage between the drain/gate voltage and the bulk voltage, calculated by Eq. (22).

$$V = GIDL3\cdot(Vds + GIDL5) - GIDL4\cdot Vgs - Vbs + GIDL7\cdot\Delta Vth, \quad (22)$$

where ΔVth is the threshold voltage (Vth) correction as a function of the drain voltage, written in Eq. (23).

$$\Delta Vth = \Delta Vthsc + \Delta Vthlp + \Delta Vthw, \quad (23)$$

where $\Delta Vthsc$ is the threshold voltage shift due to short channel effect, $\Delta Vthlp$ is the threshold voltage shift due to reverse short channel effects due to impurity concentration inhomogeneity in the direction parallel to the channel caused by the pocket implantation, and $\Delta Vthw$ is Vth reduction for reduced channel width with the shallow trench isolation. The variables $\Delta Vthsc$, $\Delta Vthlp$ and $\Delta Vthw$ are calculated by real device constants such as flat-band voltage, substrate doping impurity concentration, maximum peak of pocket impurity concentration, and length of the pocket extension into the channel. The effective ΔTox is calculated by Eq. (24) using the semi-empirical verification for physical device modeling and reproducing the measurements with two types of 90 nm MOSFET technologies.

$$\Delta Tox = \frac{Cox}{GIDL6\cdot WFC\cdot Weff}, \quad (24)$$

where Cox is the gate-oxide capacitance, $Weff$ is the effective gate width, WFC is a model parameter for including the edge fringing capacitance effects, and

Table 2 GIDL current model parameters.

Parameters	*Unit*	*Remarks*
*GIDL*1	$AV^{-3/2}C^{-1}m$	magnitude coefficient
*GIDL*2	$V^{-1/2}m^{-1}$	electric field coefficient
*GIDL*3	-	Vds dependence
*GIDL*4	-	Vgs dependence
*GIDL*5	V	Vds correction
*GIDL*6	m	gate width dependence
*GIDL*7	-	ΔVth dependence

*GIDL*6 is a model parameter describing gate width dependence. The band-gap voltage *Bgap* is calculated by Eqs. (25), (26).

$$Eg12 = \sqrt{Bgap}. \tag{25}$$

$$Eg32 = Bgap \cdot Eg12. \tag{26}$$

The final GIDL current I_{GIDL} is

$$I_{GIDL} = GIDL1 \cdot \frac{E^2}{Eg12} \cdot Weff \cdot qe \cdot exp(-GIDL2 \cdot \frac{Eg32}{E}), \tag{27}$$

where *GIDL*1 is a model parameter determining of I_{GIDL} magnitude and *GIDL*2 is a model parameter for adjusting electric field. The equation is based on the HiSIM1 description considering BTBT with the model parameter *GIDL*4 as a modification of the electric field. HiSIM2 with the proposed model is implemented into Spice3f5 for model verification. The gate induced source leakage (GISL) current is calculated with same equation as the GIDL current described without introducing the new additional model parameters as HiSIM1. The selection either GIDL current or GISL current is done by the polarity of the current flow [11].

3.2 GIDL Current Model Parameters

The model parameter set of the GIDL current model is shown in **Table 2**. It requires totally 7 model parameters valid all bias conditions for any device size without binning option.

4. Calculation Results with the Former Model

4.1 Former Parameter Extraction

The GIDL calculated results of HiSIM1 former model are compared with the measurements in **Fig. 3** [11]. The gate size of the device is 10 um width and 10 um length in 90 nm technology.

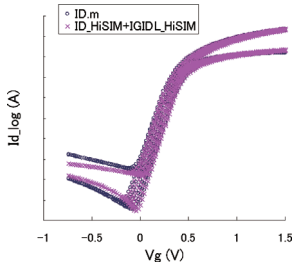

Fig. 3 Calculated results of NFET with HiSIM1 comparison to measurements. Two Vds biases (50 mV and 1.0 V) are studied. Vgs bias is varied from −0.8 V to 1.5 V with step 20 mV, and Vbs bias is fixed to 0 V. The circles are measurements, the crosses are HiSIM1 calculation results.

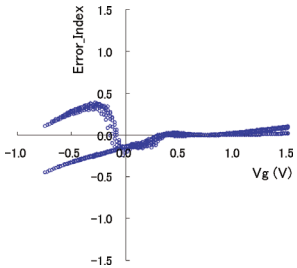

Fig. 4 The former extraction error of NFET.

4.2 Former Extraction Error

The extraction error is shown as the difference between the measurements and the simulation results. We define the error equation in Eq. (28), where *sim* means simulation results, *msr* means measurements and E is error index that we evaluate fitting accuracy of the parameter extraction.

$$10^E = \frac{sim}{msr}. \tag{28}$$

The accumulation region of HiSIM1 GIDL model is not fit to measurements. Therefore, the maximum error is up to +0.38 / −0.45 in the accumulation region, except the error index of the drain current in **Fig. 4**. The extraction errors of other gate size are same tendency.

5. Calculation Results with the Proposed Model

5.1 Proposed Parameter Extraction

The device sizes investigated are summarized in **Table 3** for NFETs and **Table 4** for PFETs with a 90 nm technology. Calculated GIDL with HiSIM2 including the proposed GIDL current model are compared with measurements in **Fig. 5** a-e for NFETs and **Fig. 6** a-b for PFETs. One model parameter set is varied for all bias conditions and all studied device sizes without binning option.

5.2 Proposed Extraction Error

The extraction error map of studied 5 NFETs is shown in **Fig. 7** a-e. The maximum error in the accumulation region is +0.24 / −0.22, except the error index of the drain current.

The extraction error map of studied 2 PFETs is shown in **Fig. 8** a-b. The maximum error in the accumulation region is +0.12 / −0.28, except the error index of the drain current.

Compared with the former model, the maximum error of the proposed model is improved from totally 0.83 to 0.46 of NMOS, and to 0.40 of PMOS by the error index. The main reason of this improvement is due to the Vds and Vgs dependence of the GIDL current model improvement.

Table 3 Studied devices.

Device	*Type*	*Wgate / Lgate**
A	NMOS	0.12 / 0.24
B	NMOS	10.0 / 0.08
C	NMOS	10.0 / 0.24
D	NMOS	0.12 / 0.4
E	NMOS	10.0 / 10.0

* Unit:um

Table 4 Studied devices.

Device	*Type*	*Wgate / Lgate**
F	PMOS	10.0 / 0.09
G	PMOS	0.12 / 10.0

* Unit:um

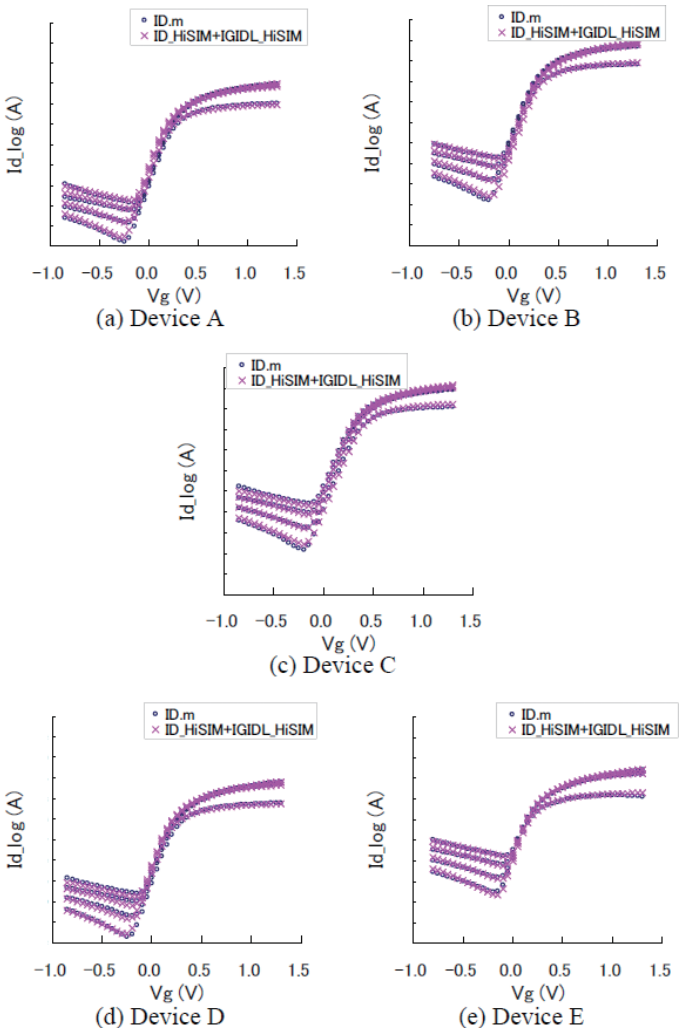

Fig. 5 Comparison of calculated results with measurements of NFETs. Four Vds biases (50 mV, 500 mV, 1.0 V, and 1.4 V) are studied, Vgs bias is varied from −0.8 V to 1.3 V with step 20 mV, and Vbs bias is fixed to 0 V. The circles are measurements, the crosses are HiSIM2 calculation results.

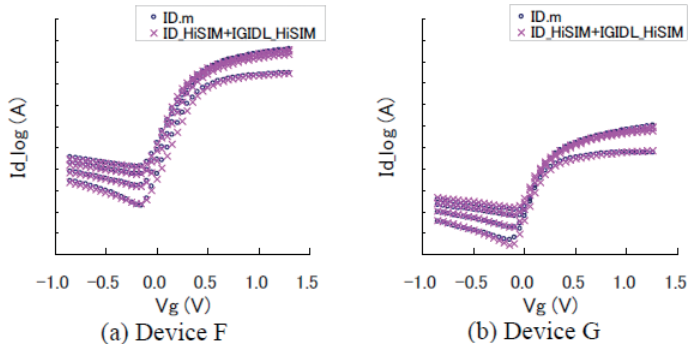

Fig. 6 Comparison of calculated results with measurements of PFETs. Four Vds biases (50 mV, 500 mV, 1.0 V, and 1.4 V) are studied, Vgs bias is varied from −0.8 V to 1.3 V with step 20 mV, and Vbs bias is fixed to 0 V. The circles are measurements, the crosses are HiSIM2 calculation results.

6. Influence on Circuit Performance

The influence of the GIDL current on circuit performances is investigated with the resistor load inverter circuit and the differential amplifier circuit. The simulation results are compared with and without the GIDL current. The strong influence on the GIDL current effect is shown in these circuit performances.

6.1 Resistor Load Inverter Circuit

The test circuit is shown in **Fig. 9**. The input signal is directly connected to the gate terminal of NMOS. The output signal is observed on drain terminal of NMOS. This circuit usually uses a waveform conversion circuit with a sine wave as an input. It provides a simple study of the GIDL current influence.

The simulated results are shown in **Fig. 10** with and without the GIDL current. The clear difference is caused by the GIDL current influence. The reason for the difference is caused by the increased GIDL leakage current as a function of the gate voltage in the accumulation region. Such drastic change of the waveform causes a serious problem in predicting circuit performance without the GIDL current.

6.2 Differential Amplifier Circuit

The test circuit is shown in **Fig. 11**. In this circuit, the DC bias voltage is fixed

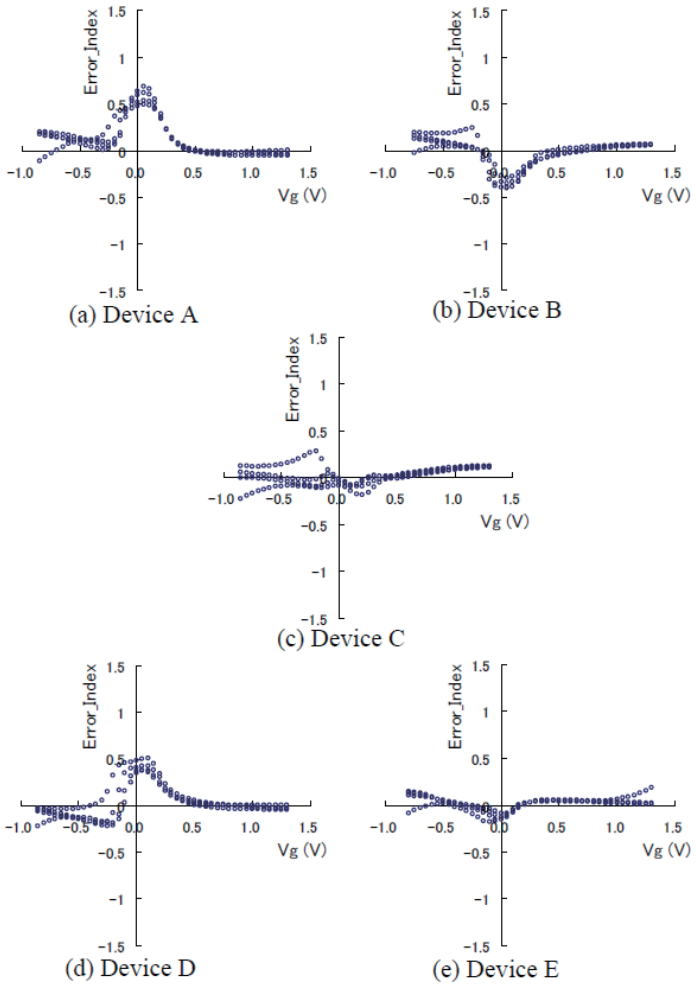

Fig. 7 The extraction error of studied 5 NFETs.

to 0.9 V given on the gate terminal of MN2, and the DC input voltage is varied from 0.5 V to 1.3 V given on the gate terminal of MN1. The output terminal is connected to 1 Meg ohm resistor load with 0.9 V DC voltage, and the current source *I_tail* is set to 0.1 uA DC current. We check the linearity of the studied

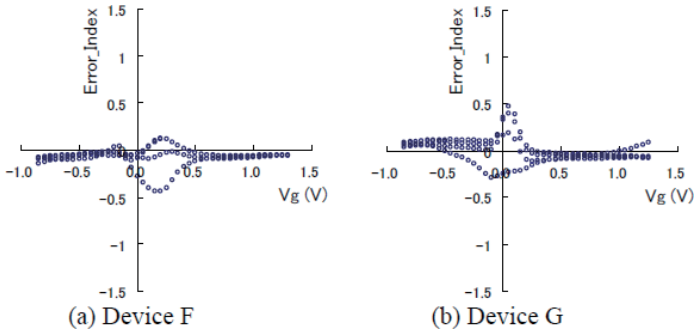

Fig. 8 The extraction error of studied 2 PFETs.

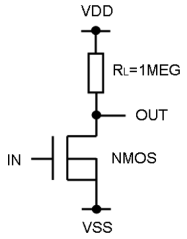

Fig. 9 Schematics of the resistor load inverter circuit, where W/L = 100 um / 0.18 um with a 0.18 um technology. VDD = 1.8 V and VSS = 0 V are given.

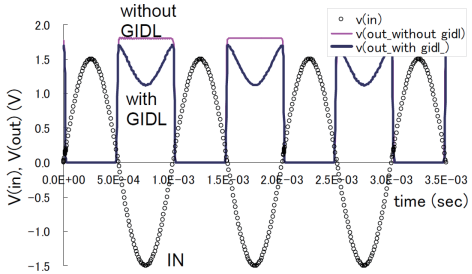

Fig. 10 Simulation results of the resistor load inverter circuit, with and without the GIDL current.

differential amplifier by DC input voltage of *IN+* terminal.

The simulated results are shown in **Fig. 12** with and without the GIDL current. The difference observed in low input voltage is caused by the GIDL current

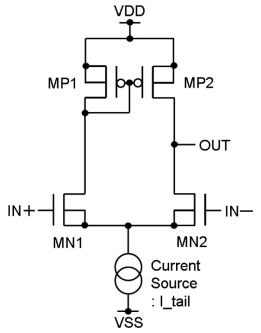

Fig. 11 Schematics of the differential amplifier, where W/L = 100 um / 0.18 um with a 0.18 um technology. VDD = 1.8 V and VSS = 0 V are given.

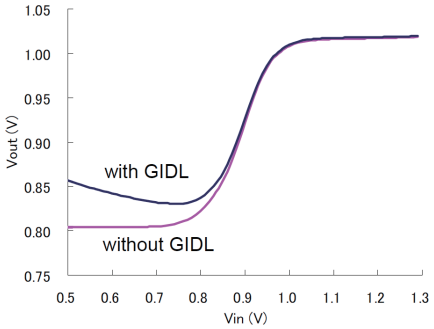

Fig. 12 Simulation results of the differential amplifier, with and without the GIDL current.

influence. The GIDL current becomes manifest at high drain voltage and low gate voltage in comparison to the source voltage of the device. The reason of the difference is caused by the bulk terminal connection of the differential pair transistor, MN1 and MN2. The voltage between the gate terminal and the source terminal of MN1 is reversed in the low input voltage of MN1.

7. Conclusions

We have proposed a GIDL current model for the advanced technologies based on the complete surface potential based model HiSIM2. It has been demonstrated that the model reproduces measurements with a single model parameter set with-

out binning option well for any device sizes fabricated with a 90 nm MOSFET technologies.

With the proposed model, the influence of the GIDL current on circuit performance has been investigated. The results show strong influence for the resistor load inverter circuit and the differential amplifier circuit fabricated with a 0.18 um MOSFET technology. This concludes the importance of the accurate GIDL current model for predicting accurate circuit performance.

Acknowledgments This work is supported by collaborative development with Santa Clara University in United States. We would like to greatly thank Q. Ngo and C.Y. Yang from Santa Clara University in United States.

References

1) Inagaki, R., Sadachika, N., Navarro, D., Miura-Mattausch, M. and Inoue, Y.: A Gate-Current Model for Advanced MOSFET Technologies Implemented into HiSIM2, *IEEJ Trans.*, pp.64–71 (Mar. 2008).
2) Yang, W., Qin, G., Shao, X., Yu, Z. and Tian, L.: Analysis of GIDL Dependence on STI-induced Mechanical Stress, Institute of Microelectronics, Tsinghua University, *IEEE Electron Devices and Solid-State Circuits*, pp.769–772 (Dec. 2005).
3) Sze, S.M.: *Physics of Semiconductor Devices*, 2nd ed., New York: Wiley (1981).
4) *BSIM4.2.1 MOSFET Model — User's Manual*. Department of Electrical Engineering and Computer Science, University of California, Berkeley CA (2001).
5) Chakrabarti, P., Gawarikar, A., Mehta, V. and Garg, D.: Effect of Trap-assisted Tunneling (TAT) on the Performance of Homojunction Mid-Infrared Photodetectors based on InAsSb, *Journal of Microwaves and Optoelectronics*, Vol.5, No.1 (Jun. 2006).
6) *HiSIM2.4.0 — User's Manual*, Hiroshima University & STARC (2007).
7) *BSIM3v3 MOSFET Model — User's manual*, University of California, Berkeley CA (2005).
8) *BSIM4.6.1 MOSFET Model — User's Manual*, University of California, Berkeley CA (2007).
9) *PSP Model — User's Manual*, The Pennsylvania University and Philips Research (2005).
10) *PSP102.1 Model — User's Manual*, The Arizona State University and NXP Research (2006).
11) *HiSIM1.2.0 — User's Manual*, Hiroshima University & STARC (2003).
12) Inagaki, R., Miura-Mattausch, M. and Inoue, Y.: A GIDL-Current Model for Advanced MOSFET Technologies Implemented into HiSIM2, *International Conference on Communications, Circuits and Systems, 2007, ICCCAS 2007*, pp.1057–1061 (July 2007).
13) Chen, T.Y., Chen, J., Ko, P.K. and Hu, C.: The impact of gate-induced drain leakage current on MOSFET scaling, *Tech. Digest of IEDM*, pp.718–721 (1987).
14) Parke, S.A., Moon, E., Wenn, H-J., Ko, P.K. and Hu, C.: Design for suppression of gate-induced drain leakage in LDD MOSFETs using a quasi 2D analytical model, *IEEE Trans. Electron Devices*, Vol.39, No.7, pp.1694–1703 (1992).
15) *BSIM4.0.0 MOSFET Model, Slide*, Department of Electrical Engineering and Computer Science, University of California, Berkeley CA (2000).
16) Pao, H.C. and Sah, C.T.: Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors, *Solid-State Electron.*, Vol.9, pp.927–937 (Oct. 1966).
17) Nakazato, K.: The lecture of Information device engineering (2), Department of Electrical Engineering and Computer Science, Graduate School of Engineering, Nagoya University, Japan, p.12 (2005).
18) *MOSFET Modeling BSIM3 USER'S GUIDE*, Yuhua Cheng and Chenming Hu, Kluwer Academic Publishers (1999).
19) *HiSIM2.4.1 — User's Manual*, Hiroshima University & STARC (2008).

(Received May 23, 2008)
(Revised August 22, 2008)
(Accepted October 9, 2008)
(Released February 17, 2009)

(Recommended by Associate Editor: *Kei Hirose*)

Ryosuke Inagaki received the B.E. degree in electronic engineering from Osaka Institute of Technology, Osaka, Japan, in 1987. He is currently working toward the Ph.D. degree at the Graduate School of Information, Production and Systems, Waseda University, Kitakyushu, Japan. From 1987 to 2003, he was with Rohm Corporation, Ltd. Since 2004, he has been a Researcher at Semiconductor Technology Academic Research Center, Yokohama, Japan. In 2005, he was a Visiting Researcher at Hiroshima University, Hiroshima, Japan. His current interests include compact modeling for advanced MOSFET technologies.

Norio Sadachika received the B.S. and M.E. degrees in electrical engineering from Hiroshima University, Hiroshima, Japan, in 2004 and 2006, respectively. He is currently working toward the doctoral degree at the Graduate School of Advanced Sciences of Matter, Hiroshima University. His current interests include compact modeling of silicon-on-insulator MOSFET and double-gate MOSFET.

Dondee Navarro received the B.S. degree in Applied Physics from the University of the Philippines in 1997 and the M.E. and Ph.D. degrees in engineering from Hiroshima University, Japan, in 2004 and 2006, respectively. From 1997 to 2001, he was an Assistant Instructor at the Ateneo de Manila University. In 1999, he was involved in the development of logic TEG devices at Hitachi Musashi, Japan. He is now an engineer working on device model development at Silvaco Japan.

Mitiko Miura-Mattausch received the Dr.Sc. degree from Hiroshima University, Hiroshima, Japan. From 1981 to 1984, she was a Researcher at the Max-Planck Institute for Solid-State Physics, Stuttgart, Germany. From 1984 to 1996, she was with the Corporate Research and Development, Siemens AG, Munich, Germany. Since 1996, she has been a Professor at the Department of Electrical Engineering, Graduate School of Advanced Sciences of Matter, Hiroshima University, where she leads the Ultra Scaled Devices Laboratory.

Yasuaki Inoue received D.E. degree in electronics and communication engineering from Waseda University, Tokyo, Japan, in 1996. From 1964 to 2000, he was with Sanyo Electric Co., Ltd. Gunma, Japan. From 2000 to 2003, he was a Professor with the Graduate School of Integrated Science and Art, University of East Asia, Shimonoseki, Japan. Since 2003, he has been a Professor with the Graduate School of Information, Production and Systems, Waseda University, Kitakyushu, Japan.