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# **Regular Paper**

# A Calibration Technique for DVMC with Delay Time Controllable Inverter

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**Abstract:** This paper presents a novel calibration method for Delay Value Measurement Circuit (DVMC), a class of embedded time to digital converter (TDC), using a variable clock generator for accurate delay measurement. The proposed method uses a design for calibration as well as a variable clock generator. The design utilizes a delay time controllable (DTC) inverter. It also uses two OR-NAND gates which work as selectors; we reconfigure the construction of the ring oscillator (RO) in DVMC when calibrating the DTC inverter. The proposed scheme accomplishes more accurate calibration compared to the traditional calibration which only uses the variable clock generator. For example, when using a variable clock generator with the resolution of 5.2 ps, the resolution of the proposed method is 0.58 ps while the traditional method is 5.2 ps.

*Keywords:* TDC (Time-to-Digital Converter), DVMC (Delay Value Measurement Circuit), calibration, variable clock generator, process variation, delay time controllable inverter

# 1. Introduction

With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. Operating frequency of integrated circuit will come into multi-gigahertz domain. However, the recent high density technology brings about delay defects caused by manufacturing defects such as resistive opens and shorts [1]. In particular, small-delay defects, the defect size of which is not large enough to cause a timing failure under the system clock cycle, have become a significant issue. For example, small-delay defects caused by a resistive open caused by a minimally connecting via can become a complete open in operation due to metal migration.

Embedded time to digital converter (TDC) is very useful to detect delay defects. There are many kinds of TDC architecture. Single delay chain architecture TDCs were proposed in Refs. [2], [3], [4], time resolution of measurement in this method related to inverter delay on delay chain. Vernier delay line based TDCs were proposed in Refs. [5], [6], [7], [8], [9]; this method improves the time resolution by using two delay lines with different inverter delays. Tanabe et al. presented a novel embedded TDC, called Delay Value Measurement Circuit (DVMC) [2]. However, embedded TDCs, including DVMC, do not make an accurate measurement without calibration because process variation changes the delay time of delay elements in the embedded TDCs. So, we need to calibrate the embedded TDC calibration schemes were presented [10], [11], [12], [13], [14]. We can cal-

ibrate TDCs by measuring the delay time of the delay elements in the embedded TDCs. A TDC calibration normally uses a variable clock generator. However its resolution is low due to the low resolution of the variable clock generator.

This paper presents a novel calibration for DVMC. The proposed calibration uses a design for calibration as well as a variable clock generator to achieve calibration with high resolution. The proposed design utilizes delay time controllable (DTC) inverter.

The rest of the paper is organized as follows: Section 2 explains the preliminaries. Section 3 describes the detail of the proposed calibration technique. Section 4 is evaluation of proposed method. Finally Section 5 presents the summary and the conclusion.

## 2. Preliminaries

#### 2.1 DVMC (Delay Value Measurement Circuit)

**Figure 1** shows the construction of the DVMC [2], which consists of a ring oscillator (RO), scan flip-flops (FFs) and a transition counter (TRC); the RO consists of inverters and a NAND gate, which work as delay elements. The DVMC has two inputs, *start* and *stop*, and measures a time interval between transitions of the two inputs.

Measurement is performed as follows: First, the transition on *start* triggers the oscillation on the RO. The TRC counts up the oscillation. When occurring the transition on *stop*, the scan FFs capture the output value of the RO. Finally, the time interval between the transitions is calculated from the captured value and TRC [2].

Tanabe et al. [2] gives the following equation to calculate the time interval  $\Delta T$  between transition of *start* and *stop* signals:

$$\Delta T = \{T_n(M-1) + T_a\}N + T_n(m-1) + T_a$$
(1)

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Fig. 2 Outline of direct calibration.

where  $T_n$  and  $T_a$  are the delay time of an inverter and a NAND gate, M is the number of delay elements in the RO (i.e., the inverters and NAND gate), N is the value of TRC and m is the number of gates in which signal transition arrives in the final cycle of the DVMC measurement, (i.e., after the final change of TRC). This lacks precision as explained in Section 3.3.

## 2.2 Related Works

Process variation on the RO affects measurement results. So, we need to calibrate TDC before we use and mitigate the effect of this variation; several calibration techniques have been studied by many researchers [10], [11], [12], [13], [14].

A self-calibration was proposed in Refs. [10], [11]. This method mitigates bubble errors, which frequently occur near rising edge of *stop* signal due to setup and hold time violation at FFs. Furthermore, this method tolerates nonlinearity characteristics which TDCs have due to delay-time variation at delay buffers. However the resolution of this calibration depends on that of the variable clock generator, which is low.

An indirect calibration was proposed in Ref. [12]. This method uses two square waves with different frequencies of  $f_1$  and  $f_2$ ; these signal waves are input to every two FFs. The result of ANDoperation of the outputs of the two FFs are a square wave with a frequencies of  $f_p = \Delta_{12}f_1f_2$ , where  $\Delta_{12}$  is the offset difference value of the two FFs. The value  $\Delta_{12}$  is the objective value of this method, and can be calculated from  $f_p$ ,  $f_1$  and  $f_2$ . This method requires reference signals with very low jitter for accurate calibration; so it is not practical.

Figure 2 illustrates direct calibration. Two transitions with the

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time interval of  $\Delta T$  are generated at variable clock generator and input to the TDC under measurement. It is assumed that the clock generator has calibrated before TDC calibration; it is guaranteed that  $\Delta T$  is accurate. Direct calibration utilizes a variable clock generator, which supplies time interval sequences to TDC. The resolution of the calibration depends on that of the variable clock generator. However the resolution is low for the TDC calibration.

Levine et al. presented a class of direct calibration [13], [14]. In this method, a temporal noise is added to the arbiter input artificial; the noise is physically created by programming a timing generator. Unlike indirect calibration, it does not need inputs with very low jitter. However, it requires an on-chip noise source with a relatively large standard deviation, which is hard to be implemented.

## 3. Proposed Calibration

This section explains the proposed calibration. The proposed method is a class of direct calibration, and accomplishes more accurate calibration compared to the traditional calibration which only uses the variable clock generator. The proposed calibration utilizes a design for calibration as well as a variable clock generator; the proposed design uses a DTC inverter. Section 3.1 explains the DTC inverter. Section 3.2 presents a construction of DVMC with the proposed design. Section 3.3 explains measurement on the proposed design. Equation (1) lacks precision; Section 3.4 presents the proposed calibration. Finally Section 3.5 discusses the errors in clock and voltage generators.

## 3.1 DTC Inverter

Figure 3 shows the construction of the DTC inverter. In the DTC inverter, PMOS and NMOS transistors are inserted between original transistors and the voltage sources  $V_{dd}$  and ground; we can control the delay time of the inverter by changing the gate bias voltage of the inserted transistors ( $V_{biasp}$  and  $V_{biasn}$ ) [15].

The delay time is controllable with higher resolution than the



Fig. 3 Delay time controlable (DTC) inverter.

variable clock generator. **Figure 4** shows HSPICE simulation results using PTM 22 nm process technology [16] ( $V_{dd} = 1$  V). The delay time of the DTC inverter changes depending on the bias voltage. In Fig. 4 (a), a falling transition is input to the DTC inverter.  $V_{biasp}$  changes from 0 to 0.5 V.  $V_{biasn}$  is constantly set to 1 V. The delay time changes from 8.2 ps to 28.0 ps depending on the bias voltage. In Fig. 4 (b), a rising transition is input.  $V_{biasn}$  changes from 1 to 0.5 V.  $V_{biasp}$  is set to 0 V. The delay time increases from 12.7 ps to 47.4 ps.

#### 3.2 Proposed Schematic of DVMC

**Figure 5** shows the construction of the proposed DVMC. Similar to the traditional DVMC (shown in Fig. 1), the proposed DVMC consists of a RO, scan FFs and a TRC. The TRC counts the transition at the output of the RO, and TRC construction is the same as the traditional on shown in Fig. 1. The RO of the proposed DVMC differs from that of the traditional one. The oscillator in the traditional DVMC consists of a NAND gate and multiple inverters. In contrast, the proposed oscillator consists of a DTC inverter and two OR-NAND gates as well as multiple inverters. The OR-NAND gates work as selectors, the DVMC is configured according to the value of the control signal *ctrl* as shown in **Fig. 6**. The loop in the RO includes the DTC inverter when *ctrl* is low (called as *full-loop mode*); it does not when *ctrl* is high (called as *measurement mode*).

## 3.3 Measurement on Proposed DVMC

Measurement is done by a similar manner to the original



(b) changing bias voltage on NMOS





DVMC [2]. The control signal *ctrl* is set to high during measurement; the DVMC works in the measurement mode. The bias voltages for the DTC inverter are set to  $V_{biasp} = 0$  and  $V_{biasn} = V_{dd}$ .

In the original DVMC, measurement results are given by Eq. (1). However, the proposed method uses the design for cali-

bration; so the equation cannot be applied to the proposed method without modification. In addition, (1) lacks precision as explained below: It is well-known that the rising time of delay element differs from its falling time. Furthermore, the delay time of inverters differ from each other due to process variation. These facts were not considered in Ref. [2].

Here we give equations considering the above matters. Let Mbe the number of delay elements (i.e., OR-NAND gates, a DTC inverter and inverters) in the RO. For example, M = 7 for DVMC shown in Fig. 5. Let  $t_r(i)$  and  $t_f(i)$  be the delay time of the *i*th delay element  $(0 \le i < M)$  for rising and falling transitions respectively. Every OR-NAND gate has three inputs; the delay time for every input differs from each other. The control signal ctrl keeps high during measurement; so we do not consider the delay time from the control inputs of the OR-NAND gates. We need to consider other two inputs. Let  $t_r(i)$  and  $t_f(i)$  be the delay time from the input of OR gate (called as feedback input) and  $\overline{t_r}(i)$ and  $\overline{t_f}(i)$  be the delay time from the input of NAND gate (called as regular input) for i = 0, 2. The delay time of the DTC inverter changes depending on the bias voltage. Let  $t_r(1)$  and  $t_f(1)$  be the delay time of the DTC inverter for  $V_{biasp} = 0$  and  $V_{biasn} = V_{dd}$ . Let  $T_r(m)$  and  $T_f(m)$  be the delay time from the feedback input of the second delay element (i.e., the right OR-NAND gate) to the output of the *m*-th delay element for rising and falling transitions at the OR-NAND gate; they are given by:

$$T_r(m) = \sum_{i=1}^{\lfloor \frac{m}{2} \rfloor} t_r(2i) + \sum_{i=2}^{\lceil \frac{m}{2} \rceil} t_f(2i-1)$$
$$T_f(m) = \sum_{i=1}^{\lfloor \frac{m}{2} \rfloor} t_f(2i) + \sum_{i=2}^{\lceil \frac{m}{2} \rceil} t_r(2i-1)$$

where  $\lfloor x \rfloor$  and  $\lceil x \rceil$  are the floor and ceiling functions. Let *N* be the value of TRC and *m* be the number of gates which *start* signal finally arrives in the final cycle of DVMC measurement. When a rising transition occurs at the zeroth delay element (i.e., the left OR-NAND gate), the time interval  $\Delta T$  between *start* and *stop* signals is given by:

$$\Delta T = \overline{t_r}(0) + t_f(1) + \overline{t_r}(2) - t_r(2) + T_r(M) \left[\frac{N}{2}\right]$$

$$+ T_f(M) \left[\frac{N}{2}\right] + \begin{cases} T_r(m) & (N \text{ is even}) \\ T_f(m) & (N \text{ is odd}) \end{cases}$$
(2)

When a falling transition occurs at the zeroth delay element,  $\Delta T$  is given by the equation obtained by replacing all suffixes 'r' ('f') with 'f' ('r') in the above equation.

In the proposed measurement procedure the parameters N and *m* are obtained and then  $\Delta T$  is calculated; the remaining values, namely  $t_r(i)$ ,  $t_f(i)$ ,  $\overline{t_r}(i)$  and  $\overline{t_f}(i)$ , are measured in the calibration. The pair (N, m) is called as a measurement result.

#### 3.4 Proposed Calibration

The goal of the proposed calibration is to measure the accurate values of  $t_r(i)$ ,  $t_f(i)$ ,  $\overline{t_r}(i)$  and  $\overline{t_f}(i)$ . To do this, we changes  $t_r(1)$ and  $t_f(1)$  by changing the bias voltage. We can increase  $t_f(1)$  by changing  $V_{biasp}$ . Let  $\Delta t_f(\Delta V)$  be the increment in the delay time of the DTC inverter for  $V_{biasp} = \Delta V$  and  $V_{biasn} = V_{dd}$ ; the delay time of the DTC inverter appears as  $t_f(1) + \Delta t_f(\Delta V)$ . We can increase  $t_r(1)$  by changing  $V_{biasn}$ . Let  $\Delta t_r(\Delta V)$  be the increment in the delay time of the DTC inverter for  $V_{biasn} = V_{dd} - \Delta V$  and  $V_{biasp} = 0.$ 

The proposed method calibrates the DVMC in two steps. 1) First we calibrate the DTC inverter by measuring  $\Delta t_r(\Delta V)$  and  $\Delta t_f(\Delta V)$ . 2) Subsequently, we measure  $t_r(i)$ ,  $t_f(i)$ ,  $\overline{t_r}(i)$  and  $\overline{t_f}(i)$ . Both steps utilize  $\Delta T$  generated by a clock generator. Just like the traditional direct calibration, it is assumed that the clock generator has calibrated before TDC calibration.

#### 3.4.1 Calibration of the DTC Inverter

In the calibration of the DTC inverter, *ctrl* is set to low; the DVMC works in *full-loop mode*. The difference  $\Delta t_r(\Delta V)$  is measured as follows:

Step 1. Set  $V_{biasn} = V_{dd}$  and  $V_{biasp} = 0$ .

Step 2. Find  $\Delta T$  which gives a measurement result for falling transition such that N is even number.

Step 3. Set  $V_{biasn} = V_{dd} - \Delta V$ .

Step 4. Find  $\Delta T'$  which gives the same measurement result for falling transition.

Step 5. Calculate  $\Delta t_r(\Delta V) = \frac{\Delta T' - \Delta T}{\frac{N}{2} + 1}$ . Next, we prove the equation in Step 5. The following equations are true:

$$\begin{split} \Delta T &= \overline{t_f}(0) - t_f(0) + \widetilde{T_f}(M)\frac{N}{2} + \widetilde{T_r}(M)\frac{N}{2} + \widetilde{T_f}(m) \\ \Delta T' &= \overline{t_f}(0) - t_f(0) + \{\widetilde{T_f}(M) + \Delta t_r(\Delta V)\}\frac{N}{2} \\ &+ \widetilde{T_r}(M)\frac{N}{2} + \{\widetilde{T_f}(m) + \Delta t_r(\Delta V)\} \end{split}$$

where  $\widetilde{T}_{r}(m)$  and  $\widetilde{T}_{f}(m)$  be the delay time from the feedback input of the zeroth delay element (the left OR-NAND gate) to the output of the *m*-th delay element for rising and falling transitions at the OR-NAND gate. From these, it is true that  $\Delta T' - \Delta T =$  $\Delta t_r(\Delta V)(\frac{N}{2}+1)$ , so the equation in Step 5 is true.

We can measure the difference  $\Delta t_f(\Delta V)$  in a similar manner, in which  $V_{biasp}$  changes instead of  $V_{biasn}$ .

The resolution of the DTC inverter depends on N; we can roughly estimate that the resolution is  $(\frac{N}{2} + 1)$  times as high as that of the variable clock generator (which generates the differences  $\Delta T$  and  $\Delta T'$ ). Thus larger number of N provides better resolution. However, this is not always correct because we cannot generate any discrete bias voltages  $\Delta t_r(\Delta V)$  and  $\Delta t_f(\Delta V)$ ; the generatable voltage depends on the resolution of the bias voltage generator. The recent generator has enough high resolution for the proposed scheme; this is discussed using experimental results in Section 4.

#### 3.4.2 Measurement of Delay Time of Every Delay Element

Next, we measures the delay time of delay elements in the RO. In this measurement, ctrl is set to high; the DVMC works in measurement mode. The delay time  $t_r(i)$  (i > 1, i is even) is measured as follows:

Step 1. Set  $V_{biasn} = V_{dd}$  and  $V_{biasp} = 0$ .

Step 2. Find  $\Delta T$  which gives a measurement result such that N is even number and m = i.

Step 3. Increase  $V_{biasp}$  until m = i - 1; let  $\Delta V$  be the ultimate value of V<sub>biasp</sub>.

Step 4. Set  $V_{biasp} = 0$ .



Fig. 7 Timing chart of proposed calibration.

Step 5. Find  $\Delta T'$  which gives a measurement result such that *N* is the same as the above and m = i + 1.

Step 6. Increase  $V_{biasp}$  until m = i; let  $\Delta V'$  be the ultimate value of  $V_{biasp}$ .

Step 7. Calculate  $t_r(i) = \{\Delta T' - \Delta t_f(\Delta V')\} - \{\Delta T - \Delta t_f(\Delta V)\}$ . The delay times  $t_r(i)$  (i > 1, i is odd) and  $t_f(i)$  are measured in a similar manner.

Next, we prove the equation in Step 7. The following equations are true:

$$\begin{split} \Delta T &= \overline{t_r}(0) + t_f(1) + \Delta t_f(\Delta V) + \overline{t_r}(2) - t_r(2) \\ &+ T_r(M)\frac{N}{2} + T_f(M)\frac{N}{2} + T_r(i-1) \\ \Delta T' &= \overline{t_r}(0) + t_f(1) + \Delta t_f(\Delta V') + \overline{t_r}(2) - t_r(2) \\ &+ T_r(M)\frac{N}{2} + T_f(M)\frac{N}{2} + T_r(i) \end{split}$$

From these it is true that

$$\Delta T' - \Delta T = \Delta t_f(\Delta V') - \Delta t_f(\Delta V) + t_r(i)$$

Thus the equation in Step 7 is true.

This algorithm gives any delay time in Eq. (2) except  $\overline{t_r}(0)$ ,  $t_f(1)$  and  $\overline{t_r}(2)$ . These three times are not measured precisely in the proposed calibration. Instead, the sum  $\overline{t_r}(0) + t_f(1) + \overline{t_r}(2)$  are precisely measured; this is enough to calculate  $\Delta T$  using Eq. (2) as long as  $\Delta T$  are not shorter than  $\overline{t_r}(0) + t_f(1) + \overline{t_r}(2)$ .

Step 1. Measure any  $\Delta T$ .

Step 2. Calculate  $\overline{t_r}(0) + t_f(1) + \overline{t_r}(2)$  using the following equation:

$$\overline{t_r}(0) + t_f(1) + \overline{t_r}(2) = \Delta T + t_r(2) - T_r(M) \left\lceil \frac{N}{2} \right\rceil$$
$$- T_f(M) \left\lfloor \frac{N}{2} \right\rfloor - \begin{cases} T_r(m) & (N \text{ is even}) \\ T_f(m) & (N \text{ is odd}) \end{cases}$$

This equation is equivalent to Eq. (2).

**Figure 7** shows an example timing chart to illustrate the merit of the proposed calibration. In this example,  $\overline{t_r}(0) + t_f(1) + \overline{t_r}(2) + t_f(3)$  is measured. Because the resolution of variable clock generator is low, generatable *stop* signals are limited. As the result the traditional calibration can bring about a significant error. In contrast, the proposed calibration achieves little error by extending the delay time of the DTC inverter; this means the proposed method obtains  $\overline{t_r}(0) + t_f(1) + \overline{t_r}(2) + t_f(3)$  with high accuracy bringing in the calibration with high resolution.

#### 3.5 Errors in Clock and Voltage Generators

We discuss the errors in the external clock generator. The proposed calibration method is a class of direct calibration methods [13], [14]. All methods in this class use the external clock generator; so they (i.e., both proposed and traditional methods) can be equally affected by the errors in the external clock generator.

Next we discuss the errors from the bias voltage generator. Process variation can impact the accuracy of voltage generator; however it does not affect the accuracy of calibration results. This is because we need not to obtain an accurate bias voltage of DTC inverter; we need only the accurate delay time of the DTC inverter for every expected output voltage of the bias voltage generator. The accurate delay time can be measured in the calibration of the DTC inverter shown in Section 3.4.1. In other words, the calibration of the DTC inverter calibrates not only the DTC inverter but also the bias voltage generator.

In summary, the superiority of the proposed calibration is unchallenged even when considering the errors in the clock and bias voltage generators.

## 4. Evaluation

#### 4.1 Resolution

We experimentally confirmed that the proposed calibration properly works with HSPICE simulation. This simulation uses netlist designed in the PTM 22 nm process technology; parasitic capacitance and resistance are not considered in the netlist design. We applied the proposed calibration on the DVMC for M = 7. The clock generator of Ref. [17] was used; the clock period can be set every 5.2 ps from 500 ps to 1,000 ps. We used an on-chip tunable wide ranged multiple output voltage reference circuit [18] to generate the bias voltage of  $V_{biasp}$  and  $V_{biasn}$  for the DTC inverter; the generator of Ref. [18] can generate bias voltages with 13-bit resolution [19]. In the calibration of the DTC inverter, the maximal value N is 16.

First we assume that we can generate arbitrary bias voltages; the resolution of the proposed calibration of the DVMC is given by  $\Delta t_r (\Delta V) = (\Delta T' - \Delta T)/(\frac{N}{2} + 1) = 5.2/(\frac{16}{2} + 1) = 0.58$  ps. **Table 1** summarizes the resolution comparison between the proposed and traditional calibration; the proposed calibration accomplishes higher resolution.

While it was assumed that we can generate arbitrary bias voltages, real voltage generator is capable of generating only limited



Fig. 9 Layout of proposed DVMC.

 Table 1
 Calibration resolution comparison between proposed and traditional methods.

|                    | resolution of calibration |
|--------------------|---------------------------|
| traditional method | 5.20 ps                   |
| proposed method    | 0.58 ps                   |

| Table 2 | Relationship | between | $\Delta t_r(\Delta V)$ | and $\Delta V$ | ٢. |
|---------|--------------|---------|------------------------|----------------|----|
|---------|--------------|---------|------------------------|----------------|----|

| -                           |                |
|-----------------------------|----------------|
| $\Delta t_r(\Delta V)$ (ps) | $\Delta V (V)$ |
| 0.58                        | 0.14           |
| 1.16                        | 0.19           |
| 1.73                        | 0.22           |
| 2.31                        | 0.25           |
| 2.89                        | 0.27           |
| 3.47                        | 0.28           |
| 4.04                        | 0.30           |
| 4.62                        | 0.31           |
| 5.20                        | 0.32           |
|                             |                |

| Table 3 | Relationship | between 2 | $\Delta t_f(\Delta V)$ | and $\Delta V$ . |
|---------|--------------|-----------|------------------------|------------------|
|---------|--------------|-----------|------------------------|------------------|

| $\Delta t_f(\Delta V)$ (ps) | $\Delta V(V)$ |
|-----------------------------|---------------|
| 0.58                        | 0.15          |
| 1.16                        | 0.20          |
| 1.73                        | 0.24          |
| 2.31                        | 0.28          |
| 2.89                        | 0.30          |
| 3.47                        | 0.32          |
| 4.04                        | 0.34          |
| 4.62                        | 0.35          |
| 5.20                        | 0.37          |

and discrete voltage. For example an on-chip tunable wide ranged multiple output voltage reference circuit of Ref. [18] generates voltages with 13-bit resolution [19].

**Tables 2** and **3** show the voltage increment  $\Delta V$  required to increase the delay time of the DTC inverter by  $\Delta t_r(\Delta V)$  and  $\Delta t_f(\Delta V)$ , which is set from 0.58 ps to 5.20 ps every 0.58 ps; these values are generated as follows:  $\Delta V$  is set from 0.01 V to 0.50 V every 0.01 V; for every  $\Delta V$  we performed the calibration of the DTC inverter shown in Section 3.4.1. We used HSPICE simulation in Steps 2 and 4. Tables 2 and 3 show the minimum values of  $\Delta V$  in which  $\Delta t_r(\Delta V)$  is equal to the value of the left column in the Tables. We can regard that a voltage generator has enough high resolution if it can generate all voltages in the Tables. The voltages shown in the Tables can be generated by using a voltage generator with 6-bit resolution or higher, which the voltage



Fig. 8 Area overhead comparison between proposed and traditional methods.

generator of Ref. [18] meets with a large margin. In summary, the comparison shown in Table 1 is valid even when considering practical voltage generator.

#### 4.2 Area Overhead

Next, we compare the area of the proposed DVMC with the design for calibration to the traditional DVMC without design for calibration [2]. The difference between the traditional and proposed DVMC is the construction of RO and the number of scan FFs. In addition, the proposed DVMC requires a bias voltage generator. The number of transistors in the traditional DVMC with M - 2 delay elements is 26M + 54K - 36, where K is the number of TFFs in TRC. In contrast that in the proposed DVMC with M delay elements is 26M + 54K + 78 which includes 26 transistors for bias voltage generators; we used the voltage generator shown in Ref. [18]. So, it is conclude that the proposed DVMC.

**Figure 8** shows area comparison of the proposed DVMC with M delay elements and the traditional DVMC with M - 2 delay elements for K = 6. We designed the layout with Cadence Virtuoso in an industrial 180 nm technology; **Fig. 9** shows a sample layout of the proposed DVMC with M = 7 and K = 3.

# 5. Conclusion

This paper presented a calibration method for DVMC. The

proposed method uses a design for calibration as well as a variable clock generator; the design uses a delay time controllable (DTC) inverter. Furthermore, the design uses two OR-NAND gates which work as selectors; the construction of the DVMC changes in calibration of the DTC inverter. The proposed method accomplishes an accurate calibration. For example, when using a variable clock generator of Ref. [17] with the resolution of 5.2 ps, the resolution of the proposed method is 0.58 ps while the traditional method is 5.2 ps.

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