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Short Paper

Supplemental PDK for ASAP7 Using Synopsys Flow

Shinichi Nishizawa[1,a)] Shih-Ting Lin[2] Yih-Lang Li[2] Hidetoshi Onodera[3]

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Abstract: This paper reports a supplemental process design kit (PDK) for ASAP7 PDK using Synopsys design flow. ASAP7 is a PDK for "predictable" 7-nm FinFET technology node. ASAP7 PDK is useful for academical and educational purpose, however it only supports Cadence platform for Place and Route. A supplemental PDK is designed for ASAP7 to use Synopsys platform for Place and Route. This PDK is opened at the author's GitHub site for both acamemical and educational usage.

Keywords: process design kit, ASAP7

1. Introduction

Technology scaling has been dramatically increased, and it improves power, performance and area of VLSI chips. Recently, 7-nm FinFET technology is widely used for high-performance processors and System-On-Chips. Today's recent state-of-the-art process, such as a 7-nm technology node, uses many "new" technologies to improve its performance and density of VLSI chips. FinFET is now a common structure for CMOS transistors. Middle-Of-Line (MOL) was introduced to connect Front-End-Of-Line and Back-End-Of-Line (BEOL) layers. Local interconnect layer in MOL and BEOL uses EUV lithography to improve its routeability and density. The semi-global interconnect layer, on the other hand, uses 193i Self-Aliened-Double-Patterning (SADP) to balance both fabrication cost and density. It is very important to learn the characteristics of FinFET process before the start of a circuit design, since it has many differences from ordinal planer process. The use of "real" process design kit (PDK) is very expensive and hard to get permission to access. Thus, "predictable" PDK is very important for both VLSI education and research.

ASAP7 is one of a "predictable" PDK for 7-nm technology node, provided by Arizona State University collaborated with ARM Ltd. [1]. It includes both custom design flow and automated digital design flow, so it is very useful to learn these design flows in state-if-the-art FinFET process. However, they only provide technology files for Cadence Innovus for place-and-route (P&R). Innovus is one major P&R EDA, however, Synopsys IC Compiler is also another major P&R tool.

This paper reports the supplemental PDK of ASAP7 using IC Compiler for P&R. This supplemental PDK includes technology file for Synopsys StarRC to enable parasitic-aware P&R. This supplemental PDK is designed to add a second choice of P&R tool to learn VLSI chip design.

The rest of this paper is organized as follows. Section 2 describes the overview of ASAP7 PDK. Section 3 describes the detail of technology file design and library design for the supplemental PDK. Section 4 concludes this paper.

2. Overview of ASAP7 PDK

This section describes the design framework of original ASAP7 PDK and our supplemental PDK. ASAP7 PDK supports both custom design and automated design using P&R tool. Cadence Virtuoso is used for custom design, and Mentor Graphics Calibre is used for verification. Cadence Innovus and QRC are used for parasitic-aware P&R.

Cadence Innovus is one major P&R tool. Synopsys IC Compiler is another major P&R in both industry and academia. We design the technology fies for IC Compiler for ASAP7 environment. **Figure 1** shows the design flow using Cadence tool-chain pro-

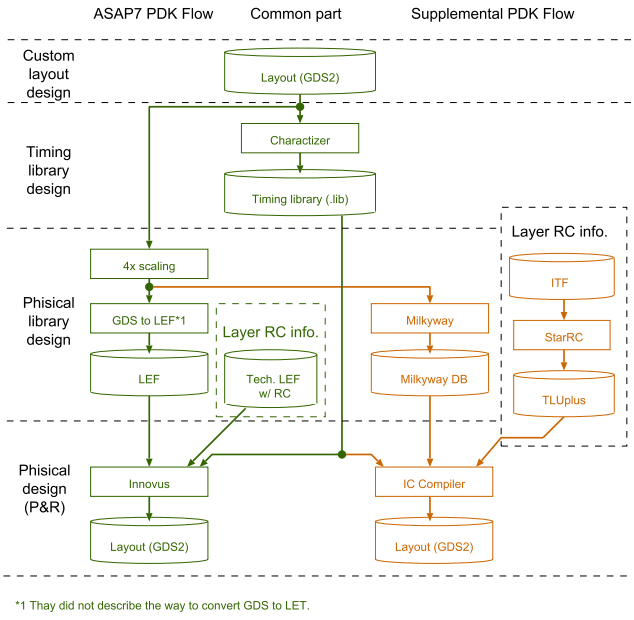

Fig. 1 Design flows of ASAP7 PDK and proposed supplemental PDK.

1 Fukuoka University, Fukuoka 814–0180, Japan
2 National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan
3 Osaka Gakuin University, Suita, Osaka 564–8511, Japan
a) nishizawa@fukuoka-u.ac.jp

vided by ASAP7 PDK, and Synopsys tool-chain provided by this paper. Several technology files are designed to support IC Compiler. TLUplus file is required to perform parasitic-aware P&R in IC Compiler. It is converted from Interconnect Technology File (ITF) designed by hand and converted with Synopsys StarRC. Designed ITF uses same cross section of ASAP7, as reported in Ref. [2]. It assumes Copper interconnect and 2 : 1 aspect ratio for metal and vias. ITF can be used to create nextgd file, which is used in RC extraction using StarRC.

3. Technology File Design and Library Design

Following files are designed for IC Compiler.

GDS2A Layer conversion table from GDS2 to Synopsys Milkyway.

A2GDS Layer conversion table from Milkyway to GDS2.

ITF Interconnect information including the dimensions (thickness, width, spacing of each layer) and electrical properties (resistances and dielectrics).

TLUplus Interconnect information for parasitic-aware P&R. Compiled from ITF using StarRC.

techfile Technology file for IC Compiler including interconnect width, spaces, routing directions and restrictions. VIA macros are defined to connect different routing layer.

3.1 Timing Library Design

The timing library of standard cells is generated with 7-nm design rule. Both PDKs have same design framework for timing library design. Netlist of standard cells is extracted from RC extraction and characterized using commercial characterization tool. Cell level timing information and power consumption are evaluated assuming 7-nm technology node. This characterization can be used for both dynamic timing simulation and static timing analysis for digital circuits.

3.2 Physical Library Design and P&R

Physical library of standard cells is generated with 4× scaled design rule. Both Innovus and IC Compiler requires "advanced node license" to handle P&R for advanced technology nodes. To avoid this license problem, ASAP7 assumes 4× scaling in P&R with Innovus. All feature sizes look like 28-nm technology, circuits are designed without using "advanced node license". In our work, designed technology file designed for IC Compiler also assumes all of the layouts are scaled by 4. For physical library design, firstly, standard cells are designed with 7-nm design rule. Secondly, cell layouts are scaled by 4 and converted to physical library for P&R with Milkyway. After the P&R, GDS of the block level design is scaled by 1/4 and used for performance evaluation such as spice level evaluation.

Baseline technology file for IC compiler is converted from provided LEF file using Milkyway. In ASAP7, they assume EUV for Metal-1 to Metal-3, SADP for Metal-4 to Metal-7, and single exposure (SE) for Metal-8 to above. Thus, Metal-4 to Metal-7 has strong restriction for routing direction, metal shape, off-grid and off-track routing. Settings for these restrictions are manually added to the technology file, and these settings are summarized in **Table 1**.

Table 1 Restrictions for routing.

Layer	Patterning	Direction	Off-grid	Bending
Metal 1	EUV	Any	OK	OK
Metal 2	EUV	Any	OK	OK
Metal 3	EUV	Any	OK	OK
Metal 4	SADP	Horizontal	NG	NG
Metal 5	SADP	Vertical	NG	NG
Metal 6	SADP	Horizontal	NG	NG
Metal 7	SADP	Vertical	NG	NG
Metal 8	SE	Horizontal	OK	OK
Metal 9	SE	Vertical	OK	OK
PAD	SE	Horizontal	OK	OK

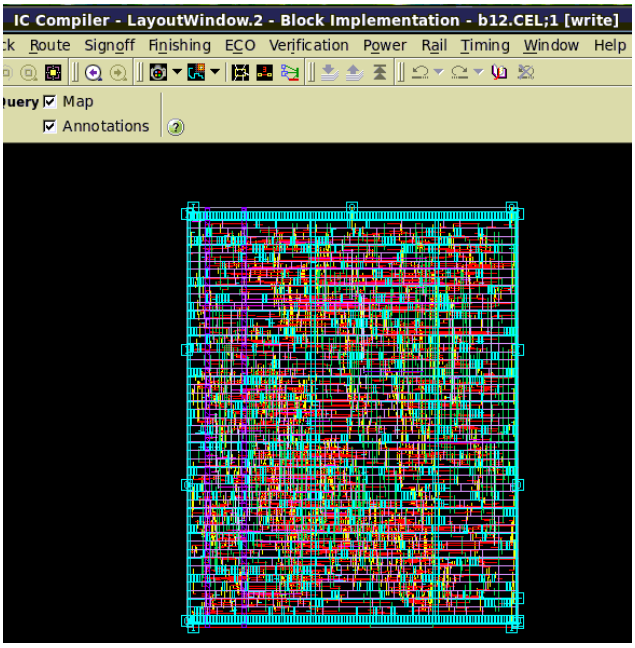

Fig. 2 Layout of b11 circuit by IC Compiler.

Figure 2 shows a design example of b12 circuit from IWLS benchmark [3], without any DRC error and LVS error.

Technology files are available for academic and educational purpose at the author's GitHub site. https://github.com/snishizawa/asap7_snps

4. Conclusion

In this paper, supplemental PDK for ASAP7 has been proposed. This PDK enables to use Synopsys IC Compiler for circuit design in ASAP7 environment. Combining both ASAP7 original PDK and this supplemental PDK, designer can train both Cadence environment and Synopsys environment for "predictable" 7-nm FinFET technology design. We hope this supplemental PDK increase the value of ASAP7 PDK, and contribute to both VLSI education and research.

Our future work is to design technology files and establish a design flow for IC Compiler II.

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References

[1] Clark, L.T., Vashishtha, V., Shifren, L., Gujja, A., Sinha, S., Cline, B., Ramamurthy, C. and Yeric, G.: ASAP7: A 7-nm finFET predictive process design kit, *Microelectronics Journal*, Vol.53, pp.105–115 (2016).

[2] Vashishtha, V., Dosi, A., Masand, L. and Clark, L.T.: Design technology co-optimization of back end of line design rules for a 7 nm predictive process design kit, *International Symposium on Quality Electronic Design*, pp.149–154 (2017).

[3] Albrecht, C.: IWLS 2005 Benchmarks, *International Workshop on Logic and Synthesis* (2005), available from ⟨http://iwls.org/iwls2005/benchmarks.html⟩.

Shinichi Nishizawa received his B.E. degree from Ritsumeikan University, Shiga, Japan, and Ph.D. in Informatics degree from Kyoto University, Kyoto, Japan. He is a Research Associate in Fukuoka University.

Shih-Ting Lin received his B.S. degrees in computer science from NCUE, Taiwan, in 2016. He is currently pursuing the Ph.D. degree from the Institute of Computer Science and Engineering, NYCU. His current research interests include very large-scale integration routing, design for manufacturing, and automatic cell synthesis.

Yih-Lang Li received his B.S. degree in nuclear engineering and his M.S. and Ph.D. degrees in computer science, majoring in designing and implementing a highly parallel cellular automata machine for fault simulation, from the National Tsing Hua University, Hsinchu, Taiwan. In 2003, he joined the Faculty of the Department of Computer Science, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, where he is currently an Associate Professor. From 1995 to 1996 and from 1998 to 2003, he was a Software Engineer and an Associate Manager at Springsoft Corporation, Hsinchu, Taiwan, where he first completed the development of DRC tool for the custom-based layout design, and then established and leaded a routing team for developing a blocklevel shape-based router for custom-based layout design. His current research interests include physical synthesis, parallel architecture, vehicle navigation, and deep learning. He joined the technical committee of the first CAD contest in Taiwan and served as the committee member for 10 years. He was the Contest Chair of the first CAD contest at ICCAD in 2012 and was the Technical Program Committee Member for ASP-DAC, ICCAD and DAC. He was a recipient of the Japan Society for the Promotion of Science Faculty Invitation Fellowship. He has also been serving as the Compensation Committee Member and Independent Director of board of directors for AMICCOM since 2012. He is also a technical member of DATC of IEEE CEDA.

Hidetoshi Onodera received B.S., M.S. and Ph.D. degrees in Electronic Engineering, all from Kyoto University, Kyoto, Japan. He joined the Department of Electronics, Kyoto University, in 1983. He was a Professor in the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University till March 2021. He is currently a Professor in the Faculty of Informatics, Osaka Gakuin University. His research interests include design technologies for Digital, Analog, and RF LSIs, with particular emphasis on low-power design, design for manufacturability, and design for dependability. He served as a Program Chair and a General Chair of ICCAD and ASP-DAC. He was a Chairman of SSCS Kansai Chapter, IEEE CASS Kansai Chapter, IEEE Kansai Section, IPSJ SIG-SLDM (System LSI Design Methodology), and IEICE Technical Group on VLSI Design Technologies. He served as an Editor-in-Chief of IEICE Transactions on Electronics and IPSJ Transactions on System LSI Design methodology. He is an IEEE Fellow, an IEICE Fellow, and a Member of Science Council of Japan.

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