Mismatch and Noise in Modern IC Processes

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ABSTRACT

Component variability, mismatch, and various noise effects are major contributors to design limitations in most modern IC processes. "Mismatch and Noise in Modern IC Processes" examines these related effects and how they affect the building block circuits of modern integrated circuits, from the perspective of a circuit designer.

Variability usually refers to a large scale variation that can occur on a wafer to wafer and lot to lot basis, and over long distances on a wafer. This phenomenon is well understood and the effects of variability are included in most integrated circuit design with the use of corner or statistical component models. Mismatch, which is the emphasis of section I of the book, is a local level of variability that leaves the characteristics of adjacent transistors unmatched. This is of particular concern in certain analog and memory systems, but also has an effect on digital logic schemes, where uncertainty is introduced into delay times, which can reduce margins and introduce 'race' conditions. Noise is a dynamic effect that causes a local mismatch or variability that can vary during operation of a circuit, and is considered in section II. Noise can be the result of atomic effects in devices or circuit interactions, and both of these are discussed in terms of analog and digital circuitry.

KEYWORDS

semiconductors, silicon, integrated circuits, variability, noise, mismatch, analog, digital, SRAM, MuGFET, silicon on insulator, reliability

Preface

Component variability, mismatch, and various noise effects are major contributors to design limitations in most modern integrated circuit (IC) processes. In this book, we take a look at these related effects and how they affect the building block circuits of modern ICs. The term variability usually refers to a large-scale variation that can occur on a wafer-to-wafer and lot-to-lot basis and over long distances on a wafer. Mismatch, which is the emphasis of Part 1, the first seven chapters, is a local level of variability that lives the characteristics of adjacent transistors mismatched. Noise is a dynamic effect that causes a local mismatch or variability that can vary during operation of a circuit and is considered in Chapters 8–12.

Chapter 1 discusses where noise, mismatch and process meet. It also contains a brief review of process and metal oxide semiconductor (MOS) components, discussion of process variability and its affect on leakage; and review of complementary metal oxide semiconductor (CMOS) gates, ring oscillators, and delay chains.

Chapter 2 takes a closer look at mismatch and variability in digital systems with analysis of mismatch effects, race conditions, and statistical modeling and with consideration of interconnect effects.

Chapters 3 and 4 consider mismatch in analog systems including in current mirrors. Cascoding, advanced mirrors mismatch effects, and minimization in current mirrors are scrutinized. Operational amplifiers (op-amps) mismatch effects and minimization in op-amps are discussed, along with circuit-induced mismatch. Memory systems are also considered.

Chapter 5 looks at reliability-induced mismatch from negative bias temperature instability (NBTI) and hot carrier injection (HCI), which are considered in both digital and analog systems.

Chapter 6 discusses nonconventional processes and circuits, in particular, silicon on insulator (SOI) and their impact on variability and mismatch.

Chapter 7 looks in detail at mismatch correction circuits and methods, including body bias, alternating current (AC) op-amps, test-and-fuse for leakage, power reduction, process control, and yield improvement.

Chapter 8 begins the discussion of noise at the component level. System noise, temperature effects, soft error rate (SER), jitter, and noise in digital systems are considered. Gate count impact on noise is also covered.

Chapter 9 considers the impact on noise on digital systems, while Chapter 10 studies noise effects in analog systems.

Chapter 11 takes a look at circuit and component design to minimize noise effects.

Chapter 12 concludes the book with a look at noise in nonconventional processes [SOI, fin-shaped field effect transistor (finFET), and multigate FET (MuGFET)].

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