New Prospects of Integrating Low Substrate Temperatures with Scaling-Sustained Device Architectural Innovation

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Nabil Shovon Ashraf, Shawon Alam, and Mohaiminul Alam
North South University

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ABSTRACT

In order to sustain Moore's Law–based device scaling, principal attention has focused on toward device architectural innovations for improved device performance as per ITRS projections for technology nodes up to 10 nm. Efficient integration of lower substrate temperatures (<300K) to these innovatively configured device structures can enable the industry professionals to keep up with Moore's Law-based scaling curve conforming with ITRS projection of device performance outcome values. In this prospective review E-book, the authors have systematically reviewed the research results based on scaled device architectures, identified key bottlenecks to sustained scaling-based performance, and through original device simulation outcomes of conventional long channel MOSFET extracted the variation profile of threshold voltage as a function of substrate temperature which will be instrumental in reducing subthreshold leakage current in the temperature range 100K–300K. An exploitation methodology to regulate the die temperature to enable the efficient performance of a high-density VLSI circuit is also documented in order to make the lower substrate temperature operation of VLSI circuits and systems on chip process compatible.

KEYWORDS

threshold voltage, substrate temperature, Fermi potential, intrinsic carrier concentration, bulk potential, depletion charge, metal-to-semiconductor work function difference, flat-band voltage, subthreshold leakage current, thin-film microcoolers

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