

Non-Volatile In-Memory Computing by Spintronics

Synthesis Lectures on Emerging Engineering Technologies

Editor

Kris Iniewski, *Redlen Technologies, Inc.*

Non-Volatile In-Memory Computing by Spintronics

Hao Yu, Leibin Ni, and Yuhao Wang

2016

Layout Techniques for MOSFETs

Salvador Pinillos Gimenez

2016

Resistive Random Access Memory (RRAM)

Shimeng Yu

2016

The Digital Revolution

Bob Merritt

2016

Compound Semiconductor Materials and Devices

Zhaojun Liu, Tongde Huang, Qiang Li, Xing Lu, and Xinbo Zou

2016

New Prospects of Integrating Low Substrate Temperatures with Scaling-Sustained Device Architectural Innovation

Nabil Shovon Ashraf, Shawon Alam, and Mohaiminul Alam

2016

Advances in Reflectometric Sensing for Industrial Applications

Andrea Cataldo, Egidio De Benedetto, and Giuseppe Cannazza

2016

Sustaining Moore's Law: Uncertainty Leading to a Certainty of IoT Revolution

Apek Mulay

2015

© Springer Nature Switzerland AG 2022

Reprint of original edition © Morgan & Claypool 2017

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means—electronic, mechanical, photocopy, recording, or any other except for brief quotations in printed reviews, without the prior permission of the publisher.

Non-Volatile In-Memory Computing by Spintronics

Hao Yu, Leibin Ni, and Yuhao Wang

ISBN: 978-3-031-00904-4 paperback

ISBN: 978-3-031-02032-2 ebook

DOI 10.1007/978-3-031-02032-2

A Publication in the Springer series

SYNTHESIS LECTURES ON EMERGING ENGINEERING TECHNOLOGIES

Lecture #8

Series Editor: Kris Iniewski, *Redlen Technologies, Inc.*

Series ISSN

Print 2381-1412 Electronic 2381-1439

Non-Volatile In-Memory Computing by Spintronics

Hao Yu

Nanyang Technological University, Singapore

Leibin Ni

Nanyang Technological University, Singapore

Yuhao Wang

Synopsis, California, USA

*SYNTHESIS LECTURES ON EMERGING ENGINEERING
TECHNOLOGIES #8*

ABSTRACT

Exa-scale computing needs to re-examine the existing hardware platform that can support intensive data-oriented computing. Since the main bottleneck is from memory, we aim to develop an energy-efficient in-memory computing platform in this book. First, the models of spin-transfer torque magnetic tunnel junction and racetrack memory are presented. Next, we show that the spintronics could be a candidate for future data-oriented computing for storage, logic, and interconnect. As a result, by utilizing spintronics, in-memory-based computing has been applied for data encryption and machine learning. The implementations of in-memory AES, Simon cipher, as well as interconnect are explained in details. In addition, in-memory-based machine learning and face recognition are also illustrated in this book.

KEYWORDS

Spintronics, in-memory computing, non-volatile memory, logic-memory integration, data encryption, AES, machine learning, data analytics, hardware accelerator

Contents

Preface	xi
Acknowledgments	xiii
1 Introduction	1
1.1 Memory Wall	1
1.2 Traditional Semiconductor Memory	3
1.2.1 Overview	3
1.2.2 Nano-scale Limitations	9
1.3 Non-volatile Spintronic Memory	13
1.3.1 Basic Magnetization Process	14
1.3.2 Magnetization Damping	14
1.3.3 Spin-transfer Torque	15
1.3.4 Magnetization Dynamics	18
1.3.5 Domain Wall Propagation	20
1.4 Traditional Memory Architecture	21
1.5 Non-volatile In-memory Computing Architecture	25
1.6 References	28
2 Non-volatile Spintronic Device and Circuit	31
2.1 SPICE Formulation with New Nano-scale NVM Devices	31
2.1.1 Traditional Modified Nodal Analysis	32
2.1.2 New MNA with Non-volatile State Variables	33
2.2 STT-MTJ Device and Model	35
2.2.1 STT-MTJ	35
2.2.2 STT-RAM	39
2.2.3 Topological Insulator	40
2.3 Domain Wall Device and Model	50
2.3.1 Magnetization Reversal	51
2.3.2 MTJ Resistance	53
2.3.3 Domain Wall Propagation	53
2.3.4 Circular Domain Wall Nanowire	54

2.4	Spintronic Storage	57
2.4.1	Spintronic Memory	57
2.4.2	Spintronic Readout	57
2.5	Spintronic Logic	61
2.5.1	XOR	61
2.5.2	Adder	63
2.5.3	Multiplier	64
2.5.4	LUT	64
2.6	Spintronic Interconnect	65
2.6.1	Coding-based Interconnect	65
2.6.2	Domain Wall-based Encoder/Decoder	68
2.6.3	Performance Evaluation	72
2.7	References	74
3	In-memory Data Encryption	81
3.1	In-memory Advanced Encryption Standard	81
3.1.1	Fundamental of AES	81
3.1.2	Domain Wall Nanowire-based AES Computing	83
3.1.3	Pipelined AES by Domain Wall Nanowire	92
3.1.4	Performance Evaluation	97
3.2	Domain Wall-based SIMON Block Cipher	102
3.2.1	Fundamental of SIMON Block Cipher	103
3.2.2	Hardware Stages	103
3.2.3	Round Counter	103
3.2.4	Control Signals	105
3.2.5	Key Expansion	105
3.2.6	Encryption	106
3.2.7	Performance Evaluation	106
3.3	References	108
4	In-memory Data Analytics	111
4.1	In-memory Machine Learning	111
4.1.1	Extreme Learning Machine	111
4.1.2	MapReduce-based Matrix Multiplication	112
4.1.3	Domain Wall-based Hardware Mapping	113
4.1.4	Performance Evaluation	116
4.2	In-memory Face Recognition	121

4.2.1	Energy-efficient STT-MRAM with Spare-represented Data	121
4.2.2	QoS-aware Adaptive Current Scaling	129
4.2.3	STT-RAM based Hardware Mapping	131
4.2.4	Performance Evaluation	135
4.3	References	140
Authors' Biographies		143

Preface

The existing memory technologies have critical challenges when scaling at nanoscale due to process variation, leakage current, and I/O access limitations. Recently, there are two research trends attempting to alleviate the memory-wall issues for future big-data storage and processing system.

First, the emerging non-volatile memory technologies, such as spin-transfer torque memory, domain wall nanowire (or racetrack) memory, etc., have shown significantly reduced standby power and increased integration density, as well as close-to DRAM/SRAM access speed. Therefore, they are considered as promising next generation memory for big-data applications.

Second, due to high data-level parallelism in big-data applications, large number of application specific accelerators can be deployed for data processing. However, the I/O bandwidth limitation will still be the bottleneck in such a memory-logic integration approach. Instead, an in-memory computing platform will be highly desired with less dependence on I/Os.

In order to achieve low power and high throughput (or energy efficiency) in big-data computing, one can build an in-memory non-volatile memory (NVM) hardware platform, where both the memory and computing resources are based on NVM devices with instant-switch-on as well as to ultra-low leakage current. Such an architecture can achieve significant power reduction due to the non-volatility. Moreover, one can develop an NVM logic accelerator that can perform domain-specific computations such as data encryption and also data analytics in a logic-in-memory fashion. Compared to conventional memory-logic-integration architectures, the storage data do not need to be loaded into volatile main memory, processed by logic, and written back afterward with significant I/O communication congestion.

In this book, we discuss the following research studies on this regard. First, we introduce a non-volatile in-memory architecture that both data storage and logic computing are inside the memory block. The data storage and logic computing is located in pairs to perform a distributed in-memory computing. We illustrate the NVM-based basic memory and logic components and find significant power reduction. Second, we develop a SPICE-like simulator NVM SPICE, which implements physical models for non-volatile devices in a similar way as the BSIM model for MOSFET. We further develop the data storage and logic computing on spintronic devices. These operations can be deployed for in-memory data encryption and analytics. Moreover, we illustrate how data encryption including advanced encryption standard (AES) and Simon cipher can be implemented in this architecture. Data analytics applications such as machine learning for super-resolution and face recognition are performed on the developed NVM platform as well.

This book provides a state-of-the-art summary for the latest literature on emerging non-volatile spintronic technologies and covers the entire design flow from device, circuit to system perspectives, which is organized into five chapters. Chapter 1 introduces the basics of conven-

tional memory architecture with traditional semiconductor devices as well as the non-volatile in-memory architecture. Chapter 2 details the device characterization for spintronics by non-electrical states and the according storage and logic implementation by spintronics. Chapter 3 explores the in-memory data encryption based on STT-RAM as well as domain wall nanowire. The implementations of in-memory AES, domain wall-based Simon cipher and low power interconnect are explained in detail. Chapter 4 presents the system level architectures with data analytics applications for the emerging non-volatile memory. In-memory machine learning and face recognition are discussed in this chapter. This book assumes that readers have basic knowledge of semiconductor device physics. It will be a good reference for senior undergraduate and graduate students who are performing research on non-volatile memory technologies.

Hao Yu, Leibin Ni, and Yuhao Wang
Singapore
October 2016

Acknowledgments

The authors would like to thank their colleagues at CMOS Emerging Technology Group at Nanyang Technological University: Dr. Wei Fei, Dr. Yang Shang, Dr. Sai Manoj P.D., Mr. Hantao Huang, Mr. Zichuan Liu, Miss. Hang Xu, and Mr. Rai Suleman Khalid. The authors also acknowledge with gratitude discussions with Prof. Guangbin Huang, Prof. Anupam Chattopadhyay, Prof. Chip-hong Chang, Prof. Jianhua Yang, Prof. Kaushik Roy, Prof. Weisheng Zhao, Prof. Dennis Sylvester, Prof. Kevin Cao, Prof. Yuan Xie, Prof. Yiran Chen, Prof. Hai Li, Dr. Tanay Karnik, Dr. Jing Li, Prof. Wei Zhang, Prof. Tony Kim, Prof. Wen-Siang Lew, Prof. Kiat-Seng Yeo, Dr. Rajiv V. Joshi, and Mr. Suman Deb. Their support was invaluable to us during the writing of this book. The relevant research is funded by MOE Tier-2 (MOE2015-T2-2-013) titled “Sparse-represented Non-volatile In-memory Accelerator for Big-Data Analytics” and NRF CRP (NRF-CRP9-2011-01) titled “Magnetic Domain Wall Logic Gate Device,” from Singapore.

Hao Yu, Leibin Ni, and Yuhao Wang
October 2016