

On-Chip Networks

Second Edition

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SYNTHESIS LECTURES ON COMPUTER ARCHITECTURE #40

ABSTRACT

This book targets engineers and researchers familiar with basic computer architecture concepts who are interested in learning about on-chip networks. This work is designed to be a short synthesis of the most critical concepts in on-chip network design. It is a resource for both understanding on-chip network basics and for providing an overview of state-of-the-art research in on-chip networks. We believe that an overview that teaches both fundamental concepts and highlights state-of-the-art designs will be of great value to both graduate students and industry engineers. While not an exhaustive text, we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on-chip network research.

With the rapid advances in this field, we felt it was timely to update and review the state of the art in this second edition. We introduce two new chapters at the end of the book. We have updated the latest research of the past years throughout the book and also expanded our coverage of fundamental concepts to include several research ideas that have now made their way into products and, in our opinion, should be textbook concepts that all on-chip network practitioners should know. For example, these fundamental concepts include message passing, multicast routing, and bubble flow control schemes.

KEYWORDS

interconnection networks, topology, routing, flow control, deadlock, computer architecture, multiprocessor system on chip

*To our families
for their encouragement and patience
through the writing of this book.*

Contents

	Preface	xvii
	Acknowledgments	xix
1	Introduction	1
1.1	The Advent of the Multi-core Era	1
1.1.1	Communication Demands of Multi-core Architectures	1
1.2	On-chip vs. Off-chip Networks	2
1.3	Network Basics: A Quick Primer	3
1.3.1	Evolution to On-chip Networks	3
1.3.2	On-chip Network Building Blocks	4
1.3.3	Performance and Cost	5
1.4	This Book—Second Edition	6
2	Interface with System Architecture	9
2.1	Shared Memory Networks in Chip Multiprocessors	9
2.1.1	Impact of Coherence Protocol on Network Performance	11
2.1.2	Coherence Protocol Requirements for the On-chip Network	12
2.1.3	Protocol-level Network Deadlock	13
2.1.4	Impact of Cache Hierarchy Implementation on Network Performance	14
2.1.5	Home Node and Memory Controller Design Issues	18
2.1.6	Miss and Transaction Status Holding Registers	18
2.1.7	Brief State-of-the-Art Survey	21
2.2	Message Passing	22
2.2.1	Brief State-of-the-Art Survey	23
2.3	NoC Interface Standards	23
2.4	Conclusion	25
3	Topology	27
3.1	Metrics	27
3.1.1	Traffic-independent Metrics	28

3.1.2	Traffic-dependent Metrics	29
3.2	Direct Topologies: Rings, Meshes, and Tori	31
3.3	Indirect Topologies: Crossbars, Butterflies, Clos Networks, and Fat Trees	32
3.4	Irregular Topologies	35
3.4.1	Splitting and Merging	35
3.4.2	Topology Synthesis Algorithm Example	37
3.5	Hierarchical Topologies	38
3.6	Implementation	39
3.6.1	Place-and-route	39
3.6.2	Implication of Abstract Metrics	40
3.7	Brief State-of-the-Art Survey	42
4	Routing	43
4.1	Types of Routing Algorithms	43
4.2	Deadlock Avoidance	44
4.3	Deterministic Dimension-ordered Routing	45
4.4	Oblivious Routing	46
4.5	Adaptive Routing	47
4.6	Multicast Routing	51
4.7	Routing on Irregular Topologies	51
4.8	Implementation	52
4.8.1	Source Routing	52
4.8.2	Node Table-based Routing	53
4.8.3	Combinational Circuits	54
4.8.4	Adaptive Routing	55
4.9	Brief State-of-the-Art Survey	56
5	Flow Control	57
5.1	Messages, Packets, Flits, and Phits	57
5.2	Message-based Flow Control	58
5.2.1	Circuit Switching	59
5.3	Packet-based Flow Control	60
5.3.1	Store and Forward	60
5.3.2	Virtual Cut-through	60
5.4	Flit-based Flow Control	61
5.4.1	Wormhole	62

5.5	Virtual Channels	63
5.6	Deadlock-free Flow Control	65
5.6.1	Dateline and VC Partitioning	65
5.6.2	Escape VCs	67
5.6.3	Bubble Flow Control	67
5.7	Buffer Backpressure	69
5.8	Implementation	69
5.8.1	Buffer Sizing for Turnaround Time	70
5.8.2	Reverse Signaling Wires	72
5.9	Flow Control in Application Specific On-chip Networks	72
5.10	Brief State-of-the-Art Survey	73
6	Router Microarchitecture	75
6.1	Virtual Channel Router Microarchitecture	75
6.2	Buffers and Virtual Channels	76
6.2.1	Buffer Organization	77
6.2.2	Input VC State	79
6.3	Switch Design	79
6.3.1	Crossbar Designs	79
6.3.2	Crossbar Speedup	81
6.3.3	Crossbar Slicing	82
6.4	Allocators and Arbiters	82
6.4.1	Round-robin Arbiter	83
6.4.2	Matrix Arbiter	84
6.4.3	Separable Allocator	84
6.4.4	Wavefront Allocator	87
6.4.5	Allocator Organization	88
6.5	Pipeline	90
6.5.1	Pipeline Implementation	90
6.5.2	Pipeline Optimizations	92
6.6	Low-power Microarchitecture	95
6.6.1	Dynamic Power	96
6.6.2	Leakage Power	97
6.7	Physical Implementation	98
6.7.1	Router Floorplanning	98
6.7.2	Buffer Implementation	100
6.8	Brief State-of-the-Art Survey	100

7	Modeling and Evaluation	103
7.1	Evaluation Metrics	103
7.1.1	Analytical Model	103
7.1.2	Ideal Interconnect Fabric	105
7.1.3	Network Delay-throughput-energy Curve	105
7.2	On-chip Network Modeling Infrastructure	107
7.2.1	RTL and Software Models	108
7.2.2	Power and Area Models	108
7.3	Traffic	109
7.3.1	Message Classes, Virtual Networks, Message Sizes, and Ordering	109
7.3.2	Application Traffic	110
7.3.3	Synthetic Traffic	112
7.4	Debug Methodology	112
7.5	NoC Generators	113
7.6	Brief State-of-the-Art Survey	114
8	Case Studies	117
8.1	MIT Eyeriss (2016)	117
8.2	Princeton Piton (2015)	120
8.3	Intel Xeon-Phi (2015)	122
8.4	D E Shaw Research Anton 2 (2014)	123
8.5	MIT SCORPIO (2014)	124
8.6	Oracle Sparc T5 (2013)	126
8.7	University of Michigan Swizzle Switch (2012)	126
8.8	MIT Broadcast NoC (2012)	128
8.9	Georgia Tech 3D-MAPS (2012)	130
8.10	KAIST Multicast NoC (2010)	130
8.11	Intel Single-chip Cloud (2009)	132
8.12	UC Davis AsAP (2009)	133
8.13	Tilera TILEPRO64 (2008)	135
8.14	ST Microelectronics STNoC (2008)	137
8.15	Intel TeraFLOPS (2007)	139
8.16	IBM Cell (2005)	141
8.17	Conclusion	142

9 Conclusions 145

9.1 Beyond Conventional Interconnects 145

9.2 Resilient On-chip Networks 147

9.3 NoCs as Interconnects within FPGAs 148

9.4 NoCs in Accelerator-rich Heterogeneous SoCs 148

9.5 On-chip Networks Conferences 149

9.6 Bibliographic Notes 150

References 151

Authors' Biographies 189

Preface

This book targets engineers and researchers familiar with many basic computer architecture concepts who are interested in learning about on-chip networks. This work is designed to be a short synthesis of the most critical concepts in on-chip network design. We envision this book as a resource for both understanding on-chip network basics and for providing an overview of state-of-the-art research in on-chip networks. We believe that an overview that teaches both fundamental concepts and highlights state-of-the-art designs will be of great value to both graduate students and industry engineers. While not an exhaustive text, we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on-chip network research.

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The structure of this book is as follows. Chapter 1 introduces on-chip networks in the context of multi-core architectures and discusses their evolution from simple point-to-point wires and buses for scalability.

Chapter 2 explains how networks fit into the overall system architecture of multi-core designs. Specifically, we examine the set of requirements imposed by cache-coherence protocols in shared memory chip multiprocessors, and contrast that with the requirements in message-passing multi-cores. In addition to examining the system requirements, this chapter also describes the interface between the system and the network.

Once a context for the use of on-chip networks has been provided through a discussion of system architecture, the details of the network are explored. As topology is often a first choice in designing a network, Chapter 3 describes various topology trade-offs for cost and performance. Given a network topology, a routing algorithm must be implemented to determine the path(s) messages travel to be delivered throughout the network fabric; routing algorithms are explained in Chapter 4. Chapter 5 deals with the flow control mechanisms employed in the network; flow control specifies how network resources, namely buffers and links, are allocated to packets as they travel from source to destination. Topology, routing, and flow control all factor into the microarchitecture of the network routers. Details on various microarchitectural trade-offs and design issues are presented in Chapter 6. This chapter includes the design of buffers, switches, and allocators that comprise the router microarchitecture. Although power consumption can

be addressed through innovations in all areas of on-chip networks, we focus our new power discussion in the microarchitecture chapter as this is where many such optimizations are realized.

New Chapter 7 covers the nuts and bolts of modeling and evaluating on-chip networks, from software simulations to RTL design and emulation on FPGA, to architectural models of delay, throughput, area, and power. The chapter also guides the reader on useful metrics for evaluating on-chip networks and ideal theoretical yardsticks for comparing against.

With the plethora of industry and academia on-chip network chips now available, we dedicate a new Chapter 8 to a survey of these. The chapter provides the reader with a sweeping understanding of how the various fundamental concepts presented in the earlier chapters come together, and the implications of the design and implementation of such concepts.

Finally in Chapter 9, we leave the reader with thoughts on key challenges and new areas of exploration that will drive on-chip network research in the years to come. Substantial new research has clearly surfaced, and here we focus on various significant trends that highlight the cross-cutting nature of on-chip network research. Emerging new interconnects and devices substantially change the implementation tradeoffs of on-chip networks, and in turn prompt new designs. Newly important metrics such as resilience, due to increasing variability in the fabrication process, or quality-of-service that is prompted by multiple workloads running simultaneously on many-cores, will add new dimensions and prompt new research ideas across the community.

Natalie Enright Jerger, Tushar Krishna, and Li-Shiuan Peh
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