Generation of Lifetime-Aware Pareto-Optimal Fronts Using a Stochastic Reliability Simulator

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***Abstract*—Process variability and time-dependent variability have become major concerns in deeply-scaled technologies. Two of the most important time-dependent variability phenomena are Bias Temperature Instability (BTI) and Hot-Carrier Injection (HCI), which can critically shorten the lifetime of circuits. Both BTI and HCI reveal a discrete and stochastic behavior in the nanometer scale, and, while process variability has been extensively treated, there is a lack of design methodologies that address the joint impact of these two phenomena on circuits. In this work, an automated and time-efficient design methodology that takes into account both process and time-dependent variability is presented. This methodology is based on the utilization of lifetime-aware Pareto-Optimal Fronts (POFs). The POFs are generated with a multi-objective optimization algorithm linked to a stochastic simulator. Both the optimization algorithm and the simulator have been specifically tailored to reduce the computational cost of the accurate evaluation of the impact on a circuit of both sources of variability.**

Keywords—Reliability, Aging, BTI, HCI, Lifetime, Simulation, Optimization, Pareto front

I. INTRODUCTION

In recent years, variability phenomena have become of increasing interest in deeply-scaled CMOS technologies. These include process variability (PV) and time-dependent variability (TDV). TDV comprises different phenomena, two of the most important being Bias Temperature Instability (BTI) and Hot-Carrier Injection (HCI), both of which can become a critical issue for circuits, causing, among other problems, the reduction of their lifetime [1]. Such reduction comes from a degradation of the transistor parameters, such as threshold voltage and mobility, which has a permanent and a recoverable component. BTI and HCI are especially important in deeply-scaled CMOS technologies, in which their behavior reveals a discrete and stochastic behavior [2], [3]. Because of the stochastic nature of these TDV phenomena and PV, nominally identical circuits can age differently. For this reason, the concept of time-dependent yield $TDY(t)$ can be introduced as the percentage of designs that fulfill a set of performance specifications at time t. Then, by setting a minimum acceptable yield, the lifetime of a circuit can be defined as the operation time of a circuit before its yield becomes smaller than that threshold value.

To mitigate the impact of TDV on circuits, the development of reliability-aware design (RAD) tools is fundamental. In particular, the lack of design methodologies to address these problems in the nanometer scale, especially for analog circuits, has become the focus of significant effort in the field of electronic design automation. These tools allow the designer to get accurate information on the impact of reliability effects on the circuit performances and lifetime early in the design process. However, the re-design iterations commonly associated to handcrafted designs can lead to impractical design times. Therefore, optimization-based approaches are becoming of increasing interest, since they allow the designer to overcome the limitations of knowledge-based methodologies by using optimization algorithms capable of performing wide design space exploration in order to find optimal designs with respect to one (single-objective algorithms) or several (multi-objective algorithms) performances. In this sense, several approaches to optimize the circuit performances, yield/lifetime or several of them have been reported [4]-[12]. In [4], a Monte-Carlo (MC) based method is presented for efficient yield optimization. In it, the total number of MC iterations is drastically reduced by selecting of a small number of representative solutions to perform the MC simulations. In [5], efficient techniques are presented for yield optimization and yield-constrained single-objective optimization. In them, only information about process variability is included. An efficient method for extracting a yield-aware Pareto front between two competing metrics of an analog circuit block, aimed at performing hierarchical system-level optimization, is reported in [6]. In [7], yield-optimized Pareto fronts are obtained by optimizing the performances at the worst-case conditions. In [8], a bi-objective stochastic optimization technique is used to generate the trade-off between yield and power. A bi-objective optimization to explore the trade-offs between yield and a figure of merit involving several performances is presented in [9]. In [10], a multi-objective optimizer generates Pareto fronts of the yield together with other performances. In [11], the lifetime, calculated via a deterministic reliability simulator, is included as a new constraint into a single objective optimization. In [12], the trade-off between lifetime and area is calculated by using an iterative single-objective optimization while considering a maximum area constraint. Although all these methods are useful to designers, they present a series of limitations. Most of them construct yield-aware Pareto fronts or address only process yield optimization, i.e., no circuit degradation along time is considered. In terms of time-dependent variability, only a deterministic reliability simulation approach has been used in order to develop a lifetime-constrained optimization or trade-offs between lifetime and area.

To address the limitations of previous approaches, a lifetime-aware design methodology based on multi-objective optimization is introduced in this paper. Lifetime, accounting for TDV, can be used as both an optimization objective and a

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constraint. The optimization process embeds a reliability simulator that is able to simultaneously consider stochastic TDV effects and PV, as well as their correlations. Computational efficiency is achieved by introducing a 4-stage evaluation process within the optimization loop and a 2-stage method in the calculation of the lifetime.

The rest of the paper is structured as follows: in Section II, the stochastic reliability simulator is reviewed and the characteristics that make it suitable to be integrated in an optimization-based methodology are highlighted. In Section III, the procedure to calculate a circuit lifetime using the stochastic reliability simulator is explained. In Section IV, the methodology to generate a lifetime-aware POF is described, and in Section V it is applied to a case study. Finally, conclusions are drawn in Section VI.

II. The Stochastic Reliability Simulator

The challenges that a reliability simulator should address in order to properly deal with nanometer-scale technologies are [3]:

- It should be based in stochastic TDV models in order to account for the random nature of HCI and BTI.
- It should handle the correlation between PV and TDV.
- It should include the dynamic bidirectional feedback between aging and biasing (i.e., stress) conditions.

In recent years, several simulators have been proposed in the literature to evaluate circuit reliability in the presence of time-dependent phenomena. Some commercial simulators allow studying the impact of BTI and HCI on circuit performance after a given operation time under certain conditions [13]-[15]. However, these simulators use deterministic models to describe the different transistor degradation phenomena and are not adequate for deeply-scaled CMOS technologies. A first attempt at developing a stochastic reliability simulator was presented in [16]. In it, stochastic process variability and stochastic soft-break down effects were included. However, BTI and HCI effects were still included with deterministic models that are repeatedly evaluated to mimic stochastic sampling.

A reliability simulator with a full stochastic model for time-dependent variability together with another stochastic model to take into account the process variability was presented in [17]. It uses the foundry-provided model parameters for process variability. Regarding TDV, it uses the Probabilistic Deffect Occupancy (PDO) model [18] to account for the stochastic nature of BTI and HCI in deeply-scaled technologies, being the first reported simulator to take into consideration this stochasticity. The PDO model assigns discrete threshold voltage shifts to charge trapping/detrapping from defects in the device during the stress/recovery phase of BTI and HCI. Each defect has an associated threshold voltage shift η and capture and emission times (τ_c, τ_e). These time constants are defined as the average time that the defect takes to capture or emit a charge carrier, and are bias and temperature dependent. The other variable used by the model is the defect density, i.e., the number of defects per unit of channel area, which is characteristic of each technology process. With this information, it is possible to randomly generate a number of transistor samples, each one with a given number of defects, each of which will cause a certain parameter degradation when occupied and have a given pair of time constants. Then, if the bias and temperature conditions (i.e., the stress conditions) during a certain operation time (e.g., one year) are known, it would be in principle possible to simulate if these defects are empty or occupied, and, therefore, calculate the degradation of each transistor sample.

However, due to the degradation of the transistors during the circuit operation, the transistor biasing and, therefore, the stress conditions vary. For this reason, a number of intermediate steps are necessary to update the stress conditions and account for this bidirectional feedback between degradation and stress along the operation time. The corresponding simulation flow is displayed in Fig. 1. Most commercial simulators include the option of incorporating intermediate steps. However, these tools use fixed time scales (such as linear or logarithmic distribution of the steps) that may not fit adequately the general behavior of the degradation [3]. Using a scale that does not properly adjust to the evolution of the circuit degradation would demand a very high number of intermediate steps in order to accurately update the stress conditions, and this would lead to very high computation times. This is not convenient, since a considerable number of simulations has to be performed during a typical optimization process, with thousands of candidate solutions to simulate. To achieve an accurate result while keeping the computational time as low as possible, the reliability simulator in [17] uses an algorithm that adapts the size of time steps with the progressive aging of the circuit [19]. This algorithm works by setting a maximum value for the degradation of the devices triggering a re-calculation of the stress conditions. This approach allows achieving a low computational time while ensuring a high accuracy in the calculation of the circuit degradation.

The most straightforward method to update each sample while simultaneously accounting for the stochastic nature of of both, PV and TDV, is to start with a set of samples at time zero according to PV. Then, each sample is aged separately, and at each intermediate step, each sample of the statistical distribution of TDV is used to update the stress conditions. However, as the number of steps increases, the number of aged samples would increase exponentially, leading to unaffordable computational times. To optimize the trade-off

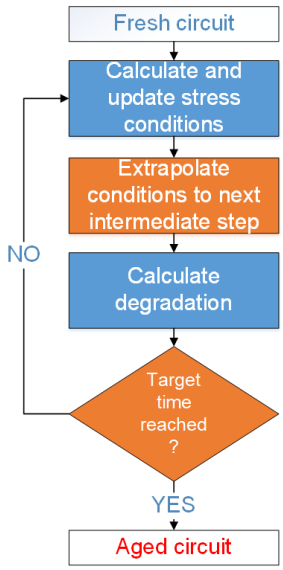

Fig. 1. Simulation flow of the stochastic reliability simulator.

between CPU time and accuracy, several methods based on averaging PV or TDV at each intermediate step have been reported in [20].

By calculating the stochastic degradation of the transistors that integrate a circuit, it is possible to study the evolution of its performances over time and, with it, the evolution of its TDY and its lifetime. The combination of these features makes the stochastic reliability simulator a promising candidate to be integrated into an accurate and time-efficient lifetime-aware multi-objective performance optimization.

III. Lifetime Simulation

The stochastic reliability simulator CASE enables a time-efficient 2-stage method to calculate the lifetime of a circuit [17], [21]. Its flow diagram is shown in Fig. 2.

The user begins by defining the design specifications or constraints that determine the TDY. Then, to determine the lifetime of the circuit, a minimum TDY (TDY_{min}) is set so that the lifetime is found when the TDY goes below TDY_{min}. To avoid unnecessary calculations, the designer can define a temporal window, setting a minimum (T_{min}) and a maximum time (T_{max}), where the analysis of the lifetime is carried out. Then, the TDY calculation within that window is performed in 2 stages: first, the yield is sequentially estimated at each intermediate time step T_i within that window with a so-called MC estimation, which uses a reduced number of samples (≈ 20, although the exact number can be chosen by the user). If the estimated TDY is higher than the minimum yield at T_i, the algorithm proceeds to the next step and performs a MC estimation at T_{i+1}. If, on the contrary, the estimated TDY is lower than the minimum yield at T_i, a more exact calculation of the TDY is performed with a larger number of MC samples (≈ 1,000, although the exact number can also be chosen by the user). If this newly calculated TDY lies above TDY_{min}, the algorithm proceeds to the next step T_{i+1}. If on the contrary the TDY calculated with a high number of samples at T_i also lies below the threshold value, the yield must be evaluated again in the previous step T_{i-1} using the higher number of samples too. If the obtained yield at T_{i-1} is larger than the minimum one, the lifetime has been found (T_i). If the lifetime is larger than T_{max} or smaller than T_{min}, only one complete MC analysis is carried out at either point in time. By performing expensive MC simulations only at time points at which the TDY has been estimated to be close to its minimum threshold value, the method allows to drastically reduce the computational time needed for the calculation of the lifetime of a given circuit. This feature is crucial when the simulator is to be integrated within a lifetime-aware optimization methodology in which, as mentioned above, the lifetime will be calculated for many circuit instances.

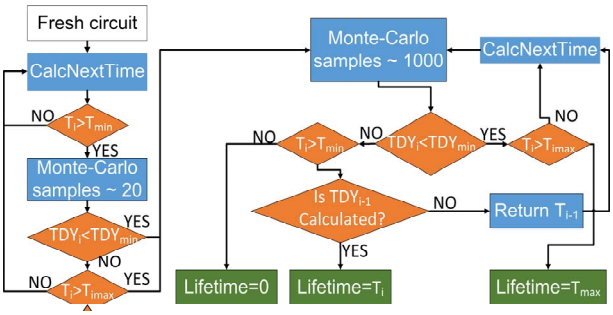

Fig. 2. Diagram of the two-stage process used for the calculation of the circuit lifetime.

IV. Lifetime-Aware Optimization

The reliability simulator with the lifetime simulation ability in Section III can be linked to an optimization algorithm in order to perform lifetime-aware circuit optimizations.

A. Considering Lifetime in Optimization Loops

Circuit design problems can be considered as an optimization problem, mathematically formulated as,

$$\begin{aligned} &\text{minimize } f(x); && f(x)\in R^m \\ &\text{subject to } g(x)\le 0; && g(x)\in R^k \\ &x\in\Omega \end{aligned} \qquad (1)$$

where $f(x)$ is a vector of m objective functions, $g(x)$ is a vector of k constraints and x is a vector of n design variables on the search space Ω. In this work, the number of objectives is greater than one ($m>1$), and a multi-objective optimization algorithm may be applied to solve (1). During the optimization, if any design constraint $g(x)$ is not fulfilled, the constraint violation parameter CV is calculated, which considers how many and how much the constraints are violated. This parameter can be used by multi-objective optimization algorithms to compare two solutions when some design constraint is not met. Accordingly, a solution a is said to constrain-dominate solution b if and only if a has a smaller constraint violation than b, or, if all constraints are met, $f_i(a) \le f_i(b)$, for every $i\in\{1,...,m\}$ and $f_j(a) < f_j(b)$ for at least an index $j\in\{1,\ldots,m\}$. A point $y\in\Omega$ is Pareto-optimal if it is not dominated by any other point in Ω. The set of all Pareto-optimal points is named the Pareto-optimal set and the corresponding points in the feasible objective space form the Pareto-optimal front (POF).

In a standard population-based optimization algorithm, all candidate solutions (individuals) must be evaluated at each generation, i.e., are simulated to calculate the value of their design objectives and constraints. In the lifetime-aware optimization proposed in this work, the lifetime is used as design objective, and must be handled in a special manner because:

- the evaluation of the lifetime is time consuming;
- the lifetime is related with the design constraints through the minimum yield required;
- the lifetime can also be a design constraint, i.e., the user may specify a minimum lifetime.

For these reasons, a new evaluation process must be proposed to efficiently obtain the desired lifetime-aware POF using a multi-objective optimization algorithm.

B. Evaluation Process for an Efficient Lifetime-Aware Optimization

The new evaluation process proposed in this work allows reducing the computational impact of the lifetime calculation during the optimization process by avoiding the evaluation of individuals with a lifetime smaller than the minimum required. Another important byproduct is that the new

evaluation process helps the optimizer to find the feasible search space more efficiently, as detailed below.

First, it must be specified how lifetime is calculated. This definition is composed of two inputs: (1) the minimum value of TDY, TDY_{min}, used by the reliability simulator to calculate the lifetime, (2) the lifetime calculation windows (T_{max} and T_{min}), i.e., as circuits with lifetime values below T_{min} (e.g., 1 day) are of no interest and the precise value of a lifetime above T_{max} (e.g., 100 years) may not be that important. TDY_{min} is not defined as an absolute value but a percentage YR of the yield at time zero, $TDY(t=0)$. That is, YR represents the time-dependent yield referred not to the fabricated circuits but only to the fully functional fabricated circuits. This information is used by the new evaluation process to reduce the time needed to evaluate the lifetime of each individual in the population during each generation. Fig. 3 illustrates the new evaluation process within a standard population-based optimization algorithm. While in standard algorithm implementations all individuals of a population are evaluated using an identical process, in this new evaluation process each individual undergoes different evaluations, depending on the particular values of its design objectives and constraints.

When the optimizer needs to evaluate a given population, a circuit simulator is used to evaluate all the design objectives (other than lifetime) and all the design constraints (other than yield and lifetime). After this nominal simulation, each individual is evaluated separately to calculate the lifetime as shown in Fig. 3. The evaluation process has been divided in 4 stages with the goal of reducing the computational effort as much as possible and to make the exploration of the design space more efficient. For these reasons, additional constraints are added to the optimization problem. The idea behind is to start with the cheapest evaluation and progressively advance to the next evaluation stage only with those individuals that check off the previous evaluation stage(s):

1) If some design constraints are not fulfilled after the initial nominal simulation (i.e., $CV<0$), the individual is assigned a lifetime equal to zero. The CV at this stage is calculated using the design constraints other than TDY and lifetime. If the individual fulfills these design constraints ($CV=0$), the reliability simulator comes into play.

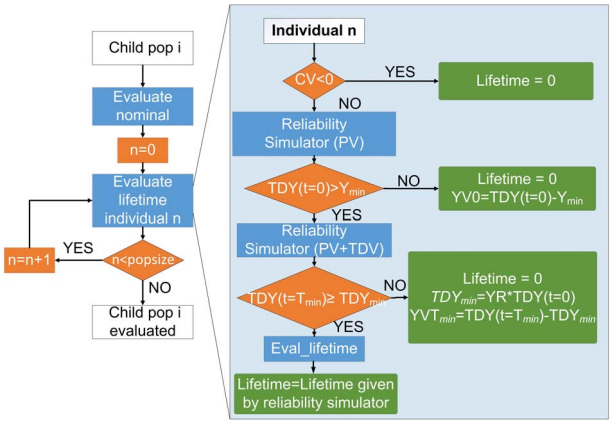

Fig. 3. The new evaluation process to optimize the circuit lifetime.

2) The reliability simulator is then used to evaluate the impact of process variations. For this, a MC analysis is carried out to evaluate the yield at time zero ($TDY(t=0)$). The minimum value of yield Y_{min} is set as an additional design constraint (yield constraint at time zero). If the impact of process variations causes the yield to be smaller than Y_{min}, the lifetime is 0, and the value of yield violation at time zero ($YV0$) is calculated as:

$$YV0 = TDY(t=0) - Y_{min} \tag{2}$$

Two important advantages of this evaluation stage are:

- If the impact of process variations causes that $TDY(t=0) \le Y_{min}$, only one MC analysis is used to calculate the lifetime.
- Although not all individuals fulfill the minimum required yield at time zero, the individuals can be classified using $YV0$, and the ones closest to fulfill this constraint can be selected for the next generation.

If the additional design constraint is fulfilled (i.e., $TDY(t=0) > Y_{min}$), the impact of PV and TDV is then evaluated using the reliability simulator.

3) As mentioned before, a lifetime constraint is also imposed ($\text{lifetime} \ge T_{min}$). This stage evaluates this constraint with only one MC analysis. Although a high number of MC analyses may be needed to evaluate the circuit lifetime using the reliability simulator, in this stage only one MC analysis is used to gain efficiency. For that, in this stage, an additional constraint is imposed on $TDY(t=T_{min})$:

$$TDY(t=T_{min}) \ge TDY_{min} = YR \cdot TDY(t=0) \tag{3}$$

Note that it is possible to calculate the yield using a small number of time steps, which speeds up this evaluation stage. However, with a lower number of steps, the calculation of $TDY(t=T_{min})$ is not very accurate and some "false positive" individuals may appear. Nevertheless, this does not impact the final outcome as, in the next evaluation stage, a high number of steps is always used. If the yield is smaller than the desired minimum, the value of yield violation at time T_{min} ($YVT_{\min}$) is calculated as:

$$YVT_{\min} = TDY(t=T_{min}) - TDY_{min} \tag{4}$$

This evaluation stage causes similar advantages than the previous stage.

4) Finally, if the yield ($TDY(t=T_{min})$) is larger than the minimum, the lifetime of the circuit is fully calculated by the reliability simulator using the 2-stage method in Section III.

In this new evaluation process, two additional parameters are included: $YV0$ and $YVT_{\min}$. The use of these parameters

is similar to the use of the CV parameter when it is used to check the dominance between two individuals. When both individuals fulfill all design constraints, (that is, $CV = 0$), the dominant individual is chosen using the Pareto-dominance criterion. In this new evaluation procedure, when both individuals fulfill all design constraints (other than yield and lifetime), that is, $CV = 0$, the parameter $YV0$ is used to check the dominance. In this case, the individual closest to fulfill this new constraint is selected. When both individuals fulfill the yield constraint at time zero (i.e., $YV0 = 0$), the parameter $YVT_{\min}$ is used to select the individual closest to fulfill the yield constraint at T_{min}. Finally, when both individuals fulfill all constraints ($CV = YV0 = YVT_{\min} = 0$), the Pareto dominance criterion for the design objectives is used.

In summary, in the proposed evaluation process, the first evaluation stage comprises only the simulation of the nominal design (without PV and TDV). The second stage involves only the impact of PV and, in a third stage, the impact of both PV and TDV at T_{min}. The lifetime is only calculated if all the constraints are fulfilled in the first three stages of evaluation. This means that the lifetime analysis, typically quite expensive, is avoided for a high number of individuals during the optimization process. It is important to note that the time needed to calculate the lifetime is approximately between 2 and 20 times the total time needed for the other evaluations. Typical optimization algorithms explore the design space searching individuals with lifetime larger than the minimum defined, using a "brute force" approach to include the information of PV and TDV. For a given number of individuals evolved through a defined number of generations, this "brute force" approach may not find any satisfactory results while the evolution process presented in this work does. Furthermore, even if the typical optimization algorithm leads to satisfactory results, the organized manner in which the design space is explored in the 4-stage evaluation process presented in this work reduces drastically the total number of individuals needed to generate a lifetime-aware POF, leading to a reduction of the computational time of approximately 40%.

V. Case Study

The use of optimization algorithms with the new evaluation process allows the efficient inclusion of the lifetime as an objective together with other circuit performances. As a result of such optimizations, the designer will gain an insight on the trade-offs between the achievable circuit performances and the lifetime. In this Section, the design of a two-stage Miller op-amp in a 65nm CMOS technology will be used as a case study to show the potential of such lifetime-aware optimizations. The circuit schematic is shown in Fig. 4.

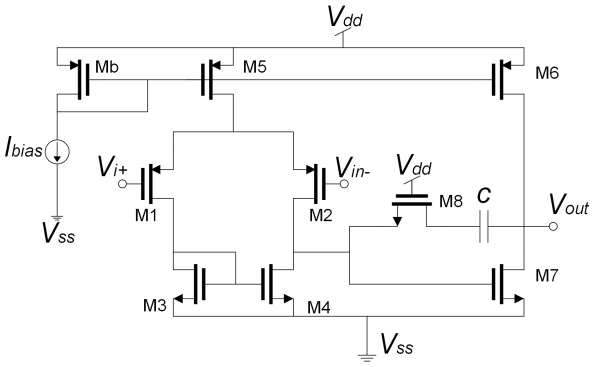

Fig. 4. Schematic of a two-stage Miller op-amp. The output load is 1pF.

TABLE I. Minimum and Maximum Values of the Variables Used in the Optimization

Variable name	Min. Value	Max. Value
$W_{1\text{-}8}$	100 nm	100 µm
W_b	100 nm	100 µm
$L_{1\text{-}8}$	60 nm	1 µm
L_b	60 nm	1 µm
C	1 fF	10 pF
I_{bias}	10 nA	10 µA

All variables used in the optimization, together with their lower and upper bounds, are detailed in Table 1. The constraints on the design objectives are a phase margin > 60º, no zeros between the dominant poles and a yield at time 0 $TDY(t=0) > 90\%$. In this case, the lifetime is defined as the operation time of the design before the yield becomes lower than $0.9 \cdot TDY(t=0)$. On the other hand, the optimization objectives are the dc gain, the unity-gain frequency (fu), the lifetime and the yield at time 0. A 10% maximum degradation of the design objectives is allowed during the circuit lifetime. The POF has been generated using 400 individuals evolving across 150 generations. The time needed to evaluate each generation varies largely: from a few seconds required to evaluate a population in the first generations to a few minutes per individual in the last generations on a 2.2-GHz processor.

Fig. 5 shows the final population in this case study. Having four design objectives, it is difficult to perform a graphical representation. Therefore, the X, Y and Z axis of a 3D plot have been used to represent DC gain, unity-gain frequency and lifetime, respectively, whereas the yield at time zero has been represented with a color code at the points, as indicated in the right bar of Fig. 5.

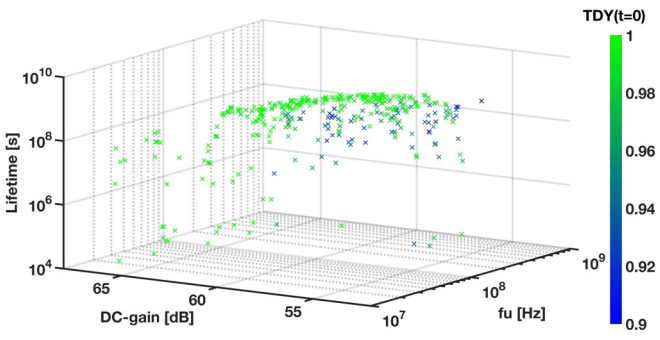

Fig. 5. Lifetime-aware POF generated using 400 individuals evolved across 150 generations.

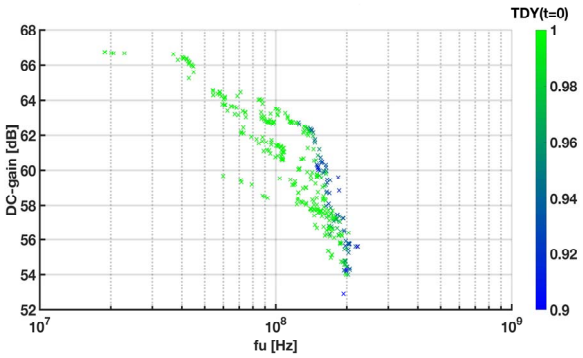

Fig. 6. DC-gain vs. unity-gain frequency of the generated POF.

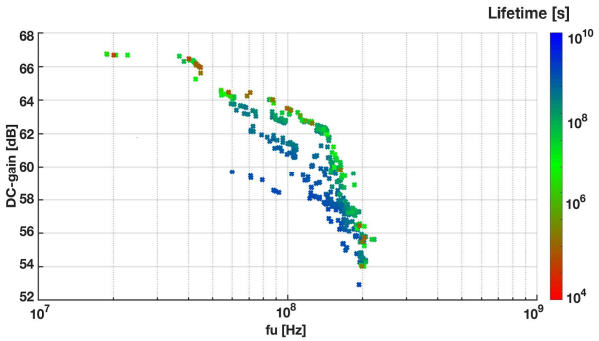

Fig. 7. DC-gain vs. unity-gain frequency of the generated POF. The color represents the lifetime of each individual.

Visual inspection is eased in Fig. 6 by projecting the results of Fig. 5 at the fu-gain plane and using the color code to represent $TDY(t=0)$. It can be observed that most designs available have a maximum yield and only the designs with higher unity-gain frequency have a yield degradation. This information can be used to select an appropriate circuit sizing. However, valuable information is obtained by looking at Fig. 7, where a similar projection is performed but the color code represents the lifetime. It is interesting to see that the best trade-offs between dc gain and unity-gain frequency imply a degradation of the circuit lifetime. Moreover, by just looking at the effect of process variations, as shown in Fig. 6, a designer might be tempted to select a high gain design (left region of the Pareto front) trusting that the yield is very good. However, Fig. 7 shows that although it is true that $TDY(t=0)$ is high, it degrades quickly and the lifetime is short.

VI. Conclusions

In this work, a novel design methodology that uses a multi-objective optimization algorithm together with a stochastic reliability simulator for lifetime calculation has been presented. This methodology enables the designer to generate lifetime-aware POFs, in which the lifetime is optimized together with other circuit performances, which allows to achieve the best performance trade-offs for the longest possible lifetime.

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