# A Simple Hybrid Model for Accurate Delay Modeling of a Multi-Input Gate 

Arman Ferdowsi ©, Jürgen Maier ©, Daniel Öhlinger ©, Ulrich Schmid ©<br>TU Wien, ECS Group (E191-02)<br>\{aferdowsi, jmaier, doehlinger, s\}@ecs.tuwien.ac.at


#### Abstract

Faithfully representing small gate delay variations caused by input switchings on different inputs in close temporal proximity is a very challenging task for digital delay models. In this paper, we use the example of a 2 -input NOR gate to show that a simple hybrid model leads to a surprisingly accurate digital delay model. Our model utilizes simple first-order ordinary differential equations (ODEs) in all modes, resulting from considering transistors as ideal switches in a simple RC model of the gate. By analytically solving the resulting ODEs, we derive expressions for the gate delays, as well as formulas that facilitate model parametrization. It turns out that our model almost faithfully captures the Charlie effect, except in just one specific situation. In addition, we experimentally compare our model's predictions both to SPICE simulations, using some 15 nm technology, and to some existing delay models. Our results show a significant improvement of the achievable modeling accuracy.

Index Terms-multi input switching, delay model


## I. Introduction

Digital circuit design relies heavily on fast digital timing analysis techniques, since they are orders of magnitude faster than analog simulations, e.g., in SPICE. In contrast to static approaches, dynamic digital timing analysis predicts the propagation of arbitrary signal traces throughout a circuit. Going beyond the popular pure (= constant input-to-output delay) and inertial delay (= constant delay + too short pulses being removed) models [1], single-history delay models [2], [3] achieve an improved behavioral coverage. Indeed, as proved in [4], it is inevitable for any faithful delay model that a gate's input-to-output delay $\delta(T)$, for a given transition, depends on a parameter like the previous-output-to-input delay $T$.

The involution delay model (IDM) proposed in [3] consists of zero-time boolean gates, which are interconnected by single-input single-output involution delay channels. IDM channels are characterized by a delay function $\delta(T)$, which is a negative involution, in the sense that $-\delta(-\delta(T))=T$. Unlike all other existing delay models, the IDM faithfully models glitch propagation in the simple short-pulse filtration problem, and is hence the only candidate for a faithful delay model known so far.

Moreover, the IDM comes with a publicly available timing analysis framework (the Involution Tool [5]), which is based on an industrial simulation suite. The Involution Tool allows to randomly generate input traces for a given circuit, and to

[^0]evaluate the accuracy of IDM predictions compared to SPICEgenerated transition times and/or other digital models like inertial delays.

Whereas the accuracy of IDM predictions for single-input, single-output circuits like inverter chains or clock trees reported in [5] is impressive, this is less so for circuits involving multi-input gates. We conjecture that this is mainly due to the inherent lack of properly covering output delay variations caused by multiple input switching (MIS) in close temporal proximity [6], also known as the Charlie effect (named after Charles Molnar, who identified its causes in the 70th of the last century). Compared to the single input switching (SIS) case, the output transition is sped up/slowed down with decreasing transition separation time on different inputs here. Singleinput, single-output IDM delay channels obviously cannot exhibit such a behavior.
Multiple approaches have been proposed to cover MIS effects in literature, ranging from linear [7] or quadratic fitting [8] over higher-dimensional model representation [9] to recent machine learning methods [10]. However, none of these naturally generalizes to multi-input involution channels.

In order to define a 2 -input IDM channel, we thus generalize the simple analog first-order model matching a classic IDM channel (which can be viewed as a hybrid model with only two modes $)^{1}$ to a four-mode hybrid model: For each state of the inputs $(A, B) \in\{(0,0),(0,1),(1,0),(1,1)\}$, a system of first-order ordinary differential equations (ODEs) is derived, which governs the analog trajectory of the gate's output in the respective mode. At an input change, the mode is instantaneously switched, in a way that guarantees continuity of the output signal. Whereas similar approaches have been advocated in [11], [12], these rely on analog fitting or extraction of unique switching waveforms.

Main contributions: (1)We introduce a simple hybrid ODE model of a 2-input CMOS NOR gate, which results from replacing transistors in a simple RC model of the circuit by ideal switches that are switched on/off at the respective input threshold voltage $V_{t h}=V_{D D} / 2$ crossing times. We analytically solve the ODE systems for every mode, and derive expressions for the resulting MIS gate delay $\delta(\Delta)$, defined by the time when the output waveform crosses $V_{t h}$; the parameter $\Delta=t_{B}-t_{A}$ denotes the switching time separation of the

[^1]

Fig. 1: Transistor level implementation of the NOR gate.
inputs. It turns our that the resulting delay model captures all MIS effects very well, except for one case ( $\Delta<0$ for rising output transitions).
(2) We develop expressions to ease the parametrization of our ODE model, given the characteristic SIS delay values $\delta(-\infty)$ and $\delta(\infty)$ as well as the MIS value $\delta(0)$. Since it turned out that it is impossible to simultaneously match all three values for a real circuit simultaneously, we had to add an additional pure delay (supported by the IDM) to our parametrization.
(3) We use an appropriately extended version of the Involution Tool to compare the average modeling accuracy of our hybrid model to other analog/digital simulations. To that end, we evaluate random traces for one of the circuits studied in [5], using some empirically optimal parametrization of our hybrid model. Whereas the latter outperforms the original IDM, as well as standard models like inertial delays, its deficiency in fully capturing all MIS effects also somewhat impairs its average accuracy.

In a nutshell, our results show that describing multi-input gates with hybrid models is beneficial, albeit our instantaneously switching transistor abstraction is slightly too simplistic to fully cover all MIS effects.

Paper organization: In Section II, we explain the causes for MIS delay variations and determine characteristic values for a NOR gate. In Section III, we present our simple hybrid ODE model and explore in Section IV its ability to capture MIS effects. Section V provides formulas for parametrizing the model, and Section VI quantifies the average modeling accuracy. Some conclusions and directions of future research close the paper in Section VII.

## II. Multiple Input Switching (MIS)

In this section, we will provide some basic explanations for MIS effects and quantify those by conducting analog simulations using Spectre (version 19.1) and the Nangate Open Cell Library featuring FreePDK15 ${ }^{\mathrm{TM}}$ FinFET models [13]. The investigated CMOS NOR gate is among the simplest multiinput gates and hence a natural target for our analysis. Its transistor-level implementation, with the parasitic capacitance $C_{N}$ and the output load capacitance $C_{O}$, is shown in Fig. 1. As we will explore later, the transistor arrangement plays
a decisive role in explaining the observed delay variations: While the pMOS ( $T_{1}$ and $T_{2}$ ) are connected in series towards $V_{D D}$, the nMOS ( $T_{3}$ and $T_{4}$ ) provide parallel paths towards GND.

In the sequel, we apply the rising/falling input waveforms $f_{\uparrow / \downarrow}\left(t-t_{A}\right)$ on input $A$ resp. $f_{\uparrow / \downarrow}\left(t-t_{B}\right)$ on input $B$, whereat $t_{A}$ resp. $t_{B}$ denote the point in time the discretization threshold voltage $V_{t h}=V_{D D} / 2$ is crossed. In the same spirit, $t_{O}$ denotes the time when the output voltage $V_{O}$ crosses $V_{D D} / 2$. Varying $t_{A}$ and $t_{B}$ allows us to represent the gate delay by $t_{O}-t_{A}$ resp. $t_{O}-t_{B}$ (depending on the particular output state) over the relative input separation time $\Delta=t_{B}-t_{A}$.

We first consider the case of a falling output transition. In a nutshell, either transistor $T_{3}$ or $T_{4}$ starts to conduct (is closed), while one of the two pMOS transistors in series stops conducting (is opened). Consequently, the output is drained and $V_{O}$ starts to decrease. It is easy to see that it makes a difference whether only one or both nMOS transistors are closed, i.e., only a single or both inputs switch, as it takes, at least theoretically, only half the time to drain the output in parallel. So the MIS causes a speed-up here, whose effect is clearly visible in the analog waveforms shown in Fig. 2a: When both transistors start to conduct, the output slope changes notably, leading to a reduction of the gate delay.

As the first rising input transition already induces an output transition, the relevant gate delay is $\delta_{S}^{\downarrow}(\Delta)=t_{O}-$ $\min \left(t_{A}, t_{B}\right)$, i.e., the time difference between the threshold crossing of the output and the earlier input (see Fig. 2b). As predicted, the delay is the smallest for simultaneous transitions ( $\Delta=0$ ), whereat the change in delay is around $30 \%$. Note that $\delta_{S}^{\downarrow}(-\infty) \neq \delta_{S}^{\downarrow}(\infty)$ is mainly caused by transistor $T_{2}$, which is closed in one case, connecting nodes $N$ and $O$, while in the other it is open (see Section III). Although the absolute values differ, our results fit very well ${ }^{2}$ to previous investigations in other technologies [7], [8], [9].

A less visible phenomenon of the speed-up MIS effect deserve to be mentioned here: Simulations for an older 65 nm technology and results reported in the literature (e.g. in [7], [8]) reveal local delay maxima for medium-sized $|\Delta|$. We conjecture these to be caused by input-output coupling capacitances, which introduce a current working against the intended behavior of the gate. If the input transitions are far apart $(|\Delta| \gg 0)$, the second one appears way after $t_{O}$, such that the introduced current has no impact. For decreasing $|\Delta|$, however, the second transition will eventually occur when $V_{O}$ is about to cross the threshold. Since the additional current has to be compensated by the driving transistor, the output slope decreases and thus the delay increases. Further reducing $\Delta$ first amplifies this effect until the closing of the second transistor leads to an increased conductivity that, overall, is able to make up for the added delay, causing it to finally drop again.

For rising output transitions, the behavior of the NOR is

[^2]

Fig. 2: Analog simulation results for the CMOS NOR gate.
quite different. First and foremost, the gate only switches after both inputs have changed (see Fig. 2c), resulting in the gate delay $\delta_{S}^{\uparrow}(\Delta)=t_{O}-\max \left(t_{A}, t_{B}\right)$. At the transistor level, each falling input transition causes one of the nMOS to stop conducting while simultaneously one of the pMOS gets closed. We emphasize that the shape of the output signal in Fig. 2c is essentially independent of $\Delta$, only the position in time varies. This is in accordance with the fact that there is only a single path connecting the output to $V_{D D}$.

The SIS delays $\delta_{S}^{\uparrow}(\infty)$ and $\delta_{S}^{\uparrow}(-\infty)$ again differ (see Fig. 2d), i.e., the gate delay depends on the order of the input transitions. Taking a closer look at the schematics in Fig. 1 reveals that an early transition on $A$ closes the topmost transistor and thus causes the internal node $N$ between the pMOS to be charged to $V_{D D}$. By contrast, an early transition on $B$ causes $N$ to be fully discharged, which obviously prolongs the transition time.

In any case, the gate delay for $|\Delta| \rightarrow 0$ increases, i.e., the MIS effect is a slow-down here. The causes are, once again, coupling capacitances, this time between $N$ and the input: If both inputs switch at the same time, the parasitic current (dis)charges $C_{N}$, possibly below $G N D$, since both adjacent transistors are still open. After they start to conduct, the additional charge has to be compensated, which explains the increased delay. Naturally, the delay variations depend on the initial value of $V_{N}$ and thus on the switching history of the gate. Note that we used the worst case ( $V_{N}=G N D$ ) in all our simulations.

## III. Simple hybrid ODE model

In our attempt to analytically express the gate delays of a NOR gate, we replace the transistors by zero-time switches: Depending on whether the appropriate input is above (logical 1) resp. below (logical 0) $V_{t h}=V_{D D} / 2$, an nMOS transistor is replaced by a fixed resistor $R<\infty$ or removed ( $R=\infty$ ), while a pMOS is handled in the opposite way. Note that this is similar to the approach used in [14], with the main difference that we added a capacitance at the internal node in the p-stack $\left(C_{N}\right)$ and one at the output ( $C_{O}$ ) (cf. Fig. 1). Thus, we end up with a system of coupled first-order differential equations.

## A. General solution

We briefly recall the general solution of first-order ODE systems first. Let $V: \mathbb{R} \rightarrow \mathbb{R}^{n}$ and $V^{\prime}=\frac{\mathrm{d}}{\mathrm{d} t} V$, and consider a homogeneous system of ordinary differential equations (ODEs) with constant coefficients $V^{\prime}(t)=A \cdot V(t)$; $A=\left[a_{i j}\right]^{n \times n} \in \mathbb{R}^{n \times n}$ and initial values $V(0)$. For a diagonizable matrix $A$, this system has a general solution

$$
V(t)=c_{1} \cdot \epsilon_{1} \cdot e^{\lambda_{1} t}+\ldots+c_{n} \cdot \epsilon_{n} \cdot e^{\lambda_{n} t}=c \cdot \phi(t)
$$

where $\left\{\left(\lambda_{i}, \epsilon_{i}\right)\right\}_{i=1}^{n}$ is a set of pairs consisting of $n$ eigenvalues and the corresponding eigenvectors of $A . c=\left[c_{1}, \ldots, c_{n}\right]^{T}$ is made up of arbitrary real constants determined by $V(0)$, and $\phi(t)=\left[\epsilon_{1} e^{\lambda_{1} t}, \ldots, \epsilon_{n} e^{\lambda_{n} t}\right]$ is the fundamental matrix solution of the homogeneous system. Moreover, the general solution to the non-homogeneous system $V^{\prime}(t)=A \cdot V(t)+g(t)$, for a continuous function $g: \mathbb{R} \rightarrow \mathbb{R}^{n}$, is given by the sum of the general solution of the corresponding homogeneous system $V(t)^{\prime}=A \cdot V(t)$ plus a particular solution to the nonhomogeneous one. To be more precise, $V(t)=\phi(t) \cdot c+\phi(t)$. $\int \phi^{-1}(s) \cdot g(s) d s$. We refer the interested reader to standard textbooks such as [15] for more information.

Since there are four different states $(0,0),(0,1),(1,0)$ and $(1,1)$ of the inputs $(A, B)$, interpreted as binary signals, we need to consider 4 different RC circuits and their corresponding ODE systems $V^{\prime}(t)=A \cdot V(t)+g(t) . V(t) \in \mathbb{R}^{2}$ is a two-element vector, representing the voltage $V_{N}$ at the internal node $N$ in Fig. 1, and the gate output voltage $V_{O}$, i.e.,

$$
V(t)=\binom{V_{N}}{V_{O}}
$$

while the non-homogeneous term $g(t)$ is either identically zero or a constant. In the sequel, we will evaluate $V(t)$ for each input combination individually.
B. System $(1,1): V_{A}=V_{D D}, V_{B}=V_{D D}$

If inputs $A$ and $B$ are above the threshold, both nMOS transistors are conducting and thus replaced by resistors (see Fig. 3a), causing the output $O$ to be discharged in parallel. By contrast, $N$ is completely isolated and keeps its value. Formally, we obtain


Fig. 3: First order RC approximations.

$$
\begin{aligned}
& C_{N} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{N}=0 \\
& C_{O} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{O}=I_{O}=-I_{3}-I_{4}=-V_{O} \cdot\left(\frac{1}{R_{3}}+\frac{1}{R_{4}}\right) .
\end{aligned}
$$

This homogeneous system can be rewritten in matrix form

$$
\binom{\frac{\mathrm{d}}{\mathrm{~d} t} V_{N}}{\frac{d}{\mathrm{~d} t} V_{O}}=\left(\begin{array}{cc}
0 & 0 \\
0 & -\left(\frac{1}{C_{0} R_{3}}+\frac{1}{C_{0} R_{4}}\right)
\end{array}\right) \cdot\binom{V_{N}}{V_{O}},
$$

which leads to the general solution

$$
\binom{V_{N}}{V_{O}}=c_{1}\binom{1}{0}+c_{2}\binom{0}{1} \cdot e^{-\left(\frac{1}{C_{O}^{R_{3}}}+\frac{1}{C_{O}^{R_{4}}}\right) t} .
$$

C. System $(1,0): V_{A}=V_{D D}, V_{B}=G N D$

Since $T_{1}$ and $T_{4}$ are open (see Fig. 3b), node $N$ is connected to $O$, and $O$ to GND. Note that both capacitances have to be discharged over resistor $R_{3}$, resulting in less current that is available for discharging $C_{O}$. More specifically, we observe $I_{O}=-I_{3}-I_{N}$ and hence obtain

$$
\begin{aligned}
& C_{N} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{N}=I_{N}=-\frac{V_{N}-V_{O}}{R_{2}}, \\
& C_{O} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{O}=I_{O}=-I_{3}-I_{N}=-\frac{V_{O}}{R_{3}}+\frac{V_{N}-V_{O}}{R_{2}} .
\end{aligned}
$$

The matrix form of this homogeneous system is

$$
\binom{\frac{\mathrm{d}}{\mathrm{~d} t} V_{N}}{\frac{\mathrm{~d}}{\mathrm{~d} t} V_{O}}=\left(\begin{array}{cc}
-\frac{1}{C_{N} R_{2}} & \frac{1}{C_{N} R_{2}} \\
\frac{1}{C_{0} R_{2}} & -\left(\frac{1}{C_{O} R_{2}}+\frac{1}{C_{O} R_{3}}\right)
\end{array}\right) \cdot\binom{V_{N}}{V_{O}}
$$

which has the general solution

$$
\binom{V_{N}}{V_{O}}=c_{1} \cdot\binom{\frac{1}{C_{N} R_{2}}}{\alpha+\beta} e^{\lambda_{1} t}+c_{2} \cdot\binom{\frac{1}{C_{N} R_{2}}}{\alpha-\beta} e^{\lambda_{2} t}
$$

where
$\alpha=\frac{C_{O} R_{3}-C_{N}\left(R_{2}+R_{3}\right)}{2 C_{O} C_{N} R_{2} R_{3}}$,
$\beta=\frac{\sqrt{\left(C_{O} R_{3}+C_{N}\left(R_{2}+R_{3}\right)\right)^{2}-4 C_{O} C_{N} R_{2} R_{3}}}{2 C_{O} C_{N} R_{2} R_{3}}$,
$\lambda_{1,2}=-\frac{C_{O} R_{3}+C_{N}\left(R_{2}+R_{3}\right)}{2 C_{O} C_{N} R_{2} R_{3}} \pm \beta$.
D. System $(0,1): V_{A}=G N D, V_{B}=V_{D D}$

Opening transistors $T_{2}$ and $T_{3}$, as shown in Fig. 3c, decouples the nodes $N$ and $O$ once again. We thus get the nonhomogeneous system of ODEs

$$
\begin{aligned}
& C_{N} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{N}=I_{N}=\frac{V_{D D}-V_{N}}{R_{1}}, \\
& C_{O} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{O}=I_{O}=-\frac{V_{O}}{R_{4}},
\end{aligned}
$$

which is in matrix representation

$$
\begin{aligned}
\binom{\frac{\mathrm{d}}{\mathrm{~d} t} V_{N}}{\frac{\mathrm{~d}}{\mathrm{~d} t} V_{O}} & =\left(\begin{array}{cc}
-\frac{1}{C_{N} R_{1}} & 0 \\
0 & -\frac{1}{C_{O} R_{4}}
\end{array}\right) \cdot\binom{V_{N}}{V_{O}} \\
& +\binom{\frac{V_{D D}}{C_{N} R_{1}}}{0} .
\end{aligned}
$$

It is easy to check that the fundamental matrix solution to the corresponding homogeneous system is

$$
\phi(t)=\left(\begin{array}{cc}
e^{-\frac{t}{C_{N} R_{1}}} & 0 \\
0 & e^{-\frac{t}{C_{O} R_{4}}}
\end{array}\right)
$$

leading to the general non-homogeneous solution

$$
\binom{V_{N}}{V_{O}}=\binom{c_{1} \cdot e^{-\frac{t}{C_{N} R_{1}}}+V_{D D}}{c_{2} \cdot e^{-\frac{t}{C_{O} R_{4}}}} .
$$

E. System $(0,0): V_{A}=G N D, V_{B}=G N D$

Closing both pMOS transistors, as shown in Fig. 3d, causes both capacitances to be charged over the same resistor $R_{1}$, similarly to system $(1,0)$. Since $I_{O}=I_{1}-I_{N}$, the ODE system describing the behavior is

$$
\begin{aligned}
& C_{O} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{O}=I_{O}=\frac{V_{N}-V_{O}}{R_{2}} \\
& C_{N} \cdot \frac{\mathrm{~d}}{\mathrm{~d} t} V_{N}=I_{N}=I_{1}-I_{O}=\frac{V_{D D}-V_{N}}{R_{1}}-\frac{V_{N}-V_{O}}{R_{2}},
\end{aligned}
$$

which is a non-homogeneous system, with the matrix form

$$
\begin{aligned}
\binom{\frac{\mathrm{d}}{\mathrm{~d} t} V_{N}}{\frac{\mathrm{~d}}{\mathrm{~d} t} V_{O}}= & \left(\begin{array}{cc}
-\left(\frac{1}{C_{N} R_{1}}+\frac{1}{C_{N} R_{2}}\right) & \frac{1}{C_{N} R_{2}} \\
\frac{1}{C_{O} R_{2}} & -\frac{1}{C_{O} R_{2}}
\end{array}\right) \\
& \binom{V_{N}}{V_{O}}+\binom{\frac{V_{D D}}{C_{N} R_{1}}}{0}
\end{aligned}
$$



Fig. 4: Temporal evolution of the trajectories for all systems.

By straightforward but tedious calculations, it follows that the fundamental matrix solution of the homogeneous system is

$$
\phi(t)=\left(\begin{array}{cc}
\frac{1}{C_{N} R_{2}} \cdot e^{\lambda_{1} t} & \frac{1}{C_{N} R_{2}} \cdot e^{\lambda_{2} t} \\
(\alpha+\beta) \cdot e^{\lambda_{1} t} & (\alpha-\beta) \cdot e^{\lambda_{2} t}
\end{array}\right)
$$

where
$\alpha=\frac{C_{O}\left(R_{1}+R_{2}\right)-C_{N} R_{1}}{2 C_{O} C_{N} R_{1} R_{2}}$,
$\beta=\frac{\sqrt{\left(C_{N} R_{1}+C_{O}\left(R_{1}+R_{2}\right)\right)^{2}-4 C_{O} C_{N} R_{1} R_{2}}}{2 C_{O} C_{N} R_{1} R_{2}}$,
$\gamma=-\frac{C_{N} R_{1}+C_{O}\left(R_{1}+R_{2}\right)}{2 C_{O} C_{N} R_{1} R_{2}}$,
$\lambda_{1,2}=\gamma \pm \beta$.

The general solution of the non-homogeneous system is

$$
\binom{V_{N}}{V_{O}}=\binom{\frac{c_{1}}{C_{N} R_{2}} e^{\lambda_{1} t}+\frac{c_{2}}{C_{N} R_{2}} e^{\lambda_{2} t}+V_{D D}}{c_{1} \cdot(\alpha+\beta) e^{\lambda_{1} t}+c_{2} \cdot(\alpha-\beta) e^{\lambda_{2} t}+V_{D D}}
$$

## F. Trajectory Comparison

Fig. 4 depicts the signals $V_{N / O}(n, m)(t)$ over time $t$ in system $(n, m)$. The initial values were set to $V_{N}(0)=V_{O}(0)=$ $V_{D D}$, with the exception of $V_{N}(0,0)(0)=V_{O}(0,0)(0)=$ $G N D$ and $V_{N}(1,1)(0)=V_{D D} / 2$. Compared to the cases where only one nMOS is closed, the output trajectory of system $(1,1)$ is much steeper. Note that this is in line with the considerations for the speed-up MIS effect in Section II.

## IV. Modeling MIS Effects

In this section, we will investigate how well our simple hybrid ODE model is capable of faithfully representing the MIS effects described in Section II. It turns out that the speedup is modeled appropriately, whereas the slow-down is only partially covered. Note that also the approaches presented in [11], [12] struggled with this effect, such that the authors finally resorted to fitting the delays for these cases.

For our analysis, we computed the delay as a function of the input separation time $\Delta=t_{B}-t_{A}$ for falling and rising

TABLE I: Empirically obtained parameter values

| Parameter | Value |
| :---: | :---: |
| $R_{1}$ | $37.088 \times 10^{3} \Omega$ |
| $R_{2}$ | $44.926 \times 10^{3} \Omega$ |
| $R_{3}$ | $45.150 \times 10^{3} \Omega$ |
| $R_{4}$ | $48.761 \times 10^{3} \Omega$ |
| $C_{N}$ | $59.486 \times 10^{-18} \mathrm{~F}$ |
| $C_{O}$ | $617.259 \times 10^{-18} \mathrm{~F}$ |

output transitions, and compared it with our analog simulation results (cf. Fig. 2b and Fig. 2d). Similar to Section II, we start with a falling output transition. To compute the delay for a given $\Delta$, we need to combine two solutions:
$1)$ : Starting in the system $(0,0)$ initially, which models a gate whose inputs have been 0 for a very long time, we switch to $(1,0)$ resp. $(0,1)$ at time $t=0$ and compute the corresponding trajectory.
2): When in the mode entered in 1), we switch to system $(1,1)$ at time $t_{s}$, and determine $t_{O}$ where $V_{O}\left(t_{O}\right)=V_{D D} / 2$. The delay is extracted as $t_{O}-\min \left(t_{A}, t_{B}\right)=t_{O}$, since the earlier of the two inputs triggers the output transition. Starting in system $(1,0)$ results in $\Delta=t_{s}$, whereat for system $(0,1)$ we get $\Delta=-t_{s}$, which accounts for the reversed order of the input transitions.

The calculation of the rising output delay is carried out analogously, with the exception that we start in the system $(1,1)$ initially and switch to $(1,0)(\Delta<0)$ resp. $(0,1)(\Delta>$ 0 ) at $t=0$, before turning to $(0,0)$ at $t_{s}$. The sought delay is now equal to $t_{O}-\max \left(t_{A}, t_{B}\right)=t_{O}-t_{s}$, since it is the later of the two inputs that initiates the output change. Note carefully, however, that it is unfortunately not clear which initial value to use for $V_{N}$ in the system $(1,1)$ here: As the latter does not change the value of $V_{N}(t)$ at all, the proper initial value would be the actual value of $V_{N}$ in the state $(m, n)$ the system was in before/at the switch to $(1,1)$ occurred.

For a quantitative comparison, we parameterized the resistances and capacitances in our model using a least square fitting approach, with the goal to match the output threshold crossing times $\delta_{S}^{\uparrow}( \pm \infty)$ and $\delta_{S}^{\uparrow}(0)$ resp. $\delta_{S}^{\downarrow}( \pm \infty)$ and $\delta_{S}^{\downarrow}(0)$ shown in Fig. 2. Interestingly, simultaneous fitting of all three data points turned out to be impossible, even for the "wellbehaved" case of falling output transitions. To understand why, we derived analytic expressions for the values

$$
\delta^{\downarrow}(-\infty) \approx \ln (2) \cdot C_{O} R_{4} \quad \text { and } \quad \delta^{\downarrow}(0)=\frac{\ln (2) \cdot C_{O} R_{3} R_{4}}{R_{3}+R_{4}}
$$

(as well as for $\delta^{\downarrow}(\infty), \delta^{\uparrow}(-\infty), \delta^{\uparrow}(0)$ and $\delta^{\uparrow}(\infty)$ ), by inverting the explicit formulas of our trajectories. Unfortunately, necessary simplifications that enabled these calculations induced some approximation errors, which made a direct computation of the desired parameters impossible.

Nevertheless, important insights could be gained. More specifically, since $R_{3}$ and $R_{4}$ are the on-resistors of the two nMOS transistors and should hence be roughly the same, we obtain $\frac{\delta^{\downarrow}(-\infty)}{\delta^{\downarrow}(0)} \approx \frac{R_{3}+R_{4}}{R_{3}} \approx 2$. Since the desired ratio


Fig. 5: Computed MIS delays for falling output transitions.
according to our simulations (see Fig. 2) is $\frac{\delta_{S}^{\downarrow}(-\infty)}{\delta_{S}^{\downarrow}(0)} \approx \frac{38 \mathrm{ps}}{28 \mathrm{ps}}$, however, we could not even simultaneously fit these two values with reasonable choices for $R_{3}$ and $R_{4}$.

We solved the problem by adding (that is, subtracting) a pure delay $\delta_{\min }=18 \mathrm{ps}$, also present in the original IDM, which defers the switching to the new state upon an input transition. This results in an effective ratio of $\frac{20 \mathrm{ps}}{10 \mathrm{ps}}=2$, which could finally be matched by least squares fitting, leading to the parameter values presented in Table I. To also accommodate $\delta_{\text {min }}$ in the MIS delay computations, we just need to transform $t_{O}-\min \left(t_{A}, t_{B}\right)=t_{O}$ to $\delta_{M}^{\downarrow}(\Delta)=t_{O}+\delta_{\text {min }}$ and, correspondingly, $\delta_{M}^{\uparrow}(\Delta)=t_{O}-t_{s}+\delta_{\min }$. Note that the same $\delta_{\text {min }}=18 \mathrm{ps}$ was also used for rising output transitions.

Utilizing the found parameters, we can finally visualize the delay predictions of our model. Fig. 5 shows the very good fit of $\delta_{M}^{\downarrow}(\Delta)$ for a falling output transition compared to the ana$\log$ simulation results presented in Section II. Unfortunately, a comparable coverage of the MIS effects for rising output transitions cannot be achieved (see Fig. 6): For none of the initial values $V_{N} \in\left\{G N D, V_{D D} / 2, V_{D D}\right\}$, the computed delay $\delta_{M}^{\uparrow}(\Delta)=t_{O}-t_{s}+\delta_{\text {min }}$ reasonably matches $\delta_{S}^{\uparrow}(\Delta)$ obtained in our analog simulations. More specifically, for $V_{N}=V_{D D}$ and $V_{N}=V_{D D} / 2$, our simple ODE model fails to correctly predict the case of $\Delta<0$, i.e., switching to system $(1,0)$ at $t=0$ and then to $(0,0)$ at time $t=\Delta$. In the case of $V_{N}=G N D$, which reasonably matches $\delta_{S}^{\uparrow}( \pm \infty)$ and $\delta_{S}^{\downarrow}( \pm \infty)$ and thus has been used in Section VI, it fails to model the MIS peak around $\Delta=0$ in Fig. 2d for small negative and positive $\Delta$.

We conclude that our simple ODE model perfectly captures the MIS effects caused by the parallel transistors, but not for the ones caused by transitors arranged in series.

## V. Parametrization

In order to apply our hybrid model in practice, in particular, for digital timing simulations using the Involution Tool, one needs to compute the input-to-output delay functions for all possible state transitions, including the ones shown in Fig. 5 and Fig. 6. This, in turn, requires a proper parametrization of our model, i.e., the determination of the parameters


Fig. 6: Computed MIS delays for rising output transitions.
$R_{1}, \ldots, R_{4}, C_{N} C_{O}$ that cause our model to match the actual delays of a given NOR gate in a circuit as good as possible.

There is no unique and possibly even optimal parametrization approach, but it is natural to match Fig. 5 and Fig. 6 (for $\Delta>0$ ) to Fig. 2b and Fig. 2d as close as possible. For this purpose, it is sufficient to match the characteristic Charlie delay values $\delta^{\downarrow}(-\infty), \delta^{\downarrow}(0), \delta^{\downarrow}(\infty)$ in Fig. 2b (falling output transition) and the corresponding values $\delta^{\uparrow}(-\infty), \delta^{\uparrow}(0)$, $\delta^{\uparrow}(\infty)$ in Fig. 2d.

Below, we provide exact or approximate ${ }^{3}$ analytic formulas ${ }^{4}$ for the characteristic Charlie delay values in Fig. 5 and Fig. 6 in terms of the parameters $\left(R_{1}-R_{4}, C_{N}\right.$, and $\left.C_{O}\right)$. These expressions will allow us to understand which parameters affect the which value, and could even be used for explicit parametrization of a circuit with given characteristic Charlie delays.

For falling output transitions (Fig. 5, $\Delta=0$ ), an exact formula for $\delta^{\downarrow}(0)$ is

$$
\begin{equation*}
\delta^{\downarrow}(0)=\frac{-\ln (0.5)}{\frac{1}{C_{O} R_{3}}+\frac{1}{C_{O} R_{4}}} \tag{8}
\end{equation*}
$$

For falling output transitions (Fig. 5, $\Delta=-\infty$ ) an exact formula for computing $\delta^{\downarrow}\left(-2 \times 10^{-10}\right) \approx \delta^{\downarrow}(-\infty)$ is

$$
\begin{equation*}
\delta^{\downarrow}\left(-2 \times 10^{-10}\right)=-\ln (0.5) \cdot C_{O} R_{4} \tag{9}
\end{equation*}
$$

For falling output transitions (Fig. 5, $\Delta=\infty$ ), an approximation to compute $d=\delta^{\downarrow}\left(2 \times 10^{-10}\right) \approx \delta^{\downarrow}(\infty)$ is
$d \approx \frac{0.6-\left[c_{1}(\alpha+\beta) e^{\lambda_{1} w}\left(1-\lambda_{1} w\right)+c_{2}(\alpha-\beta) e^{\lambda_{2} w}\left(1-\lambda_{2} w\right)\right]}{c_{1}(\alpha+\beta) \lambda_{1} e^{\lambda_{1} w}+c_{2}(\alpha-\beta) \lambda_{2} e^{\lambda_{2} w}}$,

[^3]where $\alpha, \beta, \lambda_{1,2}$ are given in (1), (2), and (3), respectively, and
$w=10^{-10}$,
$c_{2}=\frac{0.6\left[\left((\alpha+\beta) C_{N} R_{2}\right)-1\right]}{\beta}$,
$c_{1}=\left(V_{D D} C_{N} R_{2}\right)-c_{2}$.

For rising output transitions (Fig. $6, \delta^{\uparrow}(\Delta)$ for any $\Delta \geq 0$ and initial value $\left.V_{N}^{( } 0\right)=X$ ), an approximation for $d=\delta^{\uparrow}(\Delta)$ is

$$
\begin{align*}
d \approx & \frac{0.6-l-c_{1}^{\Delta} \cdot(\alpha+\beta) e^{\lambda_{1} w}\left(1-\lambda_{1} w\right)}{c_{1}^{\Delta} \cdot(\alpha+\beta) \lambda_{1} e^{\lambda_{1} w}+c_{2}^{\Delta} \cdot(\alpha-\beta) \lambda_{2} e^{\lambda_{2} w}}  \tag{11}\\
& -\frac{c_{2}^{\Delta} \cdot(\alpha-\beta) e^{\lambda_{2} w}\left(1-\lambda_{2} w\right)}{c_{1}^{\Delta} \cdot(\alpha+\beta) \lambda_{1} e^{\lambda_{1} w}+c_{2}^{\Delta} \cdot(\alpha-\beta) \lambda_{2} e^{\lambda_{2} w}}-\Delta
\end{align*}
$$

where $\alpha, \beta, \gamma$, and $\lambda_{1,2}$ are respectively equal to (4), (5), (6), and (7). Moreover, we have

$$
\begin{aligned}
& w=2 \times 10^{-10} \\
& l=\frac{V_{D D}\left(-\alpha^{2}+\beta^{2}\right) R_{2}}{R_{1}\left(\gamma^{2}-\beta^{2}\right)} \\
& c_{2}^{\Delta}=\frac{\left(\left[(\alpha+\beta) V_{N}^{(0,1)}(\Delta)\right]+a+b\right) C_{N} R_{2}}{2 \beta e^{\lambda_{2} \Delta}} \\
& c_{1}^{\Delta}=\frac{\left[(\alpha+\beta) V_{N}^{(0,1)}(\Delta)-c_{2} \frac{\alpha+\beta}{C_{N} R_{2}} e^{\lambda_{2} \Delta}+a\right] C_{N} R_{2}}{(\alpha+\beta) e^{\lambda_{1} \Delta}} \\
& a=\frac{V_{D D}(\alpha+\gamma)(\alpha+\beta)}{C_{N} R_{1}\left(\gamma^{2}-\beta^{2}\right)} \\
& b=\frac{V_{D D}\left(-\alpha^{2}+\beta^{2}\right)}{C_{N} R_{1}\left(\gamma^{2}-\beta^{2}\right)} \\
& V_{N}^{(0,1)}(\Delta)=V_{D D}+\left(X-V_{D D}\right) e^{\frac{-\Delta}{C_{N} R_{1}}}
\end{aligned}
$$

Recall that one does not usually have information about the initial value $V_{N}^{(0,1)}(0)=X$; Fig. 6 shows $X=0, X=V_{D D} / 2$ and $X=V_{D D}$.

For rising output transitions (Fig. 6, $\delta^{\uparrow}(\Delta)$ for any $\Delta<0$ and initial value $\left.V_{N}^{( } 0\right)=X$ ), an approximation for $d=\delta^{\uparrow}(\Delta)$ is

$$
\begin{aligned}
d \approx & \frac{0.6-l-c_{1}^{\Delta} \cdot(\alpha+\beta) e^{\lambda_{1} w}\left(1-\lambda_{1} w\right)}{c_{1}^{\Delta} \cdot(\alpha+\beta) \lambda_{1} e^{\lambda_{1} w}+c_{2}^{\Delta} \cdot(\alpha-\beta) \lambda_{2} e^{\lambda_{2} w}} \\
& -\frac{c_{2}^{\Delta} \cdot(\alpha-\beta) e^{\lambda_{2} w}\left(1-\lambda_{2} w\right)}{c_{1}^{\Delta} \cdot(\alpha+\beta) \lambda_{1} e^{\lambda_{1} w}+c_{2}^{\Delta} \cdot(\alpha-\beta) \lambda_{2} e^{\lambda_{2} w}}-|\Delta|
\end{aligned}
$$

where $l, \alpha, \beta, \gamma, \lambda_{1,2}, a$, and $b$, are as same as Case 4 and

$$
\begin{aligned}
& w=10^{-10} \\
& c_{2}^{\Delta}=\frac{\left(\left[(\alpha+\beta) V_{N}^{(1,0)}(\Delta)-\frac{V_{o}^{(1,0)}(\Delta)}{C_{N} R_{2}}\right]+a+b\right) C_{N} R_{2}}{2 \beta e^{\lambda_{2} \Delta}} \\
& c_{1}^{\Delta}=\frac{\left[(\alpha+\beta) V_{N}^{(1,0)}(\Delta)-c_{2} \frac{\alpha+\beta}{C_{N} R_{2}} e^{\lambda_{2} \Delta}+a\right] C_{N} R_{2}}{(\alpha+\beta) e^{\lambda_{1} \Delta}} \\
& V_{N}^{(1,0)}(\Delta)=\frac{g_{1}}{C_{N} R_{2}} e^{(z+y) \Delta}+\frac{g_{2}}{C_{N} R_{2}} e^{(z-y) \Delta} \\
& V_{O}^{(1,0)}(\Delta)=g_{1}(x+y) e^{(z+y) \Delta}+g_{2}(x-y) e^{(z-y) \Delta} \\
& z=-\frac{C_{O} R_{3}+D\left(R_{2}+R_{3}\right)}{2 C_{O} C_{N} R_{2} R_{3}}
\end{aligned}
$$

with $x=\alpha$ and $y=\beta$ given by (1) and (2) and $g_{1}=\frac{(y-x) g_{2}}{x+y}$.
Again, since the initial value of $X=V_{N}^{(1,0)}(0)$ is usually unknown, we consider only the cases $X=0, X=V_{D D} / 2$ and $X=V_{D D}$ shown in Fig. 6, which lead to

- if $X=0$, then $g_{2}=0$,
- If $X=V_{D D}$, then $g_{2}=\frac{0.6(x+y) D R_{2}}{y}$,
- If $X=V_{D D} / 2$, then $g_{2}=\frac{0.3(x+y) D R_{2}}{y}$.

It is apparent from (8)-(10) that the characteristic Charlie delays in Fig. 5 are not affected by $R_{1}$ at all. To be more precise, $\delta^{\downarrow}(0)$ is determined by $C_{O}, R_{3}$, and $R_{4}$, while $\delta^{\downarrow}(-\infty)$ is determined by $C_{O}$ and $R_{4}$ only; $\delta^{\downarrow}(\infty)$ is affected by $C_{N}, C_{O}, R_{2}$, and $R_{3}$. On the other hand, the characteristic Charlie delays $\delta^{\uparrow}(0)$ and $\delta^{\uparrow}(\infty)$ in Fig. 6, which seems to match Fig. 2 d best, are only affected by $C_{N}, C_{O}, R_{1}$, and $R_{2}$ according to (11). Finally, (12) reveals that $\delta^{\uparrow}(-\infty)$ does not depend on $R_{4}$.

One immediate consequence of this is that $R_{3}$ and $R_{4}$ are fixed already by matching $\delta^{\downarrow}(0)$ and $\delta^{\downarrow}(-\infty)$. To simultaneously match $\delta^{\downarrow}(\infty)$, in theory, $C_{N}$ and $R_{2}$ were still available, but since their influence on $\delta^{\downarrow}(\infty)$ is very small, this is not always effective. Even worse, according to (8) and (9), it may even be impossible to find a parametrization for $R_{3}$ and $R_{4}$ that allows to match even the two characteristic Charlie delay values $\delta^{\downarrow}(0)$ and $\delta^{\downarrow}(-\infty)$ simultaneously, which happens in the case of too large a ratio of $\delta^{\downarrow}(-\infty) / \delta^{\downarrow}(0)$. And indeed, as already mentioned, a pure delay of $\delta_{\min }=18 \mathrm{ps}$ had to be subtracted from all these delay values in order to be able to determine a matching set of parameters.

We conclude this section by noting that relying on the characteristic Charlie delays from Fig. 6 for $V_{N}=X=0$ for parametrization makes sense, since the system $(0,0)$ starts, at time $\Delta$, from $V_{D D}$ in this case, i.e., a value not affected by $X$. This is in accordance with the fact that our model does reasonably capture the Charlie-effect in Fig. 2d for the case $\Delta \geq 0$ (that is, for $X=0$ ). It is apparent, though, that the parasitic capacitance $C_{N}$ has a substantial influence on the characteristic Charlie delays, as it is a factor in the denominator of $\delta^{\uparrow}(0)$ and $\delta^{\uparrow}(\infty)$. Like the invariance of $V_{N}$ in the system $(1,1)$, which has already been identified in Section IV as the main cause for our model's inability to fully


Fig. 7: Accuracy of inertial delay, Exp-Channel and hybrid model compared to analog simulations of a NOR gate. Lower bars indicate better results.
cover the Charlie effect, this is an unwanted artefact of our simplistic modeling.

## VI. Modeling Accuracy

In this section, we will compare our hybrid model to inertial delays and the IDM. To be able to do so, we added our model to the publicly available Involution Tool [5]. Previously, all channel implementations had to be written in VHDL. However, since this approach was already rather tedious for a SumExp-Channel, where the inverse of the trajectory had to be numerically approximated, we decided to come up with a new way of implementing channels: Using the QuestaSim Foreign Language Interface (FLI) [16] allowed us to escape the Involution Tool's standard VHDL environment and to execute C code. In a second step, Python code was called from C, which finally implemented our hybrid channels. This approach enabled us to utilize the complete Python ecosystem, which reduces the effort the hybrid channel implementation itself drastically.
For the evaluation, we again used the 15 nm Nangate Open Cell Library featuring FreePDK15 ${ }^{\mathrm{TM}}$ FinFET models [13] $\left(V_{D D}=0.8 \mathrm{~V}\right)$. Based on a Verilog description of a NOR gate, we utilized the Cadence tools Genus and Innovus (version 19.11) to perform optimization, placement and routing. Finally, we extracted the parasitic networks from the final layout to obtain SPICE models, which we used as golden reference in analog Spectre (version 19.1) simulations.

Using the parameter set introduced in Table I, we performed simulations for various waveform configurations, ranging from very short to broad pulses. Each simulation consisted of 500 transitions, except for the last simulation, where we generated 250 transitions. The simulations have been repeated 20 times, and the averaged results are presented in Fig. 7. The waveform configuration 100/50-LOCAL describes the case where transitions are created individually for each input, according to a normal distribution, with $\mu=100 \mathrm{ps}$ and $\sigma=50 \mathrm{ps}$. GLOBAL indicates that the transitions are not calculated separately for each input but rather for all inputs together. This option allows to test how accurately the delay models perform for large absolute values of $\Delta$, since concurrent transitions are unlikely with this configuration.

The results are compared in terms of the deviation area, which is calculated as follows: The digitized SPICE traces are


Fig. 8: Matching of the hybrid model with and without pure delay for falling output transitions.
subtracted from the corresponding traces of the digital delay model and the absolute area is summed up. Since absolute values are meaningless, the results are normalized with the inertial delay as baseline.

For short pulses ( $\mu=100 \mathrm{ps}, \mu=200 \mathrm{ps}$ ), the superiority of the hybrid model with $\delta_{\text {min }}$ can be clearly seen. The deviation area is less than half that of the inertial delays. Moreover, it also outperforms the Exp-Channel, which we chose as representation for the IDM in the Involution Tool, with $\delta_{\text {min }}=20 \mathrm{ps}$. Note that we had to determine the latter empirically, since there is no proper parametrization of IDM channels representing multi-input gates available. The hybrid model without pure delay performs worse, which is primarily due to the imperfect delay matching, which can be seen in Fig. 8. Note that the pure delay shows no effect for rising input transitions. We should also emphasize that, for the first two waveform configurations, a lot of transitions are happening within a range of $\Delta=[-40 \mathrm{ps}, 40 \mathrm{ps}]$, where the hybrid model without pure delay has deficiencies.

For broader pulses ( $\mu=2 \mathrm{~ns}, \mu=5 \mathrm{~ns}$ ), which are covered by the last two waveform configurations, it can be seen that the hybrid model and the inertial delay model perform similar. This is due to the fact that $|\Delta| \gg 100 \mathrm{ps}$, where the matching is nearly perfect. The Exp-Channel shows deficiencies for broad pulses, which is caused by placing the delay channel at the output and the consequential inability to determine which input caused the transition. Since $\delta_{S}^{\uparrow}(\infty)$ and $\delta_{S}^{\uparrow}(-\infty)$ differ, (cf. Fig. 5 and Fig. 6) the Exp-Channel simply delays the transition by their average, which explains the observed inaccuracies.

In terms of simulation runtime, our simple experiments reveal a minor overhead of the hybrid model compared to the simple inertial delay model or the Exp-Channel of $6 \%$, which seems acceptable in view of the increased modeling accuracy. For more robust numbers, more extensive simulation runs are necessary, which we are planning to execute in the near future.

## VII. Conclusions

We introduced a simple hybrid ODE model for a twoinput NOR gate, which naturally generalizes the hybrid analog
model corresponding to standard single-input, single-output involution channels. The ODEs governing the switching waveforms of the output, based on the state of the inputs, have been obtained by replacing transistors with ideal switches in a simple RC model of the circuit. By analytically solving the resulting ODE systems, we obtained a digital gate delay model that faithfully reproduces all MIS effects, except in one particular situation. We also incorporated our hybrid model in the Involution Tool for digital timing analysis and compared the average accuracy for random traces in a custom circuit for different channel models. Our results show that our new hybrid model outperforms both classic involution channels and standard inertial delay channels with respect to modeling accuracy.
Future work will be devoted to the question of whether our multi-input digital delay channels are continuous with respect a certain metric, and therefore lead to a faithful model. In addition, we will look out for alternative models that fully capture all MIS effects.

## REFERENCES

[1] S. H. Unger, "Asynchronous sequential switching circuits with unrestricted input changes," IEEE Transaction on Computers, vol. 20, no. 12, pp. 1437-1444, 1971.
[2] M. J. Bellido-Díaz, J. Juan-Chico, and M. Valencia, Logic-Timing Simulation and the Degradation Delay Model. London: Imperial College Press, 2006.
[3] M. Függer, R. Najvirt, T. Nowak, and U. Schmid, "A faithful binary circuit model," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 10, pp. 2784-2797, 2020.
[4] M. Függer, T. Nowak, and U. Schmid, "Unfaithful glitch propagation in existing binary circuit models," IEEE Transactions on Computers, vol. 65, no. 3, pp. 964-978, March 2016.
[5] D. Öhlinger, J. Maier, M. Függer, and U. Schmid, "The involution tool for accurate digital timing and power analysis," Integration, vol. 76, pp. 87 - 98, 2021.
[6] L.-C. Chen, S. K. Gupta, and M. A. Breuer, "A new gate delay model for simultaneous switching and its applications," in Proceedings of the 38th Design Automation Conference (IEEE Cat. No.01CH37232), 2001, pp. 289-294.
[7] A. R. Subramaniam, J. Roveda, and Y. Cao, "A finite-point method for efficient gate characterization under multiple input switching," ACM Trans. Des. Autom. Electron. Syst., vol. 21, no. 1, pp. 10:1-10:25, Dec. 2015. [Online]. Available: http://doi.acm.org/10.1145/2778970
[8] J. Shin, J. Kim, N. Jang, E. Park, and Y. Choi, "A gate delay model considering temporal proximity of multiple input switching," in 2009 International SoC Design Conference (ISOCC), Nov 2009, pp. 577-580.
[9] J. Sridharan and T. Chen, "Modeling multiple input switching of cmos gates in dsm technology using hdmr," in Proceedings of the Design Automation Test in Europe Conference, vol. 1, March 2006, pp. 6 pp.-.
10] O. V. S. Shashank Ram and S. Saurabh, "Modeling multiple-input switching in timing analysis using machine learning," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 40, no. 4, pp. 723-734, 2021.
111] E. Melcher, W. Röthig, and M. Dana, "Multiple input transitions in cmos gates," Microprocessing and Microprogramming, vol. 35, no. 1, pp. $683-690$, 1992, software and Hardware: Specification and Design. [Online]. Available: http://www.sciencedirect.com/science/ article/pii/016560749290387M
[12] N. Abdallah and P. Bazargan-Sabet, "Modeling the effects of input slew rate and temporal proximity of input transitions in event-driven simulation," in 2006 Proceeding of the Thirty-Eighth Southeastern Symposium on System Theory, March 2006, pp. 185-189.
[13] M. Martins, J. M. Matos, R. P. Ribas, A. Reis, G. Schlinker, L. Rech, and J. Michelsen, "Open cell library in 15 nm freepdk technology," in Proceedings of the 2015 Symposium on International Symposium on Physical Design, ser. ISPD '15. New York,

NY, USA: ACM, 2015, pp. 171-178. [Online]. Available: http: //doi.acm.org/10.1145/2717764.2717783
[14] E. Schneider, S. Holst, X. Wen, and H.-J. Wunderlich, "Data-parallel simulation for fast and accurate timing validation of cmos circuits," in 2014 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2014, pp. 17-23.
[15] G. Strang, Differential equations and linear algebra. WellesleyCambridge Press Wellesley, 2014.
[16] Mentor Graphics Corporation, Foreign Language Interface Manual, 2016, Software Version 10.5c.


[^0]:    This research was partially funded by the Austrian Science Fund (FWF) projects DMAC (P32431).

[^1]:    ${ }^{1}$ One mode for generating a rising transition switching waveform, and one for the falling one.

[^2]:    ${ }^{2}$ We ran our simulations with an older technology library ( 65 nm ) as well, which confirmed the delay values reported in the literature.

[^3]:    ${ }^{3}$ Note that all the errors related to the approximations we describe in this section is in $O\left(t^{2}\right)$, where $t$ is very small $\left(t \leq 2 \times 10^{-10}\right)$. The error is hence so small that it can be ignored in practice.
    ${ }^{4}$ It is worth noting that in parallel with obtaining these equations, we used built-in MATLAB software functions (e.g. the non-linear optimization function fminbnd) to validate the equations.

